mosaic

Mosaic Semiconductor Inc.

8K x 8 SRAM

MSM88-10/12/15

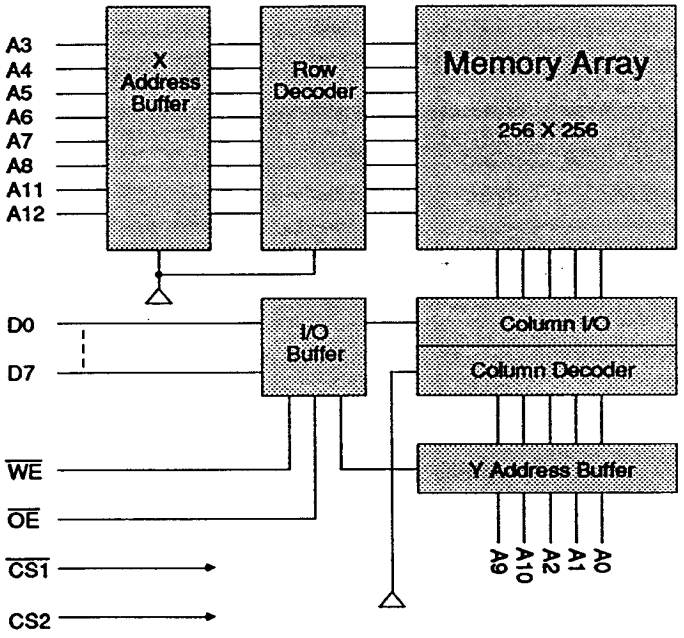
Issue 3.1 : October 1989

8, 192 x 8 CMOS High Speed Static RAM

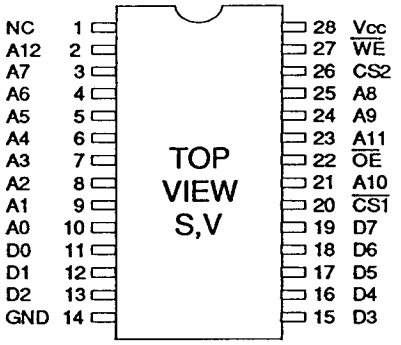
Features

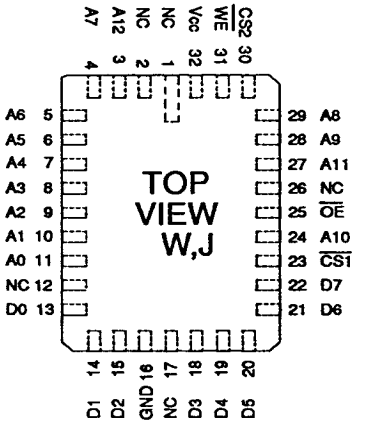
Access Times of 100/120/150 ns
JEDEC Standard 28 pin DIL/32 pad LCC,JLCC
28 pin VIL™ Package Available.
Low Power Standby 5mW (typ.)
10µW (typ.)-L Version
Completely Static Operation
Battery Back-up Capability
Common Data Inputs & Outputs
May be Processed to MIL-STD-883C (suffix MB)

Block Diagram



Pin Definitions





Pin Functions

A0-A12	Address inputs
D0-7	Data Input/Output
CS1,CS2	Chip Selects
OE	Output Enable
WE	Write Enable
Vcc	Power(+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
28	0.6" Dual-in-Line (DIP)	S	Ceramic	JEDEC
28	0.1" Vertical-in-LIne (VIL™)	V	Ceramic	JEDEC
32	Leadless Chip Carrier (LCC)	W	Ceramic	JEDEC
32	'J' Leaded Chip Cariier (JLCC)	J	Ceramic	JEDEC

Package dimensions and outlines are displayed on page 6.

VIL PAT PENDING

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	2	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse Width:-1 v for 50ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (88I)
	T_{AM}	-55	-	125	°C (88M,MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=Gnd to V_{CC}	-	-	2.0	µA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH}, or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	-	-	2.0	µA
Operating Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA,	-	4	80	mA
Average Supply Current	I_{CC1}	Min. Cycle, duty=100%, $I_{I/O}$=0mA	-	60	110	mA
Standby Supply Current	I_{SB}	$\overline{CS1}$=V_{IH}, or CS2=V_{IL}	-	1	3	mA
-L Part	I_{SB1}*	$\overline{CS1}$, CS2≥V_{CC}-0.2V, or CS2≤0.2V, I/P's<0.2V or V_{CC}-0.2V	-	2	100	µA
-L Part	I_{SB2}*	CS2≤0.2V	-	2	100	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading

*V_{IL} min.=-0.3V

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	-	6	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

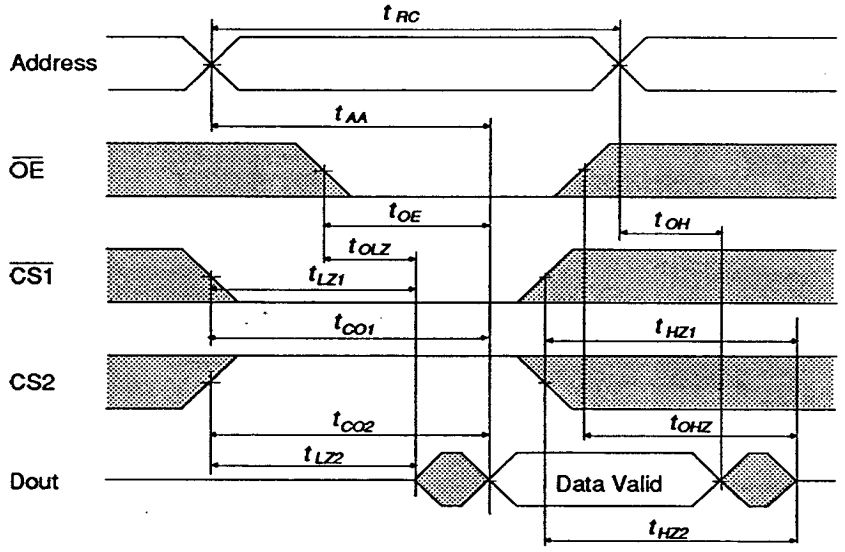
* Input pulse levels: 0.6V to 2.4V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF (including scope & jig)
* V_{CC}=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	100	-	120	-	150	ns
Chip Selection to Output ($\overline{CS1}$)	t_{CO1}	-	100	-	120	-	150	ns
Chip Selection to Output (CS2)	t_{CO2}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	50	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	15	-	ns
Chip Selection to Output in Low Z($\overline{CS1}$)	t_{LZ1}	10	-	10	-	15	-	ns
Chip Selection to Output in Low Z(CS2)	t_{LZ2}	10	-	10	-	15	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z($\overline{CS1}$)	t_{HZ1}	0	35	0	40	0	50	ns
Chip Deselection to Output in High Z(CS2)	t_{HZ2}	0	35	0	40	0	50	ns

Read Cycle Timing Waveform (1,2,3)



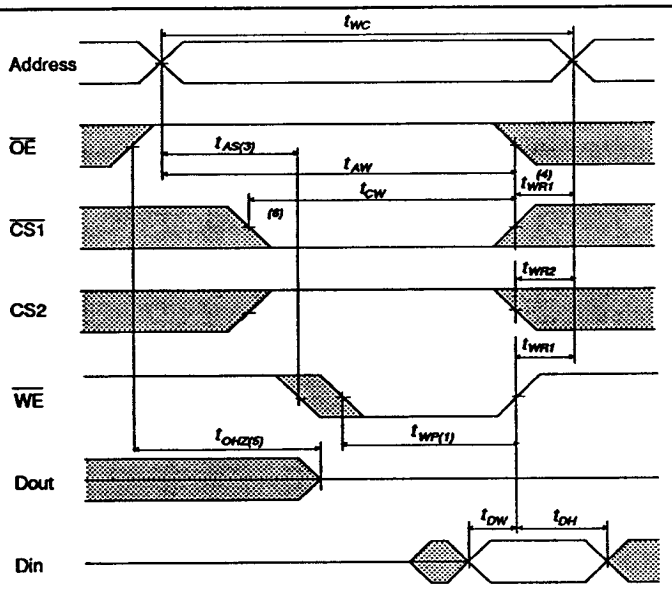
Notes:

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for Read Cycle.

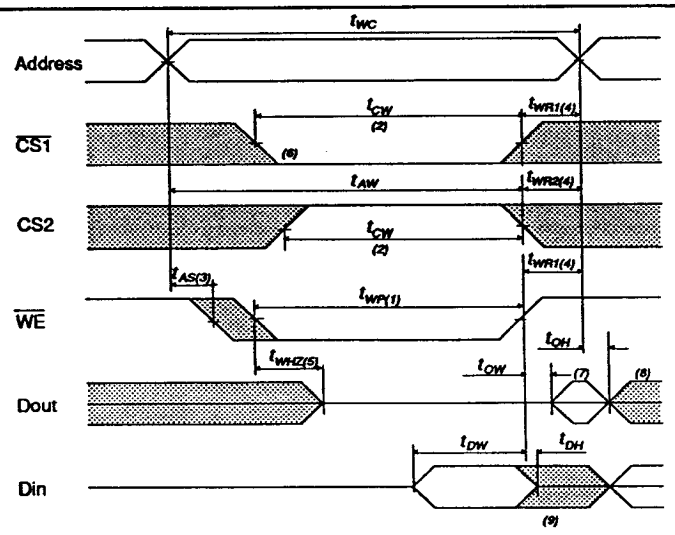
Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	80	-	85	-	100	-	ns
Address Valid to End of Write	t_{AW}	80	-	85	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	60	-	70	-	90	-	ns
Write Recovery Time ($\overline{WE}$, $\overline{CS1}$)	t_{WR1}	5	-	5	-	10	-	ns
Write Recovery Time (CS2)	t_{WR2}	15	-	15	-	15	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns

Write Cycle No.1 Timing Waveform: $\overline{OE}$ Clock



Write Cycle No.2 Timing Waveform: $\overline{OE}$ Low



AC Characteristics Notes :

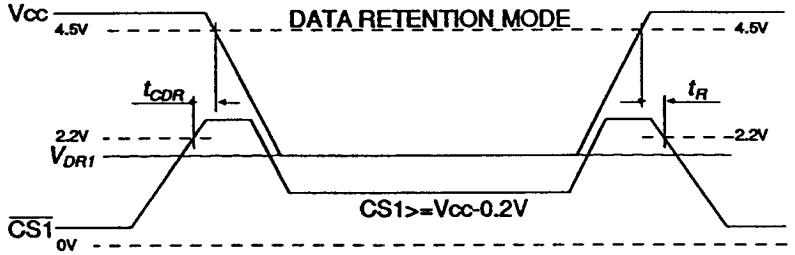
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
   t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
   t_{WR2} applies in case a write ends at $\overline{CS2}$ going low.
5. During this period, I/O pins are in the output state, therefore input signals of opposite phase to the outputs must not be applied.
6. If CS1 goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is in the same phase as written data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

Low V_{CC} Data Retention Characteristics - L Version Only (1) (T_A=-55 to +125°C)

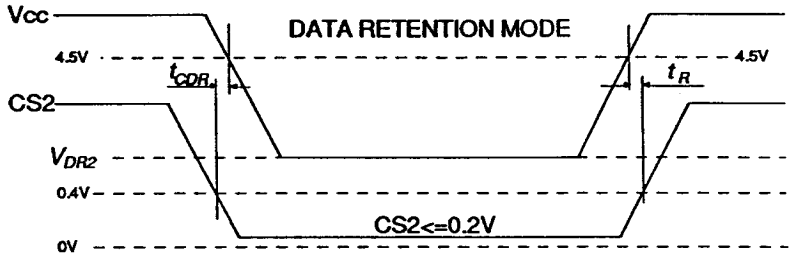
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1}$,CS2≥V_{CC}-0.2V or CS2≤0.2V	2.0	-	-	V
	V_{DR2}	CS2≤.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V,$\overline{CS1}$≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V	-	-	200(2)	µA
	I_{CCDR2}	V_{CC}=3.0V,CS2≤0.2V				
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}(3)	-	-	ns

Notes: (1) In Data Retention Mode,CS2 controls the Address,$\overline{WE}$,$\overline{CS1}$,$\overline{OE}$ and Din buffer.If CS2 controls data retention mode,Vin for these inputs can be in the high impedance state.If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2≥=Vcc-0.2V or CS2≤=0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
(2) For t_A=0 to +70°C, $I_{CCDR1,2}$=1.0µA(typ),50µA(max)
(3) t_{RC} =Read Cycle Time

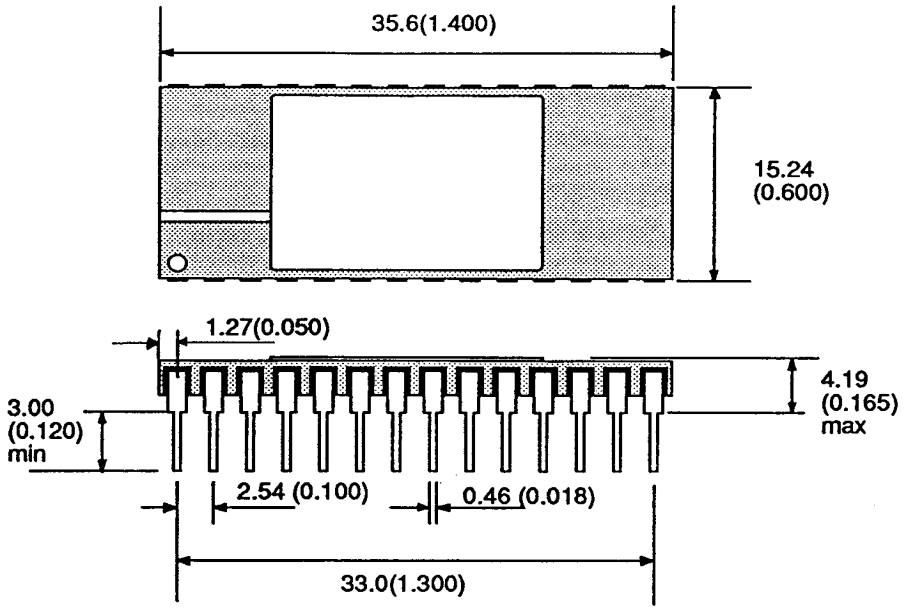
Low V_{CC} Data Retention Timing Waveform 1 (CS! controlled)



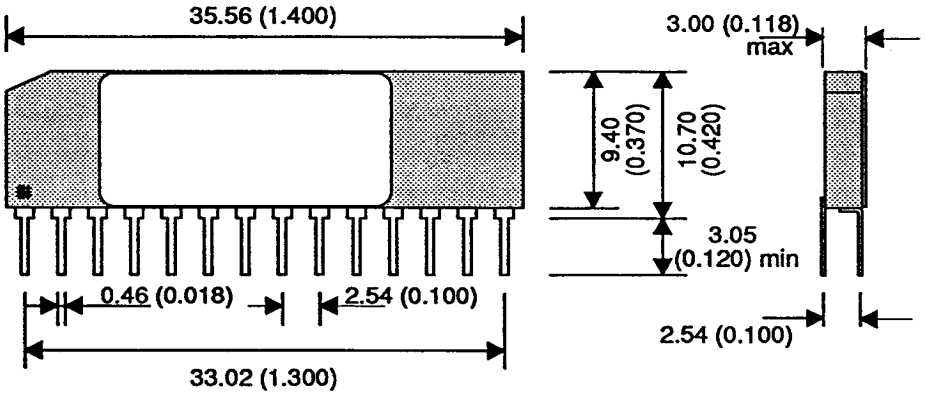
Low V_{CC} Data Retention Timing Waveform 1 (CS2 controlled)



28 Pin 0.6" Dual-In-Line (DIL) - 'S' Package

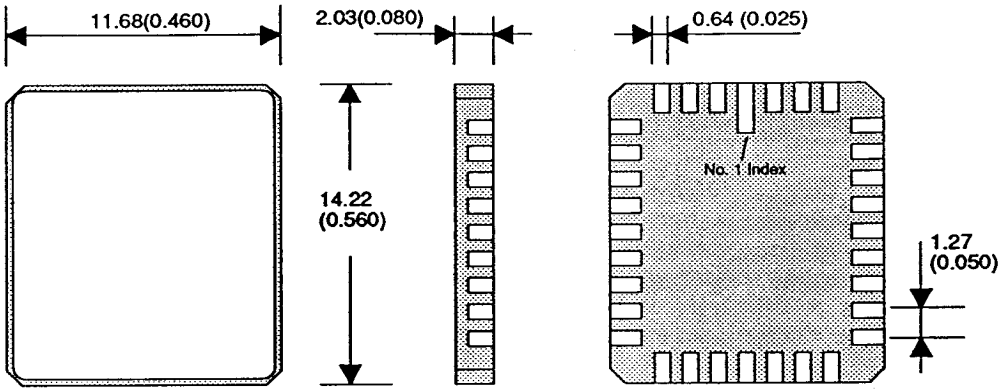


28 Pin 0.1" Vertical-In-Line (VIL ™) 'V' Package



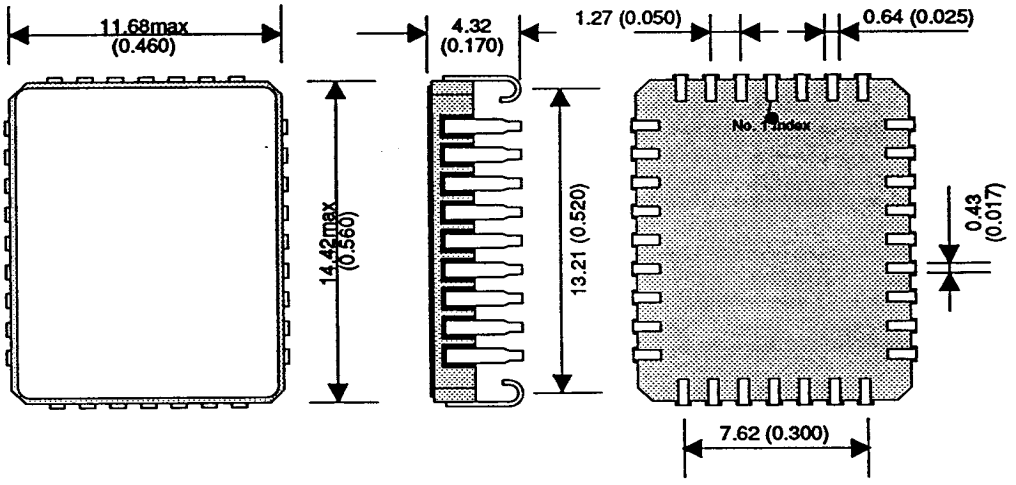
Dimensions in mm (inches)

32 Pad Leadless Chip Carrier (LCC) - 'W' Package



Dimensions in mm (inches)

32 Pin 'J' Leaded Chip Carrier (JLCC) - 'J' Package



Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW		
SCREEN	*TEST METHOD (Per MIL 883C)*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ 150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to 150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at Ta=+25°C	100%
Burn-in	Method 1015,Condition D,Ta=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable(PDA)	Calculated at post-burn-in at Ta=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM88SLM-10

Speed	10	= 100 ns
	12	= 120 ns
	15	= 150 ns
Temp. Range/screening	Blank	= Commercial
	I	= Industrial
	M	= Military
	MB	= Processed to MIL STD 883C
Power Consumption	Blank	= Standard Power
	L	= Low Power
Package	S	= 28 Pin .6" Ceramic DIP
	V	= 28 Pin .1" Ceramic VIL
	W	= 32 Pad Ceramic LCC
	J	= 32 Pin Ceramic JLCC

mosaic
Mosaic Semiconductor Inc.
7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058