

PREAMPLIFIER WITH ALC FOR C, O₂ CASSETTE RECORDERS

- EXCELLENT VERSATILITY IN USE (V_S from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- STEREO MATCHING BETTER THAN 3 dB (matched pair)

The TDA 2054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:

- low noise preamplifier
- automatic level control system (ALC)
- high gain equalization amplifier

It is intended as preamplifier in tape and cassette recorders and players (C, O₂), dictaphones, compressor and expander in telephonic equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

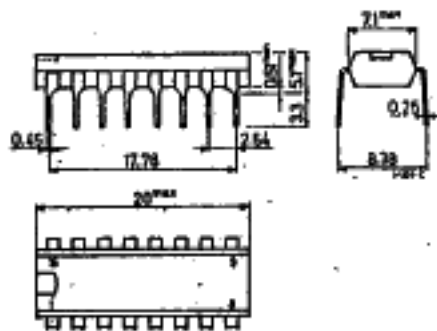
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	20	V
P_{tot}	Total power dissipation at $T_{amb} = 50^\circ\text{C}$	500	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

ORDERING NUMBERS: TDA 2054M mono applications
2 TDA 2054M stereo applications

MECHANICAL DATA

Dimensions in mm



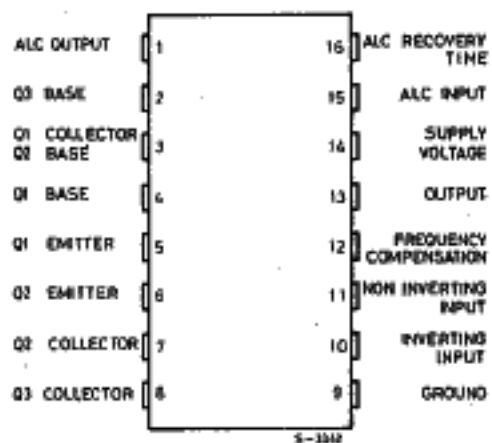
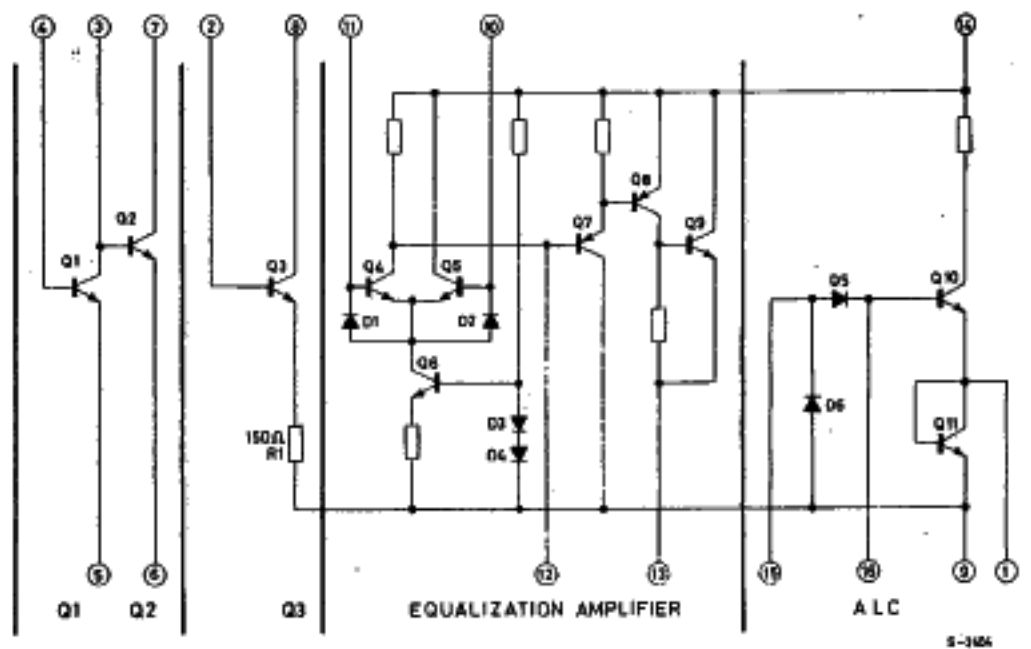
CONNECTION DIAGRAM

SCHEMATIC DIAGRAM


Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (transistors Q1, Q2, Q3)

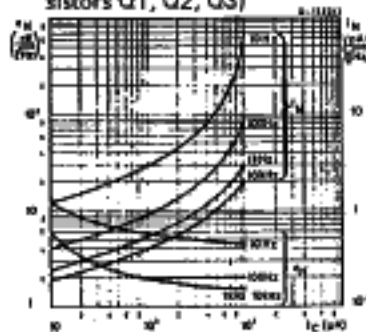


Fig. 2 - Equivalent input noise current vs. frequency (transistors Q1, Q2, Q3)

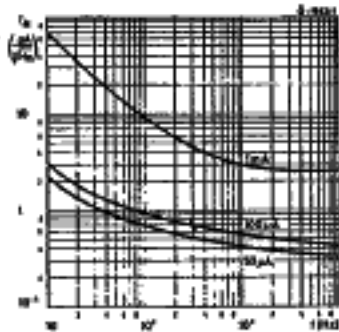


Fig. 3 - Equivalent input noise voltage vs. frequency (transistors Q1, Q2, Q3)

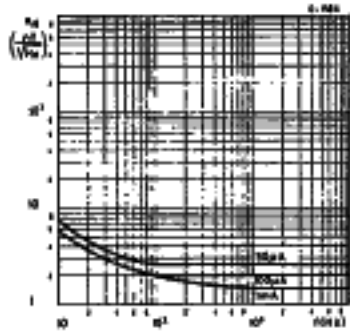


Fig. 4 - Noise figure vs. bias current (transistors Q1, Q2, Q3)

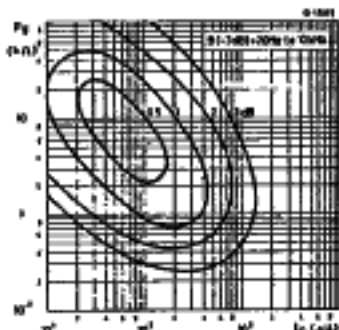


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (transistors Q1, Q2, Q3)

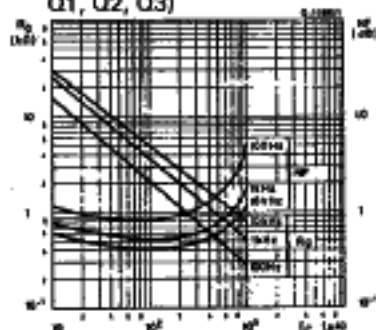


Fig. 6 - Current gain vs. collector current (transistors Q1, Q2, Q3)

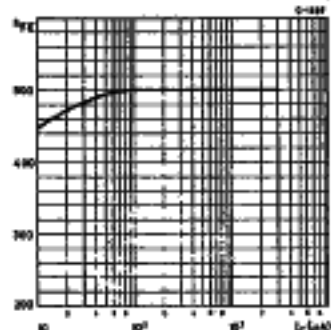


Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

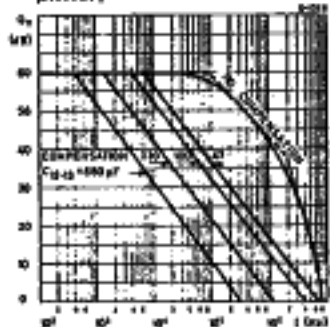


Fig. 8 - Open loop phase response vs. frequency (equalization amplifier)

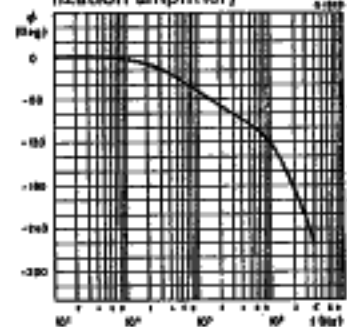
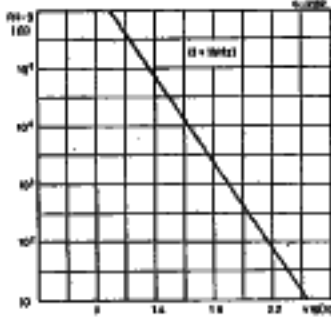


Fig. 9 - Dynamic resistance R₁₋₉ vs. ALC voltage V₁₆



APPLICATION INFORMATION

Fig. 9 - Application circuit for C₉O₂ cassette player and recorder

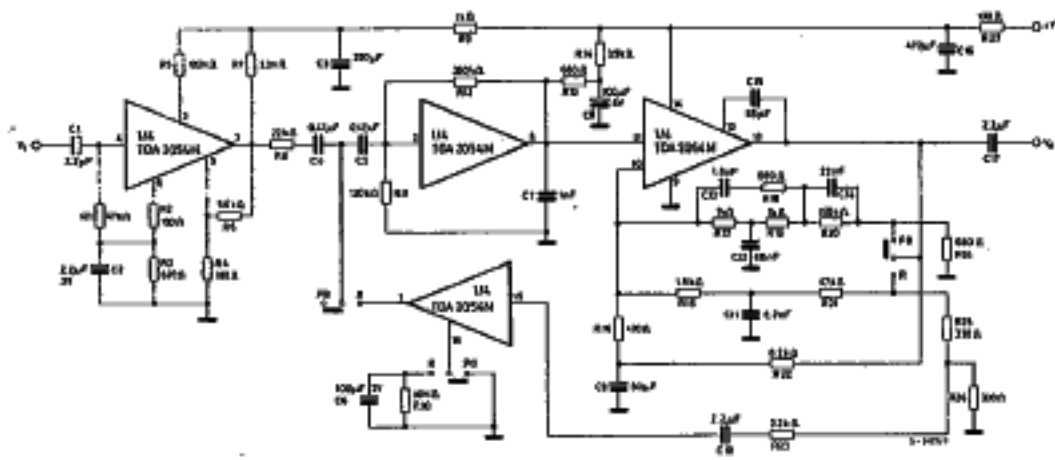
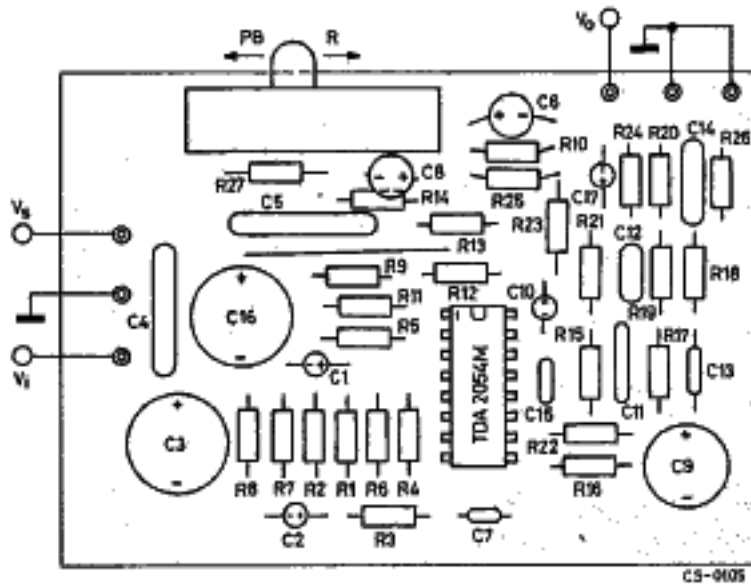


Fig. 10 - P.C. board and component layout for the circuit of Fig. 9 (1:1 scale)



TYPICAL PERFORMANCE OF CIRCUIT IN FIG. 9 ($T_{amb} = 25^{\circ}\text{C}$, $V_s = 9\text{V}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK					
G_v	Voltage gain (open loop)	$f = 20$ to 20000 Hz	134		dB
G_v	Voltage gain (closed loop)	$f = 1$ KHz	60		dB
Z_i	Input impedance	$f = 100$ Hz	10		K Ω
		$f = 1$ KHz	41		K Ω
		$f = 10$ KHz	43		K Ω
Z_o	Output impedance	$f = 1$ KHz	12	35	Ω
B	Frequency response		see fig. 11		
d	Distortion	$V_o = 1\text{V}$ $f = 1$ KHz	0.2		%
	Output background noise	$Z_g = 300\Omega + 120$ mH (DIN 45405)	1.5		mV
***	Output weighted background noise		1		mV
$\frac{S+N}{N}$	Signal to noise ratio	$V_o = 1.5\text{V}$ $Z_g = 300\Omega + 120$ mH	60		dB
t_{on}^*	Switch-on time	$V_o = 1\text{V}$	500		ms

RECORDING

G_v	Voltage gain (open loop)	$f = 20$ to 20000 Hz	134		dB
G_v	Voltage gain (closed loop)	$f = 1$ KHz	72		dB
B	Frequency response		see fig. 13		
d	Distortion with ALC	$V_o = 1\text{V}$ $f = 10$ KHz	0.5		%
ALC	Automatic level control range (for 3 dB of output voltage variation)	$V_i < 40$ mV $f = 10$ KHz	54		dB
V_o	Output voltage before clipping without ALC	$f = 1$ KHz	3		V
V_o	Output voltage with ALC	$V_i = 30$ mV $f = 1$ KHz	1.1		V
t_l^*	Limiting time (see fig. 17)	$\Delta V_i = +40$ dB $f = 1$ KHz	75		ms
t_{set}^*	Level setting time (see fig. 17)		300		ms
t_{rec}^*	Recovery time (see fig. 17)	$\Delta V_i = -40$ dB $f = 1$ KHz	150		sec.
t_{on}^*	Switch-on-time	$V_o = 1\text{V}$	500		ms
$\frac{S+N}{N}^{***}$	Signal to noise ratio with ALC	$V_o = 1\text{V}$ $R_g = 470\Omega$	64		dB

* This value depends on external network.

** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 15 KHz can be avoided - so halving the output noise.

*** Weighted noise measurement (DIN 45406).

Fig. 11 - Frequency response for the circuit in fig. 9 (playback)

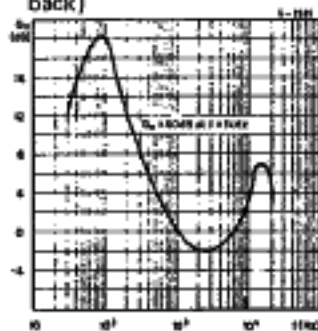


Fig. 12 - Distortion vs. frequency for the circuit in fig. 9 (playback)

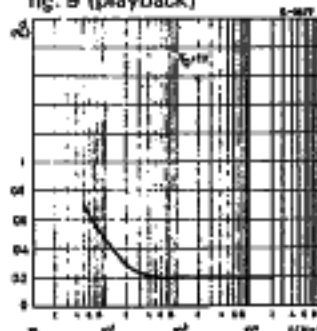


Fig. 13 - Frequency response for the circuit in fig. 9 (recording)

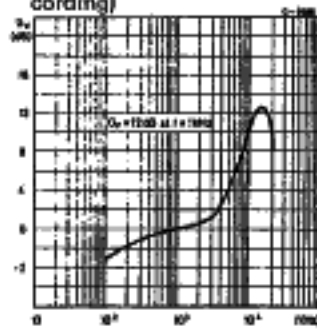


Fig. 14 - Output voltage variation with ALC vs. input voltage for the circuit in fig. 9 (recording)

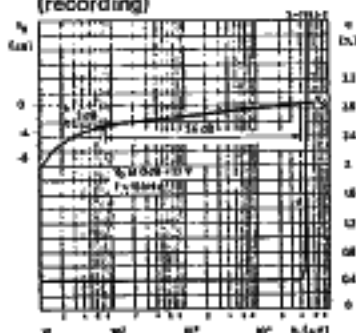


Fig. 15 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

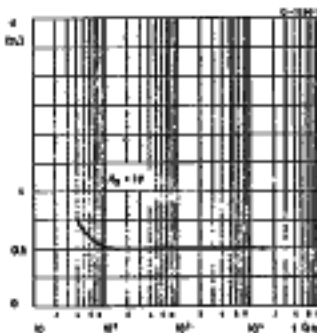


Fig. 16 - Limiting and level setting time vs. input signal variation

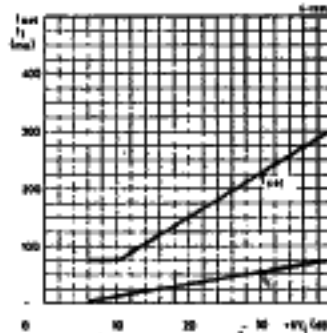


Fig. 17 - Limiting, level setting, recovery time

