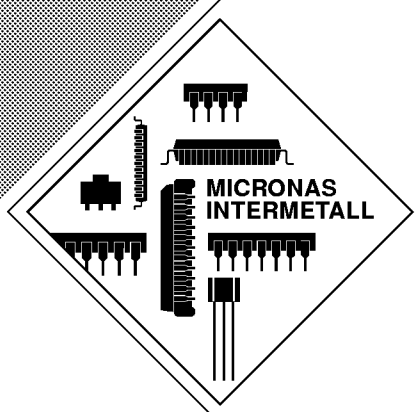


ASC 3553O
Audio Stereo Codec

Edition Aug. 5, 1998
6251-333-3DS

MICRONAS
INTERMETALL

Contents

Audio Stereo Codec

Release Notes:

The hardware description in this document is valid for the ASC 3553O technical code 19 (TC19) and following codes.

The present document is the third release of the final data sheet. Revision bars indicate significant changes to the previous version.

Note: If not otherwise designated, the pin numbers mentioned refer to the 44-pin PLCC package.

1. Introduction

This CMOS circuit presents a high quality two-channel A/D and D/A converter for modern digital signal processing systems such as: sound processing in multimedia workstations, speech synthesis and voice recognition, high performance modems, compact disk players, DAT players and recorders. The ASC 3553O has a programmable conversion rate of 8 kHz to 48 kHz. The resolution is 16 bit and exhibits audio quality with more than 90 dB S/N (@ 24 kHz) and 0.03% THD from A/D input to D/A output.

The codec comes with a new serial port protocol which can carry up to 4 stereo channels of 16-, 18-, or 20-bit sound data and additional auxiliary information (see Fig. 1–1) . This interface is compatible to most standard DSP serial ports. Also supported are I^2S compatible formats for interfacing standard sound ICs. The ASC 3553O contains all interface logic to fit the DSP ICs directly.

The ASC 3553O is designed in CMOS technology and is housed in a 44-pin PLCC package. The major blocks are shown in Fig. 2–1.

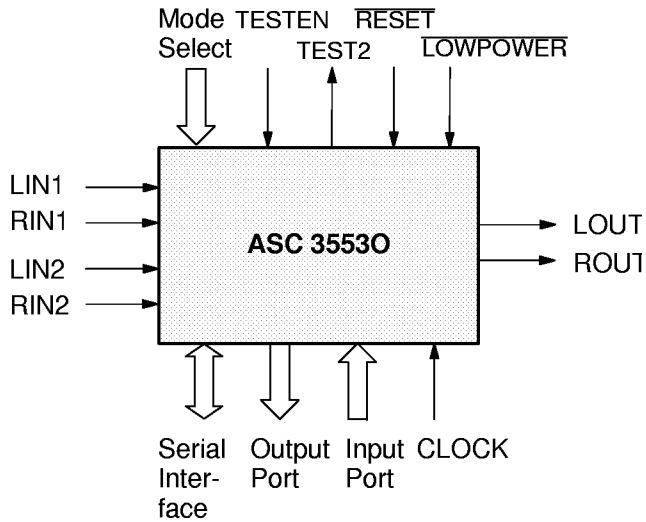


Fig. 1–1: ASC 3553O block diagram

2. Functional Description

The major features of the ASC 3553O are

- complete high performance dual channel audio ADC and DAC
- includes all necessary filters, no external filters required
- analog input multiplexer with programmable gain
- dual channel oversampling ADC
- digital decimation filters (linear phase FIR)
- digital eightfold interpolation filters (linear phase FIR)
- dual channel oversampling DAC
- variable output attenuation and mute
- automatic sampling rate detection
- programmable serial interface port
- digital I/O port
- AD conversion with typical SNR figures of 92 dB (@ 24 kHz sampling rate)
- DA conversion with typical SNR figures of 94 dB
- +5 V single supply voltage
- less than 250 mW typical power dissipation
- low power mode (typical 0.38 mW)

2.1. Analog Input Multiplexer

Two 2 to 1 input multiplexers are included on-chip, giving two analog inputs per channel. The selection of the input is controlled by the serial port.

2.2. Analog Input Gain

The input gain ranges from 0 dB to 22.5 dB adjustable in 1.5 dB steps (see Table 3–2). The gain setting is controlled by the serial port.

2.3. Analog Output Attenuation

The analog output attenuation of the audio codec provides 22.5 dB control range. It is controlled by the serial port and can be adjusted in steps of 1.5 dB (see Table 3–3).

2.4. Output Mute

The output of the audio codec can be silenced by switching the output stage to mute position. This is controlled by the serial port. Muting is done by setting the output attenuation to maximum (about –80 dB). To mute without audible clicks, it is recommended first to ramp up the analog output attenuation and to output digital zeros.

2.5. Digital I/O Port

The audio codec is equipped with 4 digital input and 4 digital output pins. The output pins can be used to control output devices. The level on the output pins can be set, the level of the input pins can be read by the serial port.

2.6. Valid Data Indicator

The valid data indicator is used to monitor the A/D data stream. It reports an invalid data condition after reset, mute or low-power operation until enough clocks have passed for the full latency of the digital filters.

2.7. Automatic Sampling Rate Detection

The codec has three timing inputs that control the internal operation. This is the master clock (CLOCK, 24.576 MHz typically), the serial clock SCLOCK, which is set externally to a value 1/n of the master clock and the serial synchronization signal SSYNC. The SSYNC signal is always identical to the sampling rate. It defines a frame structure on the serial data which spans 32, 64 or 256 data bits. The codec senses the ratio between the master clock and the serial sync and adjusts automatically to the desired sampling rate. The serial clock is further checked to be compatible to the selected frame. Table 2–1 lists allowed sampling rates and corresponding CLOCK to SCLOCK ratios.

If the sampling rate of the serial port drops below the specified minimum, an error is reported and the output muted. The serial data out of the codec indicate invalid data and error code 3. The digital input and output ports remain active.

Note: Switching from one master clock input to another requires the ASCO to be reset.

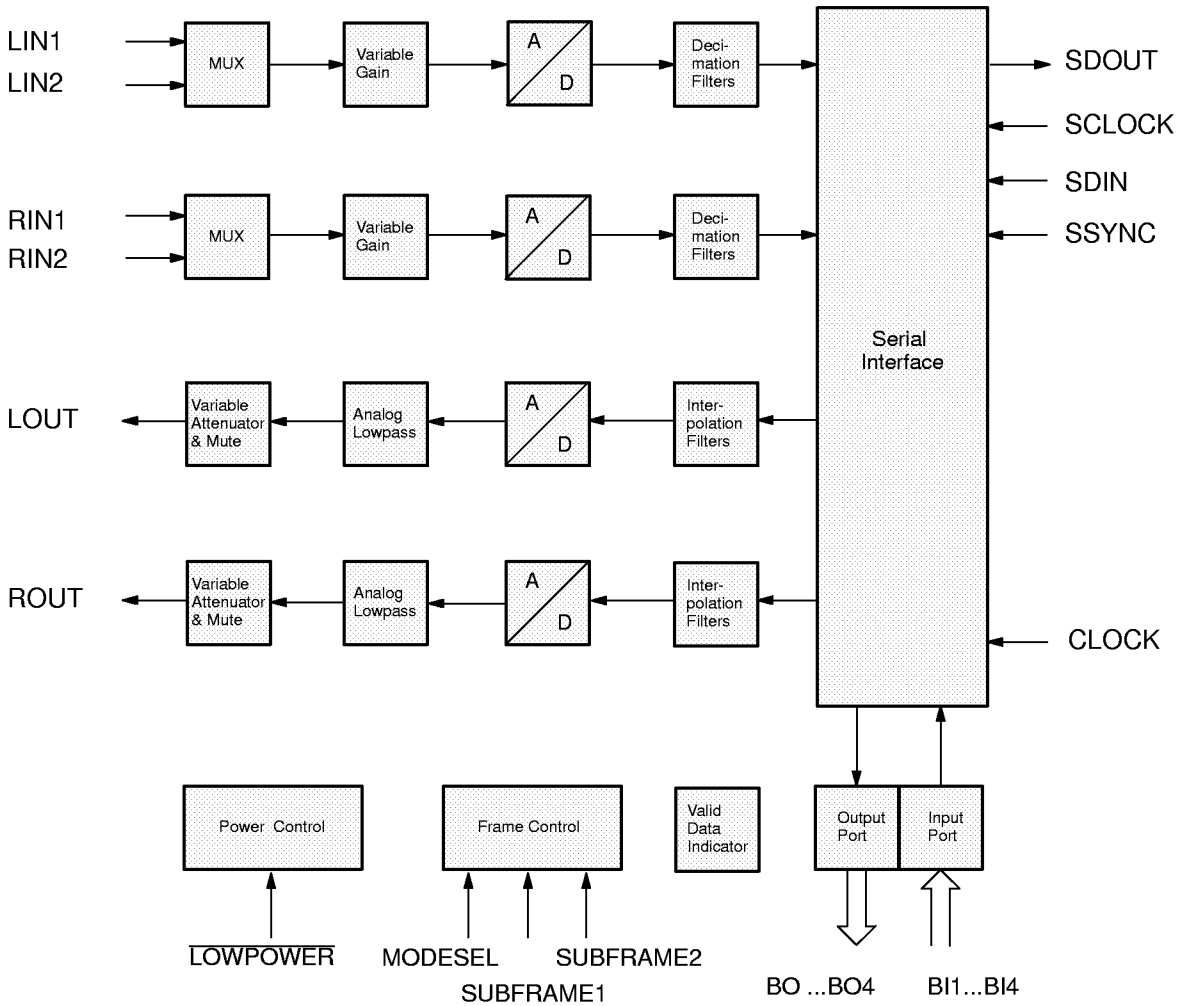


Fig. 2–1: Major blocks of ASC 3553O

2.8. Other Sampling Rates

Further sample rates of interest are 7.2 kHz and 44.1 kHz. In both of these cases, the master clock has to be changed to 22.1184 and 22.5792 MHz respectively and using the “8 kHz” setting in the first case, “48 kHz” in the latter.

2.9. A/D Converters PDM

The A/D converters are realized as pulse density modulators (PDM) running at a clock frequency of 6.144 MHz. The two A/Ds are high quality PDMs with one external capacitor (PDMCR and PDMCL). The output signals are 1 bit data streams of 6.144 MHz. Due to the high sampling rate of the pulse density modulators no expensive antialiasing filters are needed.

2.10. Digital Decimation Filters

After analog to digital conversion, the input signals are filtered by means of digital filters in order to decimate the high frequency PDM signals to an appropriate sampling rate. The second purpose of these filters is to suppress unwanted out-of-band signals. The individual filter blocks can be seen in Fig. 2–2.

The filters are designed as multirate FIR blocks. The decimation process is subdivided into 3 parts. The first part (LPF1) serves for the variable decimation from the fixed PDM rate (6.144 MHz) to the eightfold sampling rate. This filter block is implemented as a third order moving time averager (MTA). Further decimation is done by an 24 tap linear phase FIR filter (LPF2). Outgoing samples with two times the sampling rate are converted to the final sampling rate by the 82 tap LPF3 filter. Filters LPF2 and LPF3 are realized by the programmable filter processor DFP.

2.11. Digital Interpolation Filters

In order to suppress out of band signals, the audio codec is equipped with digital interpolation filters. These filters attenuate alias frequencies up to eight times the sampling frequency. The interpolation block consists of three linear phase FIR filters in cascade (see Fig. 2–1). The first one (INT1) serves for interpolation to two times the sampling rate. It consists of 82 taps. This is followed by the 24 tap filter INT2 which performs interpolation up to 8 times the sampling rate. A sample and hold filter serves for the interpolation to the operating rate of the D/A converter. Filters INT1 and INT2 are programmed within the DFP filter software.

2.12. D/A Converters DAC

The digital samples coming out of the DFP digital filter processor are oversampled to a high sampling rate where noise shaping is performed (Table 2–2). The output of the noise shaper is then converted using a highly linear 5 bit D/A converter. It’s noise power density increases with increasing frequency, the residual noise in the baseband is very low. Following the D/A conversion process, the high frequency noise is suppressed by means of built-in analog lowpass filters.

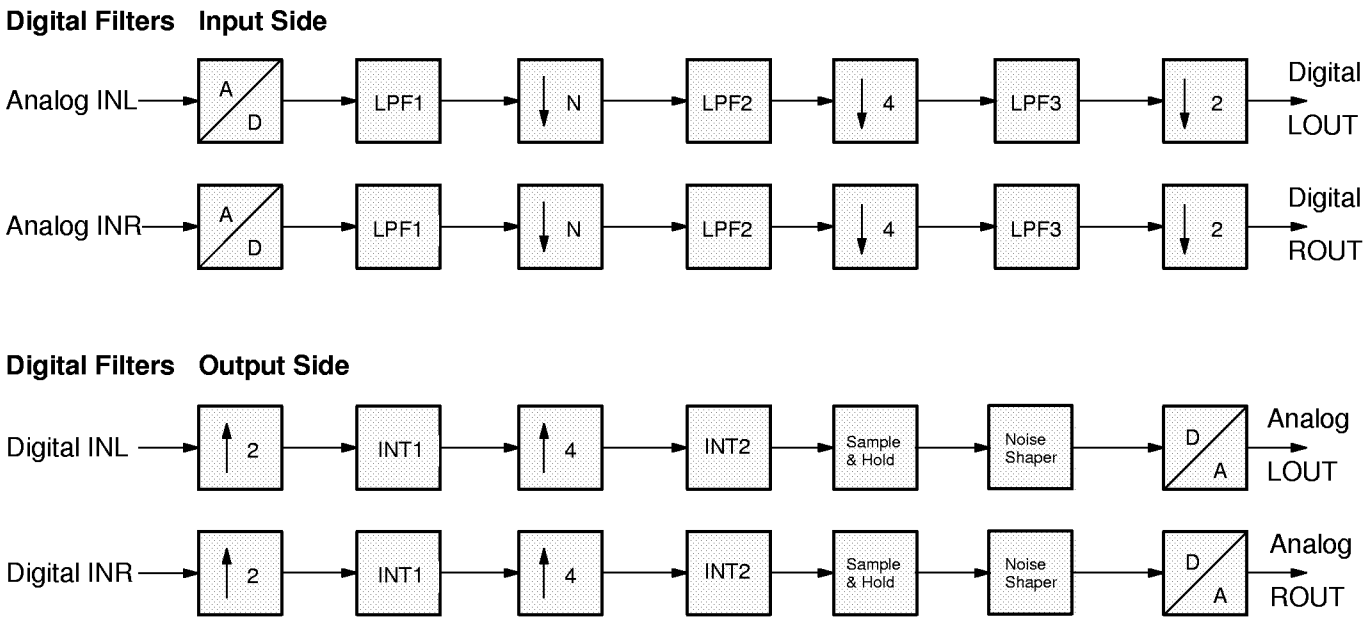


Fig. 2–2: Digital filter sections

2.13. Digital Filter Processor DFP

The Digital Filter Processor DFP is a simple but powerful DSP building block. Its main use is to perform the major part of the required digital filtering. The DFP library cell runs with a maximum clock frequency of 25 MHz. This enables the computation of 25 million multiplications and additions per second.

2.14. Power Control

2.14.1. Low Power Mode

By means of the $\overline{\text{LOWPOWER}}$ pin, the IC can be switched into a low power mode. In this mode, the IC typically consumes 75 µA. All analog output pins are switched to the analog common mode voltage (AGNDC). This is done to minimize clicks on the analog outputs. All digital output pins are switched to high impedance. Going from power off to low power or normal power, the capacitor connected to AGNDC will be charged by an internal resistor (125 kΩ). During this charging time, the given specification figures are not valid. To minimize power consumption, all digital inputs should match either GND or VSUP level as closely as possible, otherwise a small current will flow in the digital input stages. For correct operation, the analog outputs should be AC coupled. With DC coupling, a current may flow caused by the analog common mode voltage of about 2.25 V.

In order to reduce clicks on the analog outputs, the following procedure is recommended:

– Normal Operation to Low Power:
  1. Analog Attenuation to maximum (22.5 dB)
  2. Set digital sound data to zero
  3. Set mute bit in serial data stream and wait for completion of one serial frame
  4. Set $\overline{\text{LOWPOWER}}$ = low
  5. To minimize power consumption, switch CLOCK, SCLOCK, SSYNC, and SDIN to GND. All digital inputs should match either GND or VSUP level as closely as possible.

– Low Power to Normal Operation:
  1. CLOCK, SCLOCK, SSYNC, and SDIN active
  2. Set $\overline{\text{LOWPOWER}}$ = high
  3. Unmute Output

– Power Off to Low Power:
  1. Power on, $\overline{\text{RESET}}$, $\overline{\text{LOWPOWER}}$ remain low
  2. To minimize power consumption, switch CLOCK, SCLOCK, SSYNC, and SDIN to GND. All digital inputs should match either GND or VSUP level as closely as possible.

– Power Off to Normal Operation:
  1. Power on, $\overline{\text{RESET}}$, $\overline{\text{LOWPOWER}}$ remain low
  2. CLOCK, SCLOCK, SSYNC, and SDIN active
  3. Set $\overline{\text{LOWPOWER}}$ = high
  4. Wait for at least 10 µs
  5. Set $\overline{\text{RESET}}$ = high
  6. 1 s after power on analog performance is within specification

2.14.2. Zero Power Mode

The power consumption can be reduced to absolute minimum by switching the codec into Zero Power Mode. This is done by pulling $\overline{\text{LOWPOWER}}$ to low and TESTEN to high. In this mode, even the analog circuitry is switched off. The analog output pins will no longer be driven to the AGNDC level but will be high impedance. All digital output pins are switched to high impedance as well. To minimize power consumption, all digital inputs should match either GND or VSUP level as closely as possible.

2.15. Reference Output

Input and outputs are usually AC coupled (see application notes). For DC coupling, a voltage reference pin BAGNDI is included on the codec. Its 2.25 V stabilized very low impedance output can be used for biasing external opamps.

Table 2–1: Audio codec CLOCK to SCLOCK ratios

Sampling Rate f_S kHz	256 Bit Frame[1)]	64 Bit Frame[1)]	32 Bit Frame[1)]
48	2	8	16
32	3	12	24
24	4	16	32
19.2	5	20	40
16	6	24	48
12	8	32	64
9.6	10	40	80
8	12	48	96

1) F_{CLOCK}/F_{SCLOCK}

Table 2–2: Audio codec operation modes, interpolation and D/A conversion ratio

Sampling Rate f_S kHz	Interpolation Rate kHz	D/A Conversion Rate kHz
48	384	1536
32	256	
24	192	
19.2	153.6	
16	128	
12	96	
9.6	76.8	
8	64	

3. Serial Port Specification

The codec receives its data (audio and control) via the serial interface. There is one line for input and one for output. Data input and output takes place at the same time with a timing defined by the serial clock and serial sync signal.

3.1. Full Feature Format – 256 Bit Format

The serial port has four signal lines. The protocol is based on frames of four 64-bit subframes. A subframe contains two 20-bit sound values plus a 24-bit auxiliary field. The sound data is formatted MSB first, with trailing zeroes if the full resolution is not available. A diagram of this format is shown in Fig. 3–1. Note that time is assumed to move from left to right in the diagram.

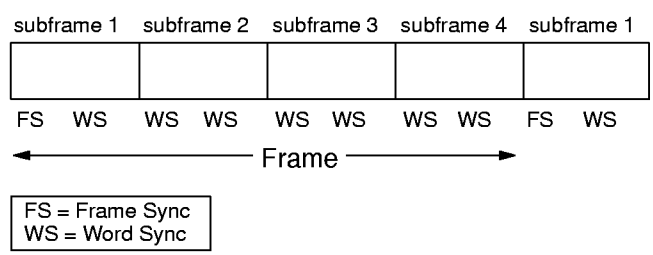


Fig. 3–1: Diagram of a single frame with four subframes

A subframe consists of two words which forms a stereo pair. Since each word start is indicated by a WS, there is actually a word sync in the middle of a subframe, as well as the one at the beginning. Note that a Frame Sync is also a Word Sync. A diagram of a subframe is shown in Fig. 3–2.

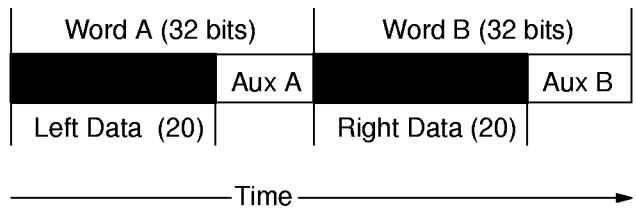
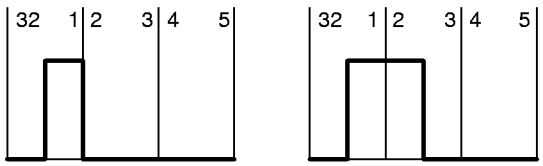


Fig. 3–2: Diagram showing a single stereo

The combination of Aux A and Aux B form the 24-bit auxiliary datum for the subframe. Each subframe has its own auxiliary data. The serial data is carried on four digital lines, defined as follows:

– SCLOCK: Serial clock; INPUT TO CODEC. The negative transition indicates data change, the positive edge is the sampling edge. The serial clock always runs at 256 x the sample rate.

– SSYNC: Serial data sync; INPUT TO CODEC. This signals is used to indicate the start of a word or a frame. Note that a frame start is also a word start. The line is normally low, and goes high for two bit cells at the beginning of a frame, or one bit cell at the beginning of a word other than the first word in a frame. A diagram of each type of sync pulse is shown in Fig. 3–3.



a) b)

Fig. 3–3: a) Word Sync b) Frame Sync

The numbers shown are word bitcells. Cell 1 is always MSB of the sound data in this format, and bit 32 is the last bit of the auxiliary data. The codec produces an error code if any other format sync is detected, and automatically mutes the output.

Note: The current implementation supplies a more flexible Frame Sync format: The sync detection circuit is triggered by a low to two times high condition on the serial sync line SSYNC, e.g. the more common 50 % duty cycle sync is also accepted. Word Syncs are not needed for correct operation. With missing Word Syncs, word boundaries are extracted by means of internal counters that are synchronized by Frame Syncs.

– SDIN: Serial D/A data in; INPUT TO CODEC: The codec only responds to the selected subframe, and ignores data in other subframes. Each 64-bit subframe (two words) has the following internal structure:

Word A:
subframe cells 1...20 for Left D/A data
subframe cells 21...32 for Auxiliary Control A data

Word B:
subframe cells 33...52 for Right D/A data
subframe cells 53...64 for Auxiliary Control B data

The Auxiliary Control A and B data is concatenated to produce a 24-bit field (Fig. 3–4). These bits are used to specify control for the codec. This field is encoded as follows:

Aux cell 1 (subframe cell 21): Expand bit. Must be zero for now. If it is 1, an error is generated (Error code 1, see SDIN aux specification). This bit will be utilized for an expanded command set in the future. NOTE: If this bit is detected, all other aux control cells are ignored. The error bits generated in the status aux bits and audio processing continue as usual.

Aux cell 2 (subframe cell 22): Mute. Value of 1 causes a mute of the D/A output. Value of 0 for normal output. This bit also acts as a “reset”condition on the A/D valid counter. This allows mute to be used when changing sample rates.

Aux cells 3, 4 (subframe cells 23, 24): Input Select. Aux cell 3 controls the 2-to-1 input mux for the left channel, and cell 4 controls the mux for the right channel (value 0 for input 1, value 1 for input 2).

Aux cells 5 to 8 (subframe cells 25 to 28): Left Input Gain. Sets the gain value of the A/D input from 0 to 22.5 dB in 1.5 dB steps. Hex 0 = 0 dB gain, hex F = 22.5 dB gain. Bits are shipped MSB first.

Aux cells 9 to 12 (subframe cells 29 to 32): Right Input Gain. Sets the gain value of the A/D input from 0 to 22.5 dB in 1.5 dB steps. Hex 0 = 0 dB gain, hex F = 22.5 dB gain. Bits are shipped MSB first.

Aux cells 13 to 16 (subframe cells 53 to 56): Left D/A Output Attenuation. Sets the attenuation value for D/A output from 0 to 22.5 dB in 1.5 dB steps. Hex 0 = no attenuation, hex F = 22.5 dB attenuation. Bits are shipped MSB first.

Aux cells 17 to 20 (subframe cells 57 to 60): Right D/A Output Attenuation. Sets the attenuation value for D/A output from 0 to 22.5 dB in 1.5 dB steps. Hex 0 = no attenuation, hex F = 22.5 dB attenuation. Bits are shipped MSB first.

Aux cells 21 to 24 (subframe cells 61 to 64): Output Control. Controls four digital output pins on the codec (BO1 to BO4). A digital value of 1 gives a high output, and a digital value of 0 gives a low output. Aux cell 21 corresponds to BO1, aux cell 24 to BO4. NOTE: after power-up sequence, these four bits are initialized to zero. Data change occurs at the first negative transition of the SCLOCK within a frame.

– SDOUT: Serial A/D data out; OUTPUT (TRI-STATE) FROM CODEC. The codec only drives the SDOUT line during the subframe that it is assigned to, and tri-states SDOUT during other subframes. Each 64-bit subframe (two words) has the following internal structure:

Word A:
subframe cells 1...20 for Left A/D data
subframe cells 21...32 for Auxiliary Status data “A”

Word B:
subframe cells 33...52 for Right A/D data
subframe cells 53...64 for Auxiliary Status data “B”

The Auxiliary Status A and B data are concatenated to produce a 24-bit field for status from the codec (Fig. 3–4). This field is encoded as follows:

Aux cell 1 (subframe cell 21): Expand bit. Must be zero now. Used for expansion later.

Aux cell 2 (subframe cell 22): A/D Valid Data. Value of 1 indicates valid A/D data. Value of 0 for invalid data. This is used to indicate that the A/D has completed initialization following power up, low power mode, or mute condition, and is generating accurate data.

Aux cells 3, 4 (subframe cells 23, 24): A/D Overflow status (bit 3 for left, 4 for right). Indicates that clipping is occurring in the A/D conversion and filtering process.

Aux cells 5 to 8 (subframe cells 25 to 28): Error Number. Field should be zero unless an error condition exists. Bits are shipped MSB first. Error conditions are:

1. SDIN auxiliary bit 1 is set. Error code = 0001 (unable to understand control word. Data is still assumed to be valid.

2. Detection of an Alternate Format Sync pulse. Error code = 0010 (unable to understand data format). This automatically causes a mute of the analog output.

3. Serial clock frequency out of allowable range. Error code = 0011 (serial clock out of range). This automatically causes a mute of the analog output.

Other error codes will be assigned in the future.

Aux cells 9 to 12 (subframe cells 29 to 32): Revision Number. Set to 0000 for this part.

Aux cells 13 to 16 (subframe cells 53 to 56): Not used. Reserved for future use. Should be 0000.

Aux cells 17 to 20 (subframe cells 57 to 60): Not used. Reserved for future use. Should be 0000.

Aux cells 21 to 24 (subframe cells 61 to 64): Input Sense. Carries values from four (digital) input pins on the codec. A high voltage produces a digital value of 1, and a low voltage produces a digital value of 0. The inputs are sampled at the last positive transition of the SCLOCK within a frame. Aux cell 21 corresponds to BI1, aux cell 24 to BI4.

Auxiliary Control Field Input

1	2	3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24
Expand Bit	Mute	Input Mux Left / Right	Left Input Gain	Right Input Gain	Left Output Attenuation	Right Output Attenuation	Output Port
Aux Data “A”					Aux Data “B”		

Auxiliary Control Field Output

1	2	3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24
Expand Bit	Valid Data	Overflow Left / Right	Status	Revision Number	Reserved ‘0000’	Reserved ‘0000’	Input Port
Aux Data “A”					Aux Data “B”		

Fig. 3–4: Auxiliary field layout

Table 3–1: Definition of Subframe Bit Cells

Serial Bit Cell Number	Input Data to Stereo Codec	Output Data from Stereo Codec
1.	Left D/A Data Bit 19 (MSB)	Left A/D Data Bit 19 (MSB)
20.	Left D/A Data Bit 1 (LSB)	Left A/D Data Bit 1 (LSB)
21.	Expand Bit	Extend Bit
22.	Mute	A/D data valid
23.	Left A/D Input Select	Left A/D Clipping
24.	Right A/D Input Select	Right A/D Clipping
25.	Left A/D Input Gain Bit 3 (MSB)	Error Number Bit 3 (MSB)
28.	Left A/D Input Gain Bit 0 (LSB)	Error Number Bit 0 (LSB)
29.	Right A/D Input Gain Bit 3 (MSB)	Revision Number Bit 3 (MSB)
32.	Right A/D Input Gain Bit 0 (LSB)	Revision Number Bit 0 (LSB)
33.	Right D/A Data Bit 19 (MSB)	Right A/D Data Bit 19 (MSB)
52.	Right D/A Data Bit 1 (LSB)	Right A/D Data Bit 1 (LSB)
53.	Left D/A Output Attenuation Bit 3 (MSB)	reserved
56.	Left D/A Output Attenuation Bit 0 (LSB)	reserved
57.	Right D/A Output Attenuation Bit 3 (MSB)	reserved
60.	Right D/A Output Attenuation Bit 0 (LSB)	reserved
61.	Digital Output Port Data (BO1)	Digital Input Port Data (BI1)
64.	Digital Output Port Data (BO4)	Digital Input Port Data (BI4)

Table 3–2: Definition of Aux cells 5 to 8 (Left Input Gain) and 9 to 12 (Right Input Gain)

Programmed Value	Gain dB	Programmed Value	Gain dB
0_{hex}	0.0	8_{hex}	+ 12.0
1_{hex}	+ 1.5	9_{hex}	+ 13.5
2_{hex}	+ 3.0	A_{hex}	+ 15.0
3_{hex}	+ 4.5	B_{hex}	+ 16.5
4_{hex}	+ 6.0	C_{hex}	+ 18.0
5_{hex}	+ 7.5	D_{hex}	+ 19.5
6_{hex}	+ 9.0	E_{hex}	+ 21.0
7_{hex}	+ 10.5	F_{hex}	+ 22.5

Table 3–3: Definition of Aux cells 13 to 16 (Left D/A output attenuation) and 17 to 20 (Right D/A output attenuation)

Programmed Value	Gain dB	Programmed Value	Gain dB
0_{hex}	0.0	8_{hex}	– 12.0
1_{hex}	– 1.5	9_{hex}	– 13.5
2_{hex}	– 3.0	A_{hex}	– 15.0
3_{hex}	– 4.5	B_{hex}	– 16.5
4_{hex}	– 6.0	C_{hex}	– 18.0
5_{hex}	– 7.5	D_{hex}	– 19.5
6_{hex}	– 9.0	E_{hex}	– 21.0
7_{hex}	– 10.5	F_{hex}	– 22.5

3.2. Reduced Format – 64 Bit Format

The ASC 3553O is switched into the reduced format by pulling MODESEL to high and SUBFRAME1 and SUBFRAME2 to low.

In this mode, one frame consists of only one subframe with 64 Bit of data. No word syncs are allowed. All other features remain the same. A diagram of this format is shown below. Note that time is assumed to move from left to right in the diagram.

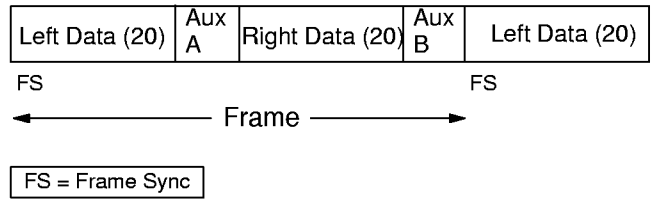


Fig. 3–5: Diagram of single frame in reduced format

3.3. Compatible Format – 32 Bit Format

This mode is intended to serve for compatible formats to existing serial audio interfaces. The ASC 3553O is switched into the compatible format by pulling MODESEL and SUBFRAME1 to high and SUBFRAME2 to low. Two pins on the digital input port (BI1 and BI2) are used to select further operation modes. With BI1 high, the internal serial clock is inverted: Now the positive transition of SCLOCK indicates data change, the negative edge defines the sampling edge. BI2 set to high assumes the serial sync signal to be placed one serial clock period before the frame boundary.

In this mode, one frames consists of 2 times 16 Bit of sound data. The sync detection circuit is triggered by a low to high condition on the serial sync line SSYNC, e.g. the more common 50 % duty cycle sync is also accepted. A diagram of this format is shown in Fig. 3–6. Note that time is assumed to move from left to right in the diagram.

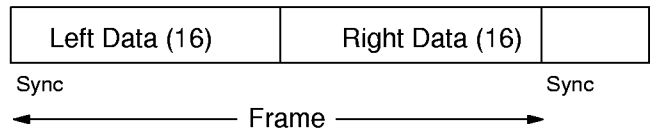


Fig. 3–6: Diagram of a sound frame in the 32 bit format

Table 3–4: Overview Frame Modes

Frame Mode	MODESEL	SUBFRAME1	SUBFRAME2
256 bit, subframe1	Low	Low	Low
256 bit, subframe2	Low	High	Low
256 bit, subframe3	Low	Low	High
256 bit, subframe4	Low	High	High
64 bit	High	Low	Low
32 bit	High	High	Low

Auxiliary data input (together with 4 LSB's of audio data) can be supplied to the ASCO via the BI4 pin. The input format uses the same structure as the above mentioned 32 bit sound frame. Auxiliary data output is available at the BO4 pin with the same timing, see Fig. 3–7. For a complete timing diagram see Fig. 5–5.

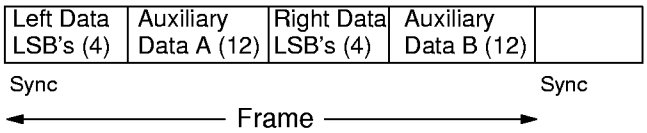


Fig. 3–7: Diagram of an auxiliary data frame in the 32 bit format

Note that only BI3 can be used for normal digital input operation, whereas for output only BO1 to BO3 are available. All other pins of the digital I/O port have special meanings in this mode.

By pulling BI4 to ground, the following default settings are valid: Input gain and output attenuation are fixed to 0dB, input select is switched to channel 1, mute is off and the output ports BO1 to BO3 remain inactive. On BO4 auxiliary data output is supplied.

4. Specifications

4.1. Outline Dimensions

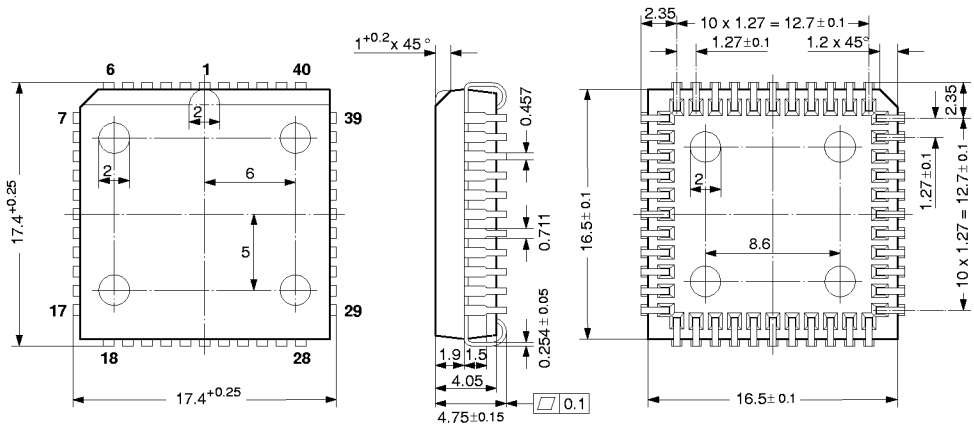


Fig. 4–1:
44-Pin Plastic Leaded Chip Carrier
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm

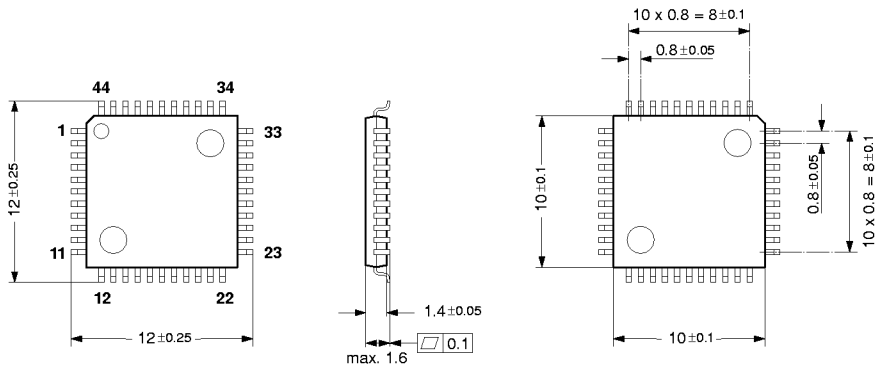


Fig. 4–2:
44-Pin Plastic Thin-Quad-Flat-Pack
(PTQFP44F)
Weight approximately 0.35 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

LV = if not used, leave vacant
VSUPD = if not used, connect to VSUPD
GNDD = if not used, connect to GNDD
X = obligatory; connect as described in circuit diagram
NC = not connected

INPUT = input signal line
OUTPUT= output signal line
SUP = supply pin
EXT = connection to external circuitry

Pin No. PLCC 44-pin	Pin No. PTQFP 44-pin	Connection (if not used)	Pin Name	Type	Short Description
1	39	X	SSYNC	INPUT	Serial sync input
2	40	X	$\overline{\text{RESET}}$	INPUT	Reset input
3	41	X	CLOCK	INPUT	Main clock input
4	42	X	VSUPD	SUP	Digital supply voltage
5	43	X	GNDD	SUP	Digital ground
6	44	LV	NC		
7	1	LV	NC		
8	2	LV	NC		
9	3	LV	NC		
10	4	LV	NC		
11	5	LV	NC		
12	6	LV	NC		
13	7	VSUPD	$\overline{\text{LOWPOWER}}$	INPUT	Low power mode input
14	8	NC	NC		
15	9	LV	ROUT	OUTPUT	Right analog output
16	10	LV	LOUT	OUTPUT	Left analog output
17	11	LV	NC		
18	12	LV	PDMCR	EXT	PDMR capacitor connection
19	13	LV	PDMCL	EXT	PDML capacitor connection
20	14	LV	BAGNDI	OUTPUT	Buffered internal analog ground
21	15	X	AGNDC	EXT	Internal analog ground
22	16	X	VREF	INPUT	Reference analog ground
23	17	X	GNDA	SUP	Analog ground
24	18	X	VSUPA	SUP	Analog supply voltage
25	19	LV	RIN1	INPUT	Right analog input, channel 1
26	20	LV	RIN2	INPUT	Right analog input, channel 2

Pin Connections and Short Descriptions, continued

Pin No. PLCC 44-pin	Pin No. PTQFP 44-pin	Connection (if not used)	Pin Name	Type	Short Description
27	21	LV	LIN1	INPUT	Left analog input, channel 1
28	22	LV	LIN2	INPUT	Left analog input, channel 2
29	23	X	MODESEL	INPUT	Mode select input
30	24	X	SUBFRAME1	INPUT	Subframe select 1 input
31	25	X	SUBFRAME2	INPUT	Subframe select 2 input
32	26	GNDD	TESTEN	INPUT	Test mode enable
33	27	GNDD	BI1	INPUT	Digital input 1
34	28	GNDD	BI2	INPUT	Digital input 2
35	29	GNDD	BI3	INPUT	Digital input 3
36	30	GNDD	BI4	INPUT	Digital input 4
37	31	LV	BO1	OUTPUT	Digital output 1
38	32	LV	BO2	OUTPUT	Digital output 2
39	33	LV	BO3	OUTPUT	Digital output 3
40	34	LV	BO4	OUTPUT	Digital output 4
41	35	LV	TEST2	OUTPUT	Test mode synchronization output
42	36	X	SDIN	INPUT	Serial data input
43	37	X	SDOUT	OUTPUT	Serial data output
44	38	X	SCLOCK	INPUT	Serial clock input

4.3. Pin Descriptions

PLCC 1 (PTQFP 39) – SSYNC: Serial sync input.
This input signal is used to indicate the start of a word or a frame for data transmissions via the serial interface.

PLCC 2 (PTQFP 40) – $\overline{\text{RESET}}$: Reset input.
In the steady state, high level is required. A low level resets the audio codec.

PLCC 3 (PTQFP 41) – CLOCK: Main clock input.
This input serves as a master clock for the codec. The A/D and D/A converters are driven by this input, so the audio codec should be supplied by a proper CLOCK input.

PLCC 4 (PTQFP 42) – VSUPD: Digital supply voltage.

This pin must be connected to the positive supply.

PLCC 5 (PTQFP 43) – GNDD: Digital ground.
This pin must be connected to the negative supply. It has to be used for ground connections in conjunction with digital signals.

PLCC 13 (PTQFP 7) – $\overline{\text{LOWPOWER}}$: Low power mode input.
A low level switches the codec to a low power mode. Analog outputs are muted, digital inputs and outputs are high impedance. If, in addition, TESTEN is set to high, the codec is switched to the zero power mode.

PLCC 15 (PTQFP 9) – ROUT: Right analog output.
The analog output signal is supplied by this pin. Analog output connection are intended to be AC coupled.

PLCC 16 (PTQFP 10) – LOUT: Left analog output.
See ROUT.

PLCC 18 (PTQFP 12) – PDMCR: Capacitor Connection.
The capacitor for the outer feedback loop of the pulse-

density modulator PDMR must be connected between this pin and BAGNDI.

PLCC 19 (PTQFP 13) – PDMCL: Capacitor Connection.
The capacitor for the outer feedback loop of the pulse-density modulator PDML must be connected between this pin and BAGNDI.

PLCC 20 (PTQFP 14) – BAGNDI: Buffered internal analog ground.
This pin is the buffered internal ground connection for the PDM capacitors. This pin shows a typical DC level of +2.25 V.

PLCC 21 (PTQFP 15) – AGNDC: Internal analog ground. This pin serves as the internal ground connection for the analog circuitry. It must be connected to VREFA with a 3.3 µF and a 100 nF capacitor in parallel. This pin shows a typical DC level of +2.25 V.

PLCC 22 (PTQFP 16) – VREF: Reference analog ground. This pin must also be connected separately to the single ground point. VREF serves as a clean ground and should be used as the reference for analog input and output connections.

PLCC 23 (PTQFP 17) – GNDA: Analog ground.
This pin serves as ground connection for the analog circuitry.

PLCC 24 (PTQFP 18) – VSUPA: Analog supply voltage.
Power is supplied via this pin for the analog circuitry of the audio codec. This pin must be connected to the positive supply.

PLCC 25 (PTQFP 19) – RIN1: Right analog input, channel 1.
The analog input signal for channel1 left is fed to this pin. Analog input connections must be AC coupled.

PLCC 26 (PTQFP 20) – RIN2: Right analog input, channel 2.
See RIN1.

PLCC 27 (PTQFP 21) – LIN1: Left analog input, channel 1.
See RIN1.

PLCC 28 (PTQFP 22) – LIN2: Left analog input, channel 2.
See RIN1.

PLCC 29 (PTQFP 23) – MODESEL: Mode select input.

By pulling MODESEL to high, the serial interface may be driven with additional formats.

PLCC 30 (PTQFP 24) – SUBFRAME1: Subframe select 1 input.
In conjunction with SUBFRAME2 this pin defines the subframe for which the codec is active.

PLCC 31 (PTQFP 25) – SUBFRAME2: Subframe select 2 input.
See SUBFRAME1.

PLCC 32 (PTQFP 26) – TESTEN: Test mode enable.
A high level switches the codec to production test mode. Enable must be low in normal mode. TESTEN = high and $\overline{\text{LOWPOWER}}$ = low switches the codec into zero power mode.

PLCC 33 (PTQFP 27) – BI1: Digital input 1.
Via the serial interface, the level supplied to this pin may be read.

PLCC 34 (PTQFP 28) – BI2: Digital input 2.
See BI1.

PLCC 35 (PTQFP 29) – BI3: Digital input 3.
See BI1.

PLCC 36 (PTQFP 30) – BI4: Digital input 4.
See BI1.

PLCC 37 (PTQFP 31) – BO1: Digital output 1.
Can be pulled high or low by means of control bits in the serial data stream. A corresponding zero pulls this pin to low. If the bit is set, the pin is driven to high.

PLCC 38 (PTQFP 32) – BO2: Digital output 2.
See BO1.

PLCC 39 (PTQFP 33) – BO3: Digital output 3.
See BO1.

PLCC 40 (PTQFP 34) – BO4: Digital output 4.
See BO1.

PLCC 41 (PTQFP 35) – TEST2: Test mode synchronization output.

PLCC 42 (PTQFP 36) – SDIN: Serial data input.
Used to input serial digital data to the codec.

PLCC 43 (PTQFP 37) – SDOUT: Serial data output.
This pin outputs the A-to-D converted signal according to the serial interface format.

PLCC 44 (PTQFP 38) – SCLOCK: Serial clock input.
This input signal serves for latching the input data on SDIN and output data on SDOUT. It defines the bit clock for the serial interface.

4.4. Pin Configuration

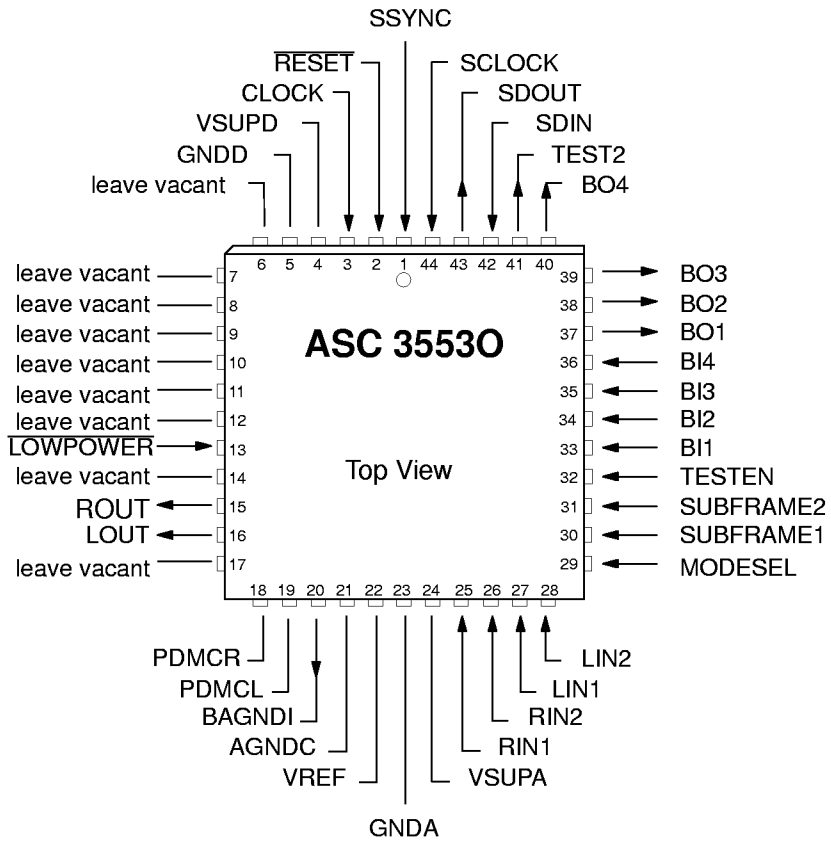


Fig. 4–3: Pinning of the ASC 3553O in PLCC44 package
Note: Pins labelled as ‘leave vacant’ must not be connected externally.

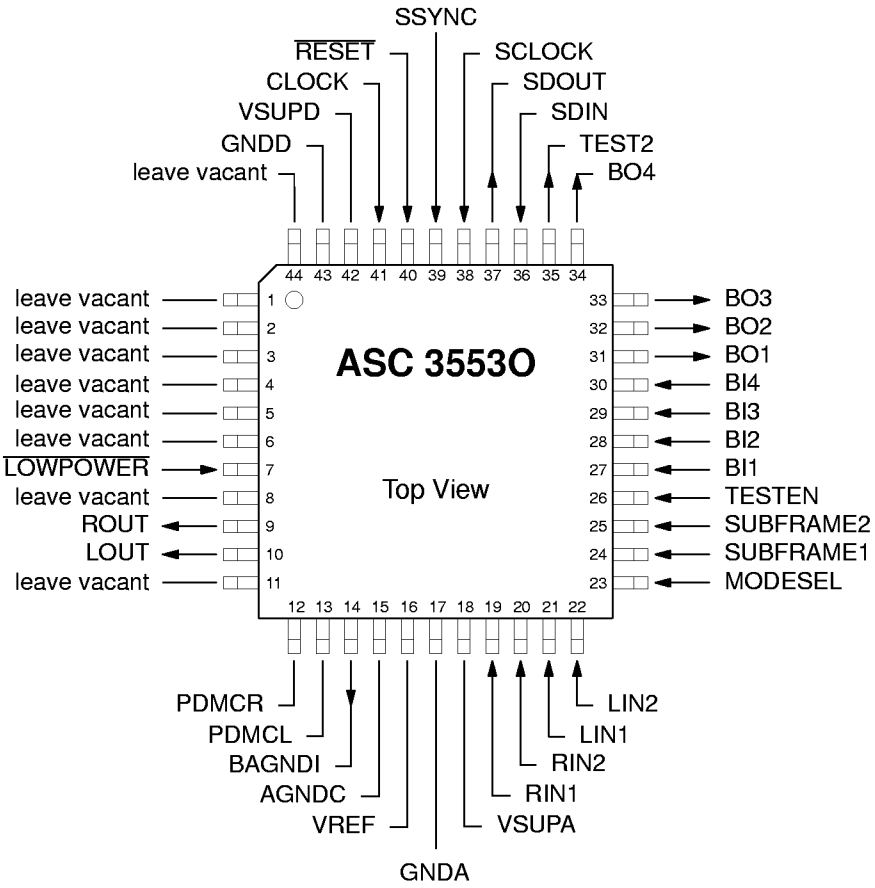


Fig. 4–4: Pinning of the ASC 3553O in PTQFP44F Package
Note: Pins labelled as ‘leave vacant’ must not be connected externally.

4.5. Electrical Characteristics

4.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	+70	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	4, 24	–0.3	+6	V
dV_{SUP}	Absolute Difference Analog to Digital Supply Voltage	4, 24	–	0.5	V
P_{TOT}	Chip Power Dissipation	4, 24		700	mW
V_I	Input Voltage, all Inputs	–	–0.3	V_{SUP} +0.3	V
I_I	Input Current, analog Inputs	25–28	–5	+5	mA
I_O	Output Current, all Outputs	–	–	*)	–
*) The outputs are short-circuit proof with respect to supply and ground. Total chip power dissipation must not exceed absolute maximum rating.					

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.5.2. Recommended Operating Conditions at T_A = 0 to 70 °C, f_{CLOCK} = 24.576 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	4, 24	4.5	5.0	5.5	V
f_{CLOCK}	CLOCK Input Frequency	3	8	24.576	25	MHz[1)]
D_{CLOCK}	CLOCK High to Low Ratio (measured at a level of 1.4 V)		45	–	55	%
T_{JITTER}	CLOCK Jitter		–	–	±50	ps
V_{AI0}	Input Voltage LIN1, RIN1, LIN2, RIN2 at minimum input gain	25–28	–	–	1.3	V_{RMS}
V_{AI1}	Input Voltage LIN1, RIN1, LIN2, RIN2 at maximum gain		–	–	0.1	V_{RMS}
Z_{AOL}	Analog Output Load	15, 16	6	–	 1	kΩ nF
I_{BAG}	BAGNDI Current Output	20	–2	–	+2	mA
C_{BAG}	BAGNDI Capacitive Load		–	–	500	pF
C_{AGND}	AGNDC Capacitor		1.0 [4)]	3.3 [4)]	–	µF

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{IHLR}	High Level, LOWPOWER and RESET Inputs	2, 13	3.0	–	–	V
V_{ILLR}	Low Level, LOWPOWER and RESET Inputs		–	–	0.8	V
V_{IH}	High Level, all other Digital Inputs	1, 3, 29–36, 42, 44	2.0	–	–	V
V_{IL}	Low Level, all other Digital Inputs		–	–	0.8	V
C_{PDM}	PDM Capacitor[2] for Standard CLOCK Range, f_{clock} = 22...25 MHz	18–20	–5%	680	+5%	pF[1]
C_{PDM}	PDM Capacitor[2] for Non-standard CLOCK Range, f_{clock} = 20...25 MHz f_{clock} = 18...25 MHz f_{clock} = 16...25 MHz		 –5% –5% –5%	 820 910 1000	 +5% +5% +5%	 pF[1] pF[1] pF[1]
f_{SCLOCK}	Input SCLOCK Frequency[3] 256 Bit Frame 64 Bit Frame 32 Bit Frame	44	 1/12 1/48 1/96	 – – –	 1/2 1/8 1/16	 f_{CLOCK} f_{CLOCK} f_{CLOCK}
T_{SCH}	Input SCLOCK High Pulse Width		32	–	–	ns
T_{SCL}	Input SCLOCK Low Pulse Width		32	–	–	ns
t_{IDS}	Input Data Setup Time	42	10	–	–	ns
t_{IDH}	Input Data Hold Time		8	–	–	ns
t_{ISS}	Input SSYNC Setup Time	1	10	–	–	ns
t_{ISH}	Input SSYNC Hold Time		8	–	–	ns
t_{IBS}	Input BI Setup Time	33–36	10	–	–	ns
t_{IBH}	Input BI Hold Time		8	–	–	ns
t_{RESET}	RESET Low Time after Stable CLOCK Input	2	10	–	–	µs

[1] For different PDM configurations (f_{clock}/C_{PDM}), please see corresponding SNR characteristics.
[2] Low loss type, e.g. ceramic type 1.
[3] For normal operation. Outside the specified frequency range analog outputs are muted, but digital input and outputs remain active.
[4] After power on, this cap is charged to V_{AGNDC} (typ. 2.25 V) with a time constant defined by an internal 125 kΩ resistor and the cap value used. During charging time (3τ), the specification figures are not valid. In the steady state, the AGNDC cap serves as a filter for the internal analog reference. A high cap value results in good noise suppression. To speed up the charging time after power on, the cap value may be reduced. In a typical application, no degradation of SNR was found with a cap value as low as 100 nF. For good results even in very noisy environments, we recommend using at least the given minimum value.

4.5.3. Characteristics at T_A = 0 to 70 °C, V_{SUP} = 4.5 to 5.5 V, f_{CLOCK} = 24.576 MHz

(Typical values are measured at T_A = 25 °C, V_{SUP} = 5 V.)

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
Z_{AII}	Analog Input Impedance all modes 0 dB gain 22.5 dB gain deselected input low power mode zero power mode	25–28	 24 140 24 130 240 high Z	 – 187 31 174 313 high Z	 420 250 45 230 420 high Z	 kΩ 2) kΩ 2) kΩ kΩ 2) kΩ 2) 2)	
Z_{AOI}	Analog Output Impedance, Active Low Power zero power mode	15, 16	 300 high Z	 450 high Z	 600 125 +3.3 high Z	 Ω kΩ 2) µF 2) 2)	
V_{AOV}	Digital Full Scale Analog Output Voltage		0.84	0.94	1.04	V_{RMS}	Output Attenuation = 0 dB $R_{load} \geq$ 100 kΩ
V_{AICL}	Analog Input Clipping Level	25–28	1.3	1.44	1.58	V_{RMS} 2)	Input Gain = 0 dB; defines analog input reference level: 0 dBr
SNR_{AD}	SNR A/D, 48 kHz; Input Gain = 0 dB 48 kHz; Input Gain = 22.5 dB 32 kHz; Input Gain = 0 dB 24 kHz; Input Gain = 0 dB	25–28	 82 – – –	 84 81 88 92	 – – – –	 dB 1) dB 1) 2) dB 1) 2) dB 1) 2)	Noise measurement with signal max. –20 dB, BW = 0.45 fs unweighted, f_{sig} = 1 kHz
SNR_{AD}	SNR A/D, for Non-standard PDM Configurations, 48 kHz mode, Input Gain = 0 dB @ C_{PDM} = 820 pF @ C_{PDM} = 910 pF @ C_{PDM} = 1000 pF	25–28	 – – –	 83 81 79	 – – –	 dB 1) 2) dB 1) 2) dB 1) 2)	Noise measurement with signal max. –20 dB, BW = 0.45 fs unweighted, f_{sig} = 1 kHz
SNR_{DA}	SNR D/A, Output Attenuation = 0 dB Output Attenuation = 22.5 dB	15, 16	 90 –	 93 85	 – –	 dB dB 2)	Noise measurement with signal max. –20 dB, BW = 20 kHz
THD_{ADH}	THD A/D	25–28	–	–	0.03	%	BW = 0.45 fs unweighted, f_{sig} = 1 kHz, –3 dBr Input Gain = 0 dB
THD_{DAH}	THD D/A	15, 16	–	–	0.01	%	f_{sig} = 1 kHz, –3 dBFS, unweighted 20 Hz...20 kHz
IMD_{AD}	IM Distortion A/D	25–28	–	0.01	0.1	%	Input signal: 14 kHz +15 kHz, sum –3 dBr, measuring 1 kHz intermodulation
XTALK0	Crosstalk Attenuation within Active Channel Pair	15, 16, 25–28	80	–	–	dB	f_{sig} = 1 kHz, unused analog inputs connected to ground measuring ADDA
XTALK1	Crosstalk Attenuation from Non-Selected Input Pair	25–28	80	–	–	dB	fsig = 1 kHz, unused analog inputs connected to ground measuring AD
G_{AOM}	Analog Output Attenuation in Mute Position	15, 16	80	–	–	dB	
BW_{ADDA}	1 dB Bandwidth A/D to D/A @ f_s = 32 kHz @ f_s = 48 kHz	15, 16, 25–28	 14.5 21.6	 – –	 – –	 kHz 2) kHz 2)	

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
dG_{AIP}	Gain Variation within Active Input Pair Input Gain = 0 dB Output Attenuation = 0 dB	25–28	–	–	0.5	dB	fsig = 1 kHz, –3 dBr
dG	Input Gain and Output Attenuation Accuracy	15, 16, 25–28	–	–	0.75	dB	fsig = 1 kHz, –3 dBr
V_{AGNDC}	AGNDC Operating Voltage	21	2.15	2.25	2.35	V	
dV_{AOC}	Analog Output Click	15, 16	–15	–	15	mV	Normal Operation Mute to Low Power and vice versa
dV_{AB}	AGNDC to BAGNDI Difference Voltage	20, 21	–5	–	5	mV	
V_{AIO}	Analog Input Offset Voltage (Difference of AGNDC and Input Voltage leading to digital zero output)	21, 25–28	–30	–	30	mV	Input gain = 0 dB
V_{AOO}	Analog Output Offset Voltage (Difference of AGNDC and Digital Zero D/A Output Voltage)	15, 16, 21	–30	–	30	mV	Output attenuation = 0 dB
Z_{BAG}	BAGNDI Output Impedance	20	–	0.1	–	Ω [2]	f < 1 kHz
I_{SUP}	Supply Current Active	4, 24	–	48	65	mA	$R_{load} \geq 100$ kΩ
I_{SUPD}	Digital Supply Current Active	4	–	41	55	mA	$R_{load} \geq 100$ kΩ
I_{SUPA}	Analog Supply Current Active	24	–	7	12	mA	$R_{load} \geq 100$ kΩ
I_{SUPLP}	Supply Current, Low-Power Mode	4, 24	–	75	150	µA	CLOCK, SCLOCK, SSYNC, and SDIN grounded. Other digital inputs either GNDD or VSUPD. Analog outputs AC coupled.
I_{SUPZP}	Supply Current, Zero-Power Mode	4, 24	–	<1 µA	20	µA	CLOCK, SCLOCK, SSYNC, and SDIN grounded. Other digital inputs either GNDD or VSUPD
PSRR	Power Supply Rejection Ratio 1 kHz	4, 15, 16, 24	52	70	–	dB	VSUP modulated with 1kHz and 5 V ± 10% pp. Analog input grounded, measuring ADDA analog output.
V_{OH}	Digital Output High Voltage	37–40, 43	2.8	–	–	V	@ 1.6 mA Output Current
V_{OL}	Digital Output Low Voltage		–	–	0.4	V	@ 1.6 mA Output Current
T_{ODC}	SCLOCK Negative Transition to SDOUT Data Change	43, 44	–	13	–	ns	SDOUT with 20 pF load
T_{OBC}	SCLOCK Negative Transition to BO Data Change	37–40	–	13	–	ns	BO with 20 pF load
I_{DI}	Digital Input Current	1–3, 13, 29–36, 42, 44	–10	–	+10	µA	

[1] Production parts are tested for fclock = 24.576 MHz and CPDM = 680 pF. With different PDM configurations the listed typical SNR values will be obtained for fclock = 24.576 MHz. The typical SNR over the whole specified clock frequency range will be equal to or better than the listed values. Being operated at the lowest allowed frequency for a given CPDM, the parts tend to have typically 85 dB SNR.

[2] Not being explicitly measured in production test. Figures are verified by other tests or by sample qualification.

Table 4–1: Digital filter characteristics A/D

Parameter	Min.	Max.	Unit
Frequency Response, ±0.5 dB	0.0	0.45	F_s
Pass Band Ripple	–	±0.15	dB
Stop Band rejection, 0.55 F_s...1.45 F_s	84	–	dB
Stop Band rejection, 1.45 F_s...F_{CLOCK}/4–0.55 F_s	75	–	dB
Pass Band Group Delay variation	–	0.0	µs

Table 4–2: Digital filter characteristics D/A

Parameter	Min.	Max.	Unit
Frequency Response, ±0.5 dB	0.0	0.45	F_s
Pass Band Ripple	–	±0.15	dB
Stop Band rejection, 0.55 F_s...1.45 F_s	84	–	dB
Stop Band rejection, 1.45 F_s...7.45 F_s (all sample rates except 48 kHz)	75	–	dB
Stop Band rejection, 1.45 F_s...3.45 F_s (48 kHz sample rate)	75	–	dB
Pass Band Group Delay variation	–	0.0	µs

5. Timing Specifications

5.1. Full Feature Format and Reduced Format

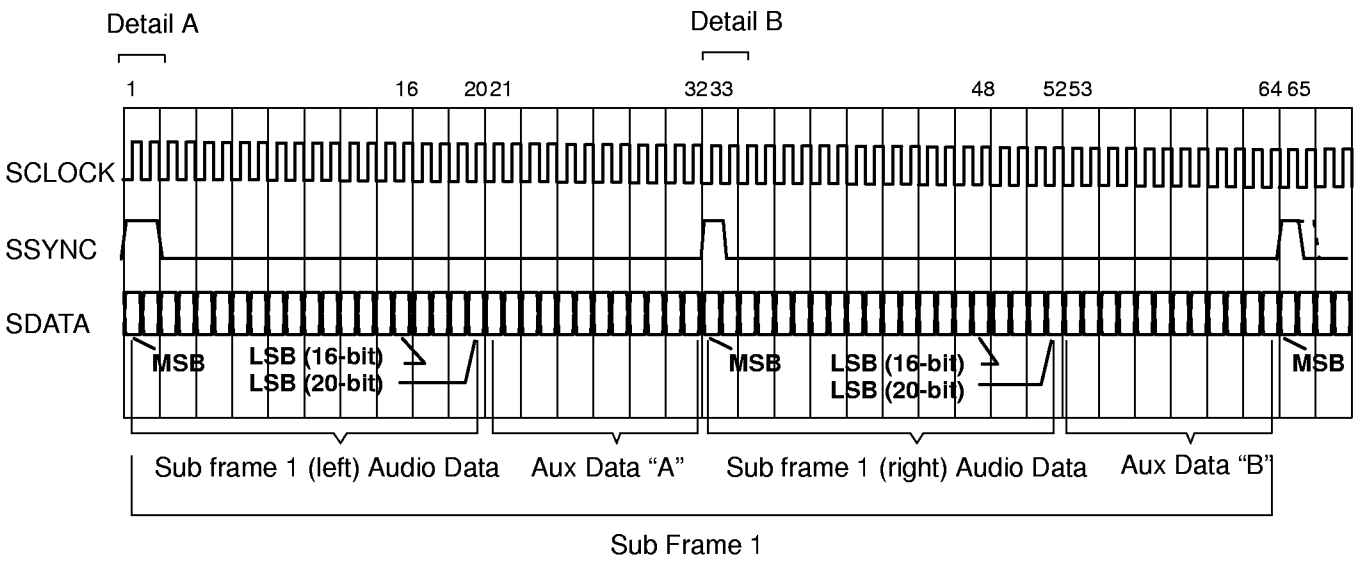


Fig. 5–1: Serial interface format for 256 bit frame and 64 bit frame

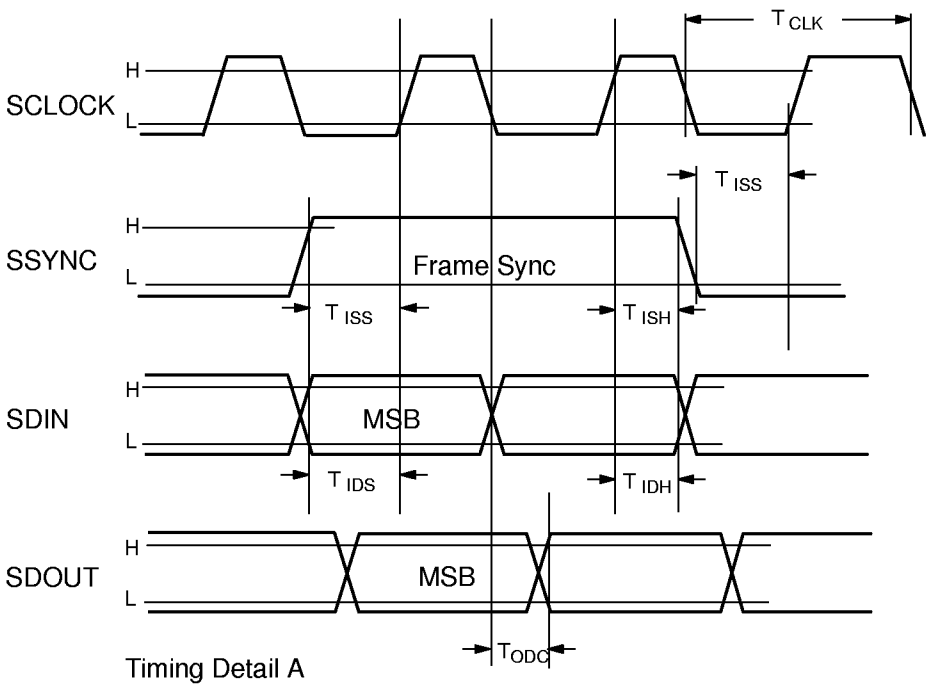


Fig. 5–2: Timing detail A

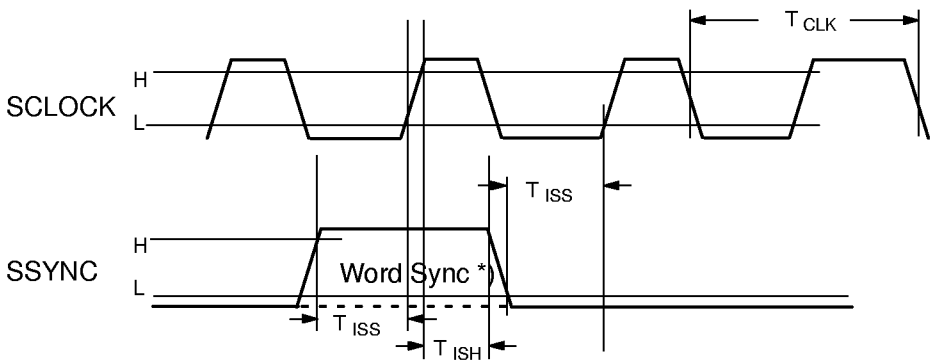


Fig. 5–3: Timing detail B
*) Word sync is not required in 256 bit frame mode and not allowed in 64 or 32 bit frame mode.

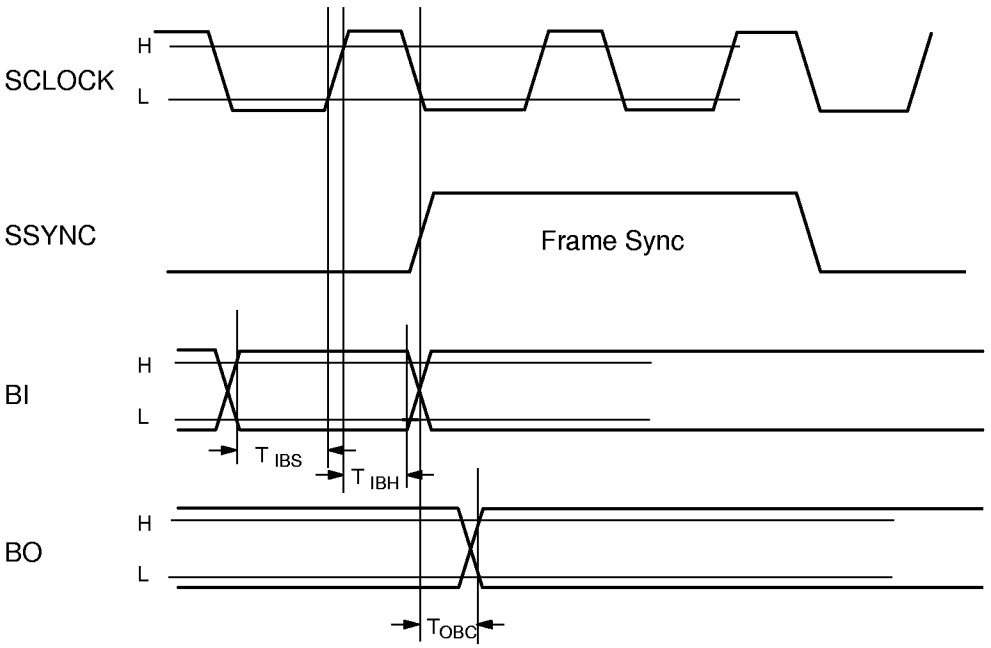


Fig. 5–4: Digital port timing

5.2. Compatible Formats – 32 Bit Format

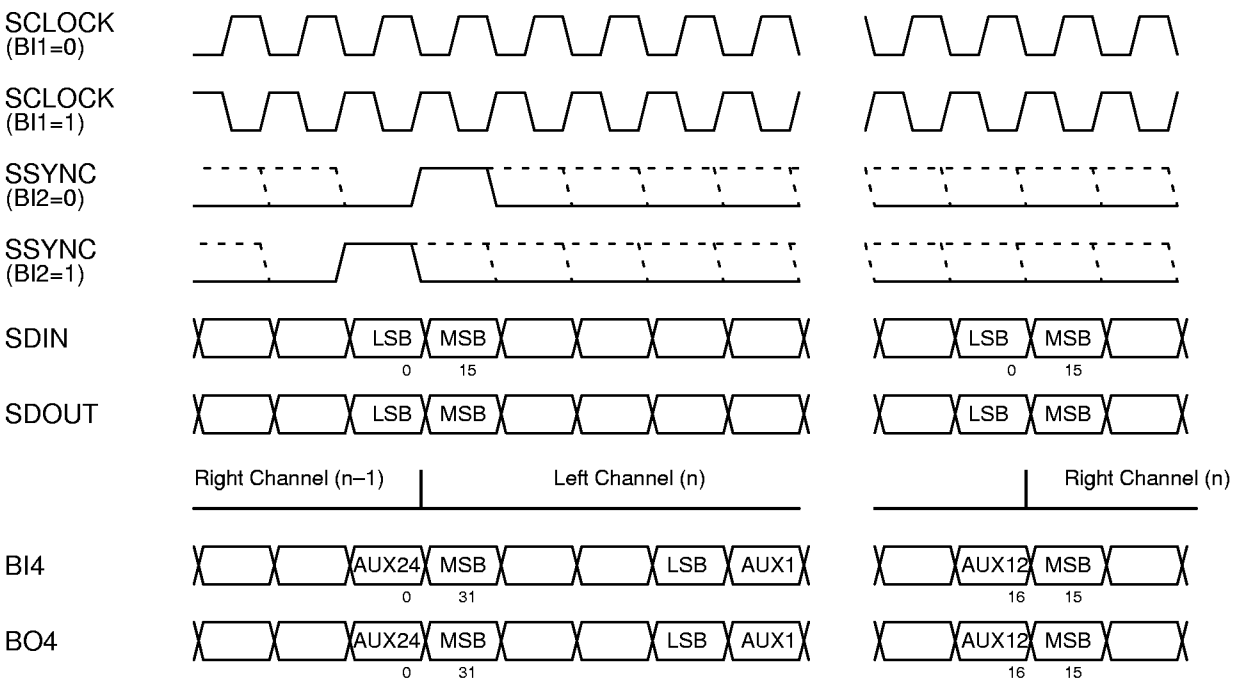


Fig. 5–5: Serial timing in 32 bit frame mode

6. Typical Application Circuit

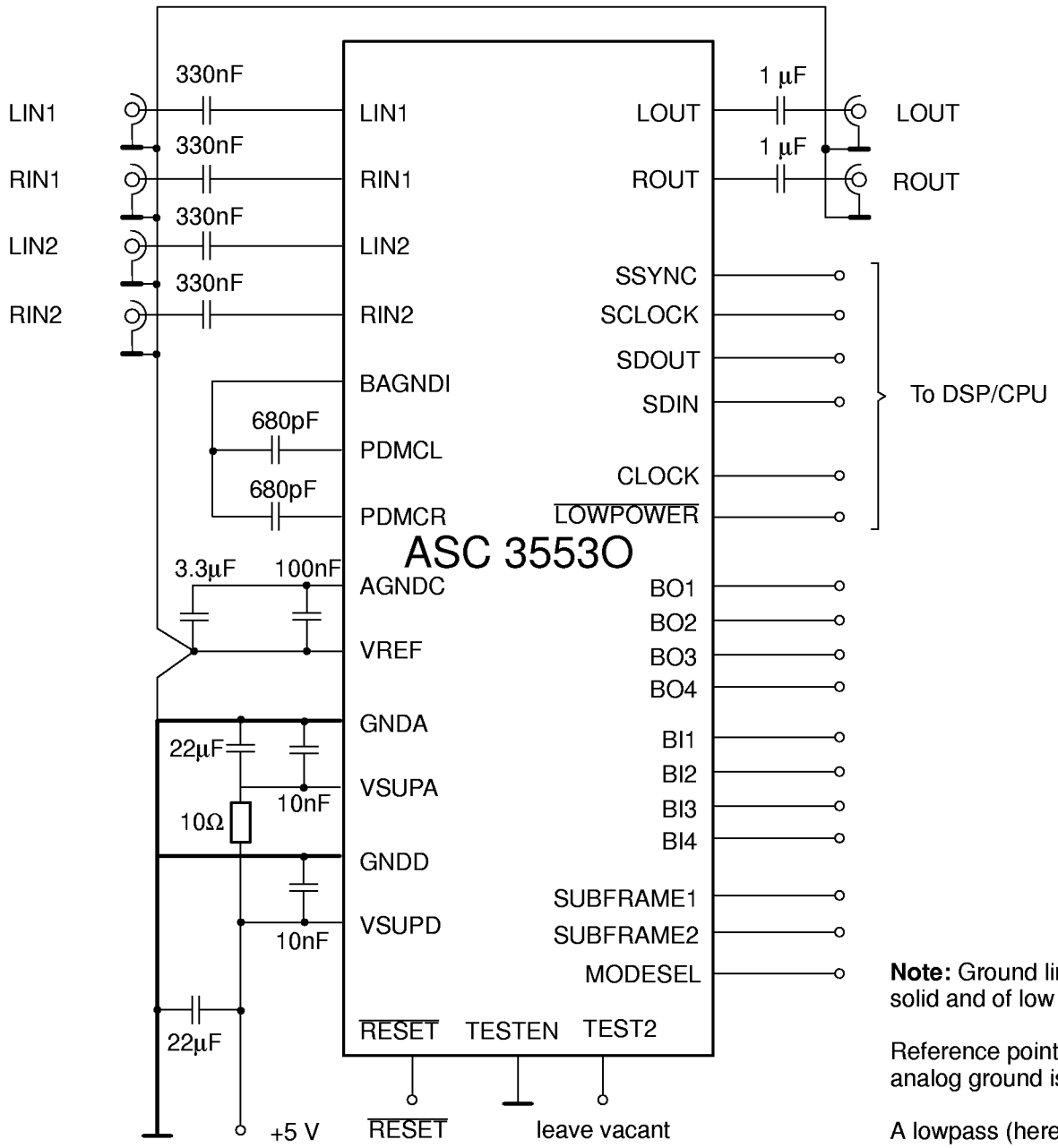


Fig. 6–1: ASC 3553O typical application circuit

Note: Ground lines should be solid and of low impedance.

Reference point for external analog ground is VREF.

A lowpass (here formed by a 10 Ω Resistor and a 22 µF Cap) is recommended to suppress HF noise on the VSUPA line.

7. Demo Board Schematic

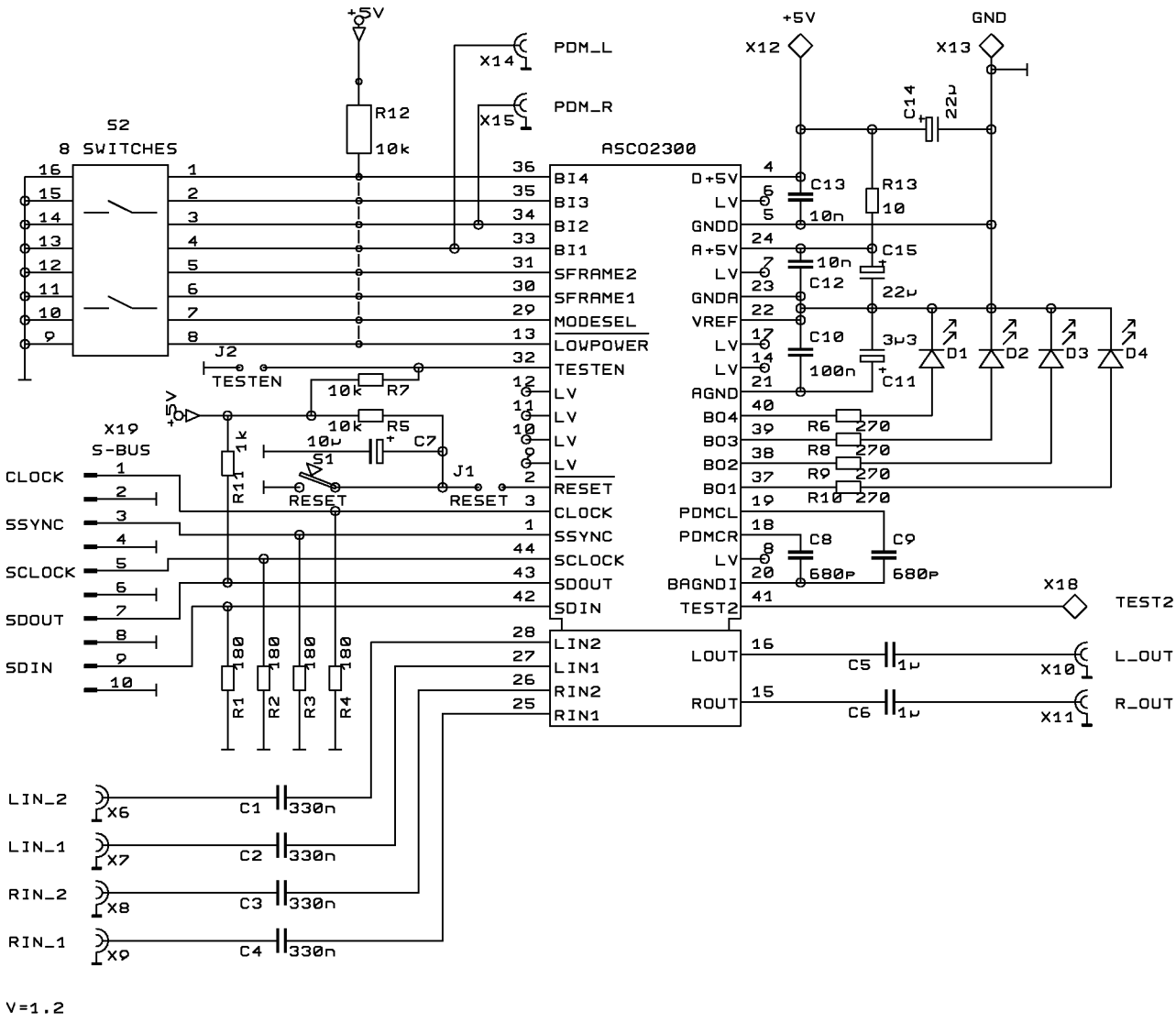


Fig. 7–1: ASC 3553O Demo Board Schematic