

## CMOS-CCD 1H/2H Delay Line for NTSC

### Description

The CXL5509M/P is a CMOS-CCD delay line developed for video signal processing. Usage in conjunction with an external low-pass filter provide 1H and 2H delay signals simultaneously (For NTSC signals).

### Features

- Single power supply (5V)
- Low power consumption 130mW (Typ.)
- Built-in peripheral circuits
- Built-in quadruple PLL circuit
- For NTSC signals
- 1 input and 2 outputs
- (Outputs for both 1H and 2H delays)

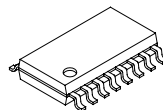
### Functions

- 906-bit (1H) and 1816-bit (2H) CCD register
- Clock driver
- Auto-bias circuit
- Sync tip clamp circuit
- Sample-and-hold circuit
- Quadruple PLL circuit

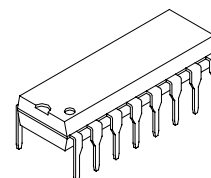
### Structure

CMOS-CCD

CXL5509M  
16 pin SOP (Plastic)



CXL5509P  
16 pin DIP (Plastic)



### Absolute Maximum Ratings (Ta = 25°C)

- Supply voltage V<sub>DD</sub> 6 V
- Operating temperature T<sub>opr</sub> -10 to +60 °C
- Storage temperature T<sub>stg</sub> -55 to +150 °C
- Allowable power dissipation P<sub>D</sub>

|          |     |    |
|----------|-----|----|
| CXL5509M | 400 | mW |
| CXL5509P | 800 | mW |

### Recommended Operating Condition (Ta = 25°C)

- Supply voltage V<sub>DD</sub> 5 ± 5% V

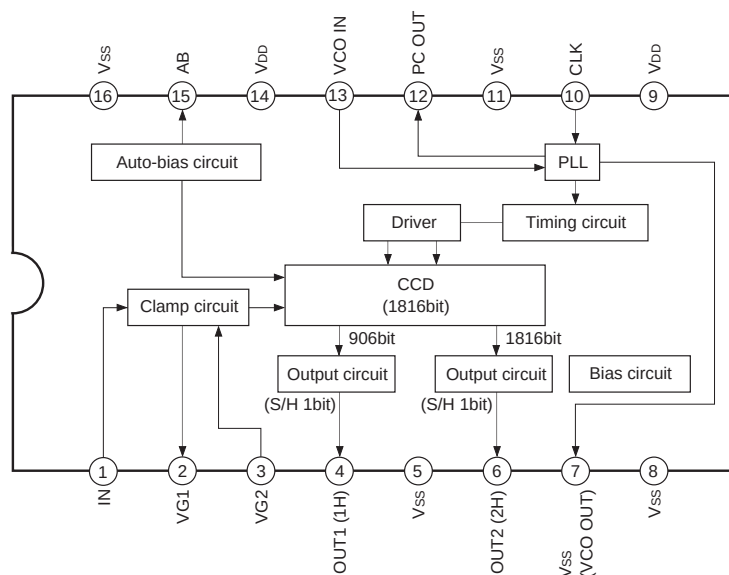
### Recommended Clock Conditions (Ta = 25°C)

- Input clock amplitude V<sub>CLK</sub> 0.3 to 1.0 V<sub>p-p</sub>  
(0.5V<sub>p-p</sub> typ.)
- Clock frequency f<sub>CLK</sub> 3.579545 MHz
- Input clock waveform sine wave

### Input Signal Amplitude

- V<sub>SIG</sub> 571mV<sub>p-p</sub> (Max.) (at internal clamp condition)

### Block Diagram and Pin Configuration (Top View)



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## Pin Description

| Pin No. | Symbol                    | I/O | Description                           | Impedance                    |
|---------|---------------------------|-----|---------------------------------------|------------------------------|
| 1       | IN                        | I   | Signal input<br>(Non-inverted signal) | > 10k $\Omega$ (at no clamp) |
| 2       | VG1                       | O   | Gate bias 1 DC output                 |                              |
| 3*      | VG2                       | I   | Gate bias 2 DC input                  |                              |
| 4       | OUT1                      | O   | 1H signal output<br>(Inverted signal) | 40 to 500 $\Omega$           |
| 5       | V <sub>SS</sub>           | —   | GND                                   |                              |
| 6       | OUT2                      | O   | 2H signal output<br>(Inverted signal) | 40 to 500 $\Omega$           |
| 7       | V <sub>SS</sub> (VCO OUT) | (O) | GND or VCO output (4fsc)              |                              |
| 8       | V <sub>SS</sub>           | —   | GND                                   |                              |
| 9       | V <sub>DD</sub>           | —   | Power supply (5V)                     |                              |
| 10      | CLK                       | I   | Clock input (fsc)                     | > 10k $\Omega$               |
| 11      | V <sub>SS</sub>           | —   | GND                                   |                              |
| 12      | PC OUT                    | O   | Phase comparator output               |                              |
| 13      | VCO IN                    | I   | VCO input                             |                              |
| 14      | V <sub>DD</sub>           | —   | Power supply (5V)                     |                              |
| 15      | AB                        | O   | Autobias DC output                    | 600 to 200k $\Omega$         |
| 16      | V <sub>SS</sub>           | —   | GND                                   |                              |

## \* Description of Pin 3 (VG2)

Control of input signal clamp condition

0V ..... Sync tip clamp condition

5V ..... Center bias condition

The input signal is biased to approx. 2.1V by means of the IC internal resistance (approx. 10k $\Omega$ ).  
In this mode, the input signal is limited to APL 50% and the maximum input signal amplitude is at 200mVp-p.

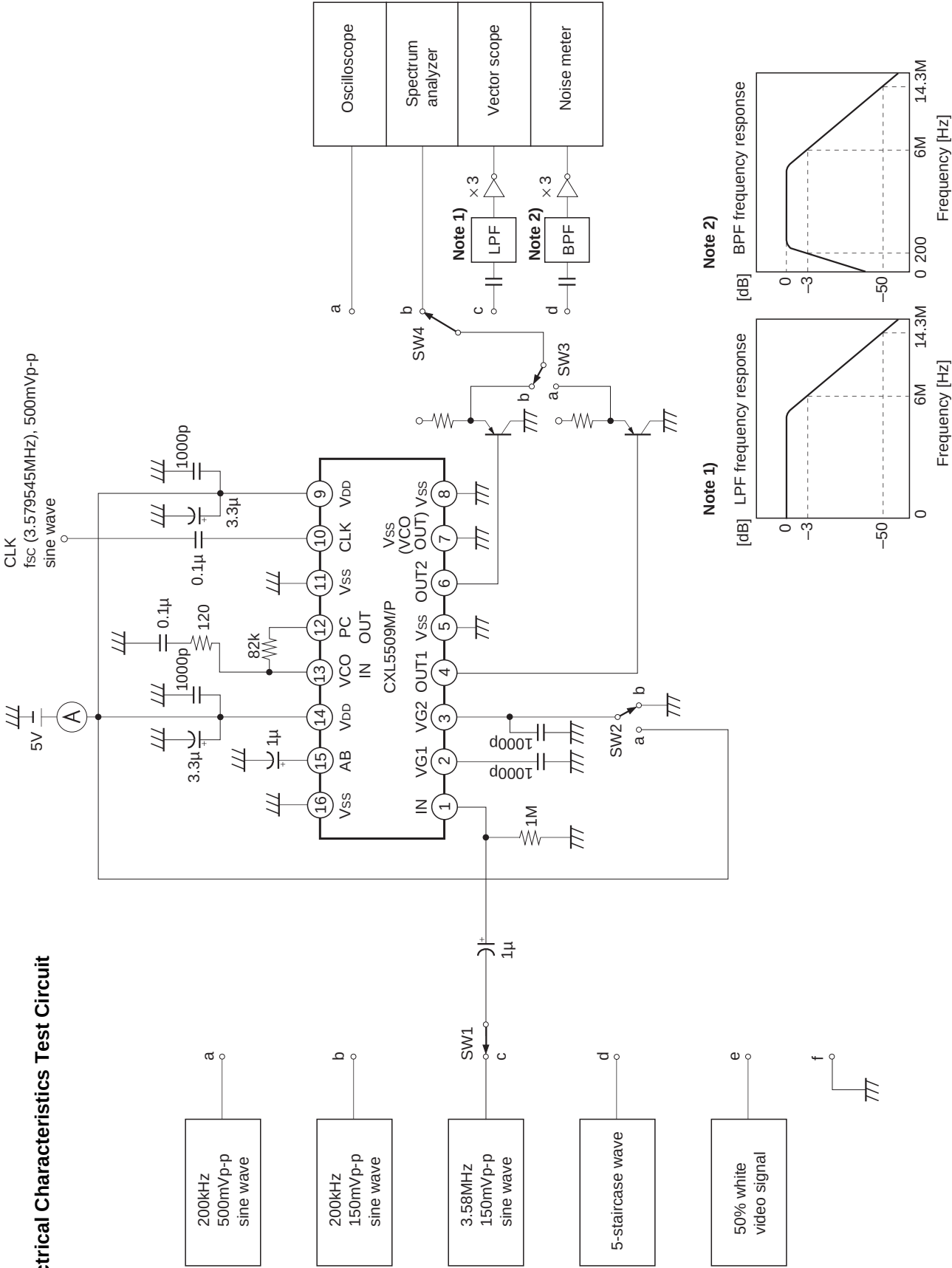
## Electrical Characteristics

(Ta = 25°C, V<sub>DD</sub> = 5V, f<sub>CLK</sub> = 3.579545MHz, V<sub>CLK</sub> = 500mVp-p, sine wave)

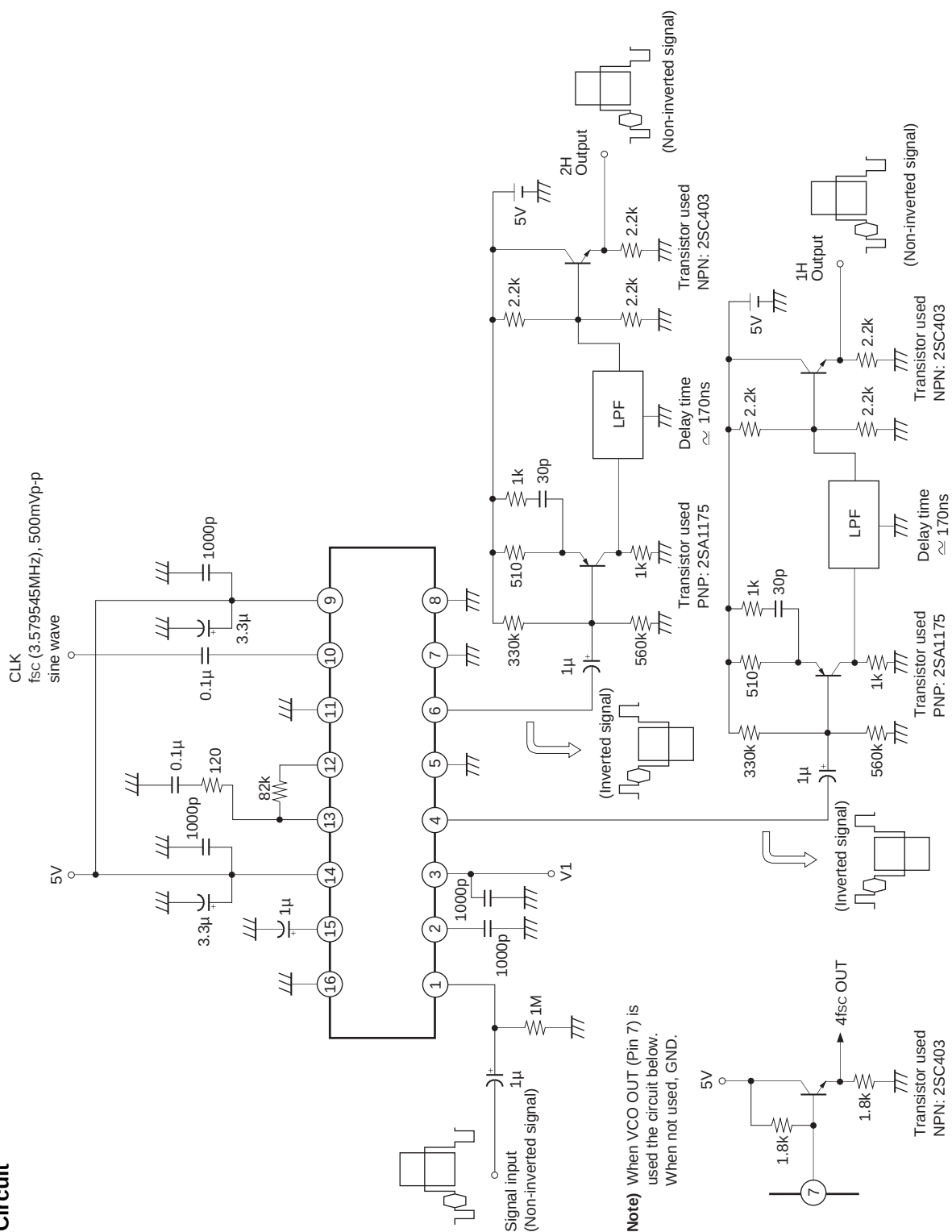
See "Electrical Characteristics Test Circuit"

| Item               | Symbol          | Test conditions<br>(Note 1)                 | SW conditions |   |   |   | Min. | Typ. | Max. | Unit   | Note |
|--------------------|-----------------|---------------------------------------------|---------------|---|---|---|------|------|------|--------|------|
|                    |                 |                                             | 1             | 2 | 3 | 4 |      |      |      |        |      |
| Supply current     | I <sub>DD</sub> | —                                           | a             | b | a | a | 16   | 26   | 36   | mA     | 2    |
| Low frequency gain | GL1             | 200kHz,<br>500mVp-p,<br>sine wave           | a             | b | a | b | −2   | 0    | 2    | dB     | 3    |
|                    | GL2             |                                             | a             | b | b | b | −2   | 0    | 2    |        |      |
| Frequency response | fR1             | 200kHz ↔ 3.58MHz,<br>150mVp-p,<br>sine wave | b ↔ c         | a | a | b | −2.0 | −1.0 | 0    | dB     | 4    |
|                    | fR2             |                                             | b ↔ c         | a | b | b | −2.0 | −1.0 | 0    |        |      |
| Differential gain  | DG1             | 5-staircase wave                            | d             | b | a | c | —    | 3    | 5    | %      | 5    |
|                    | DG2             |                                             | d             | b | b | c | —    | 3    | 5    |        |      |
| Differential phase | DP1             | 5-staircase wave                            | d             | b | a | c | —    | 3    | 5    | degree | 5    |
|                    | DP2             |                                             | d             | b | b | c | —    | 3    | 5    |        |      |
| S/N ratio          | SN1             | 50% white<br>video signal                   | e             | b | a | d | 52   | 56   | —    | dB     | 6    |
|                    | SN2             |                                             | e             | b | b | d | 52   | 56   | —    |        |      |
| S/H pulse coupling | CP1             | No signal input                             | f             | b | a | a | —    | —    | 350  | mVp-p  | 7    |
|                    | CP2             |                                             | f             | b | b | a | —    | —    | 350  |        |      |

Electrical Characteristics Test Circuit



## Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes

(1) By switching SW2, input condition turns out as follows.

| SW2 condition | Input condition                                                                                     |
|---------------|-----------------------------------------------------------------------------------------------------|
| a             | Center bias condition (approx. 2.1V)<br>Approx. 2.1V bias is applied internally to the input signal |
| b             | Sync tip clamp conditions                                                                           |

(2) This is the IC supply current value during clock and signal input.

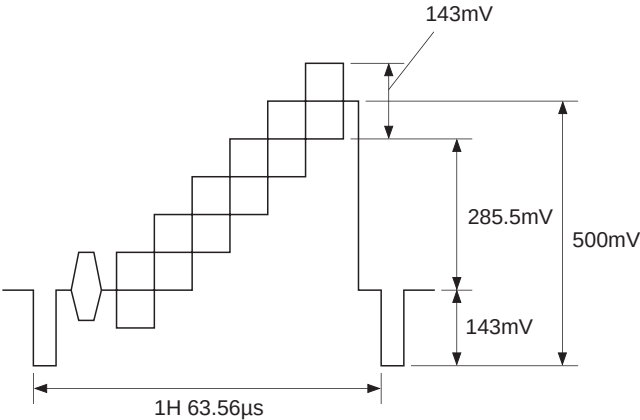
(3) GL is the output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

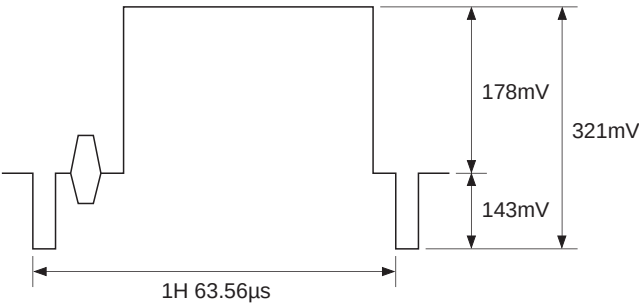
(4) Indicates the dissipation at 3.58MHz in relation to 200kHz.  
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 3.58MHz sine wave is fed to same, calculation is made according to the following formula.

$$fR = 20 \log \frac{\text{OUT pin output voltage (3.58MHz) [mVp-p]}}{\text{OUT pin output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

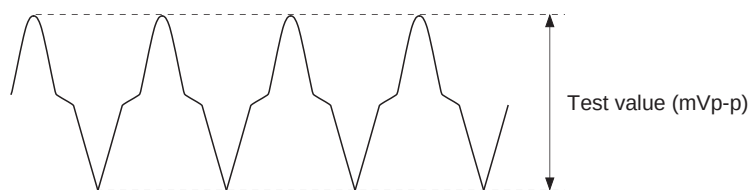
(5) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:



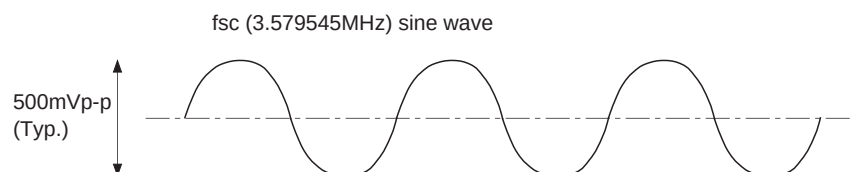
(6) S/N ratio during 50% white video signal input shown in figure below is tested at video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



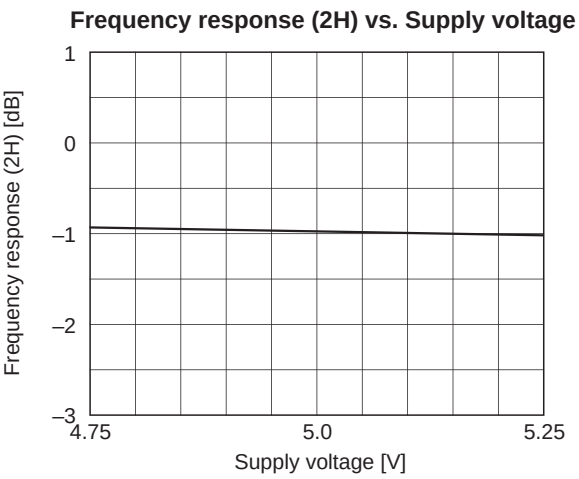
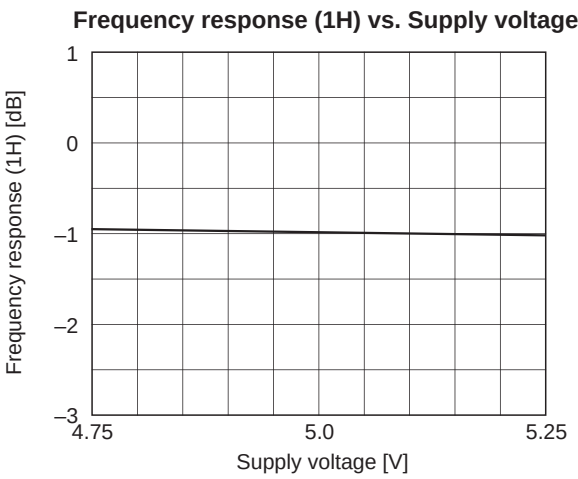
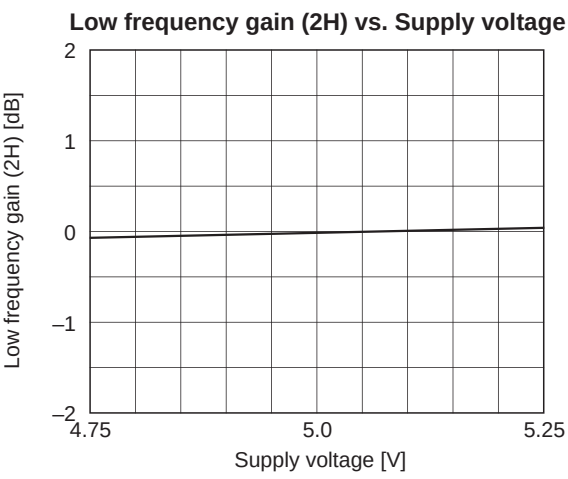
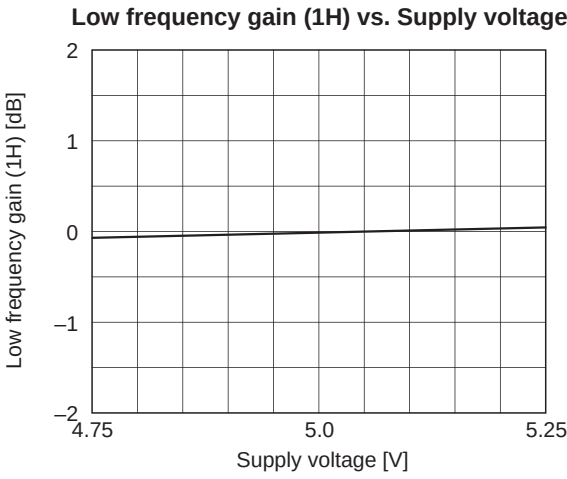
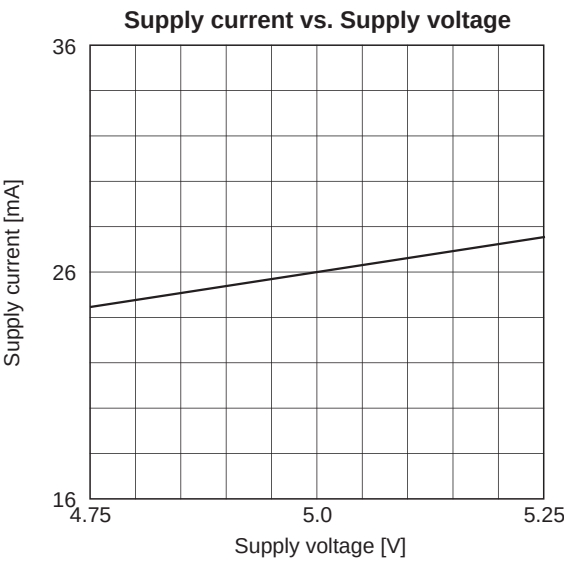
- (7) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested.



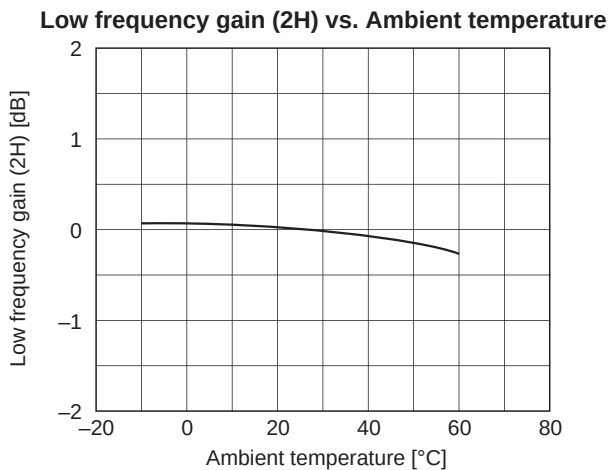
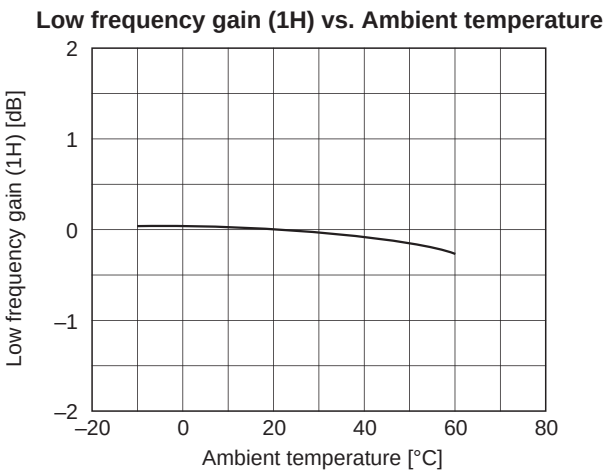
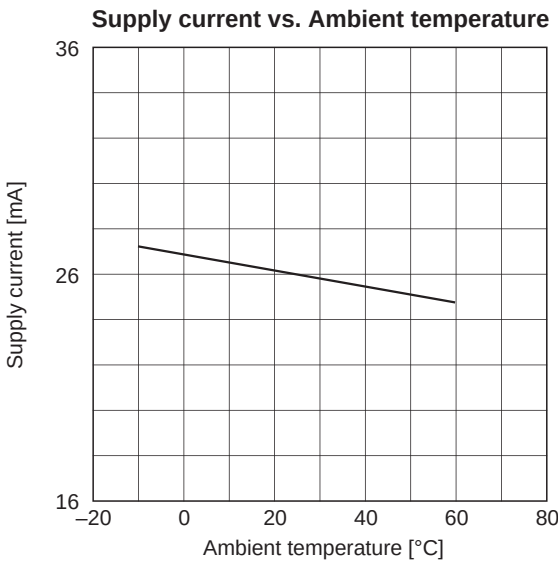
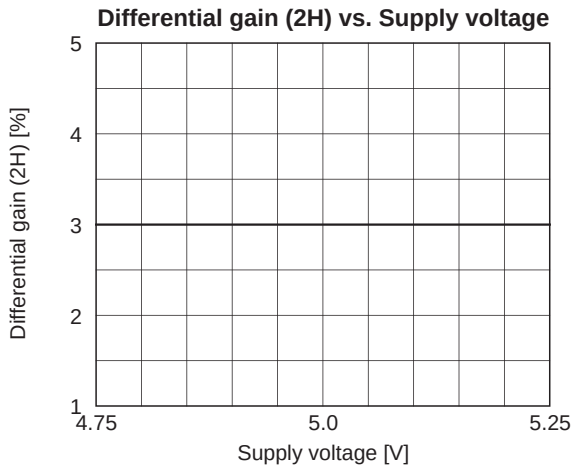
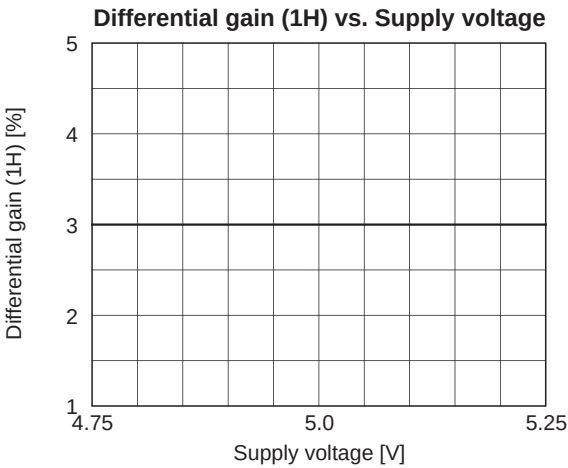
### Clock



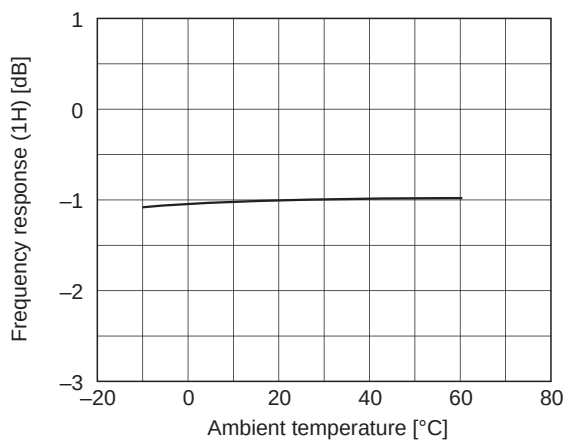
Example of Representative Characteristics



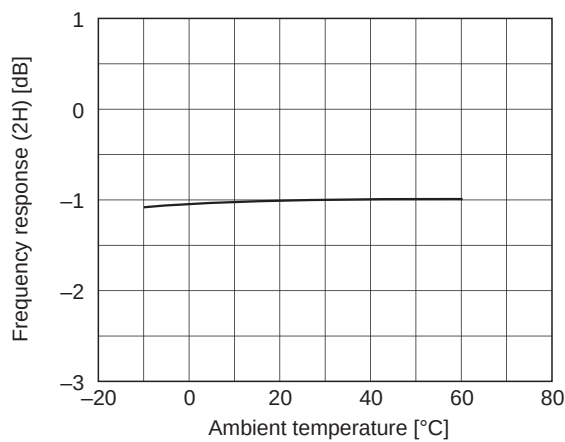




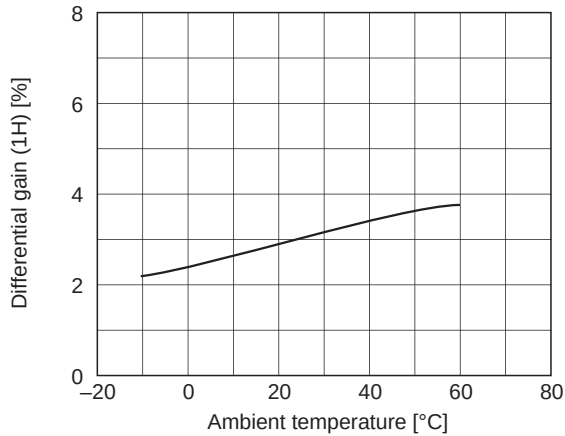
Frequency response (1H) vs. Ambient temperature



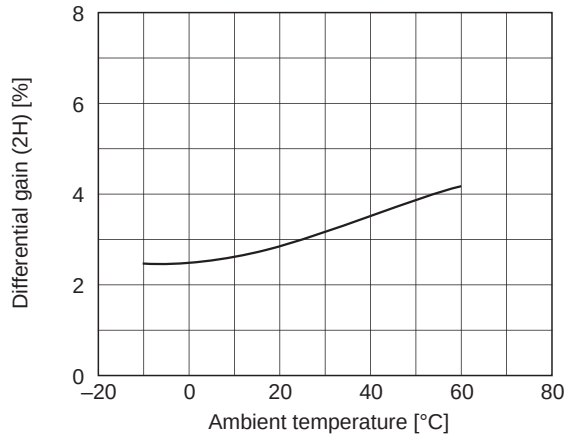
Frequency response (2H) vs. Ambient temperature

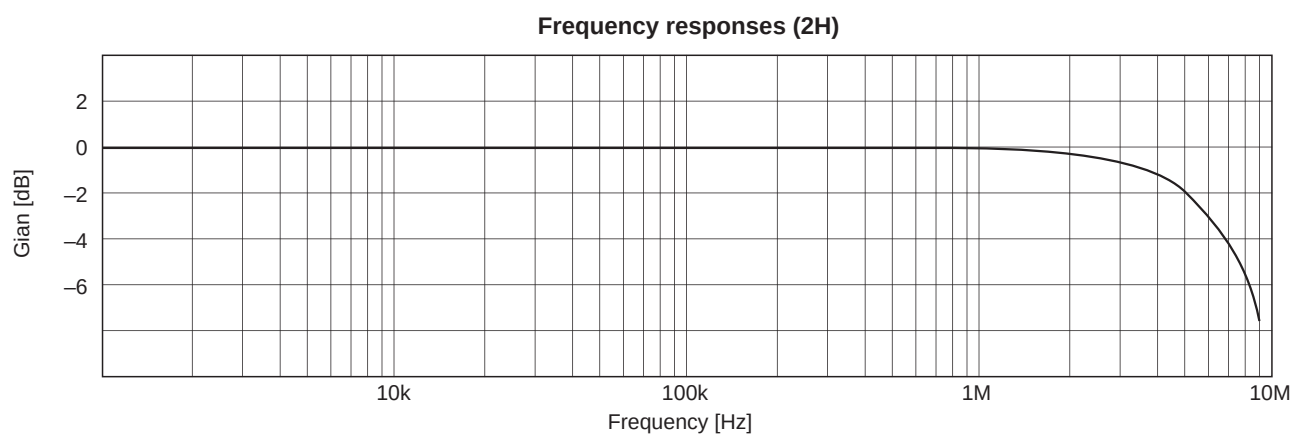
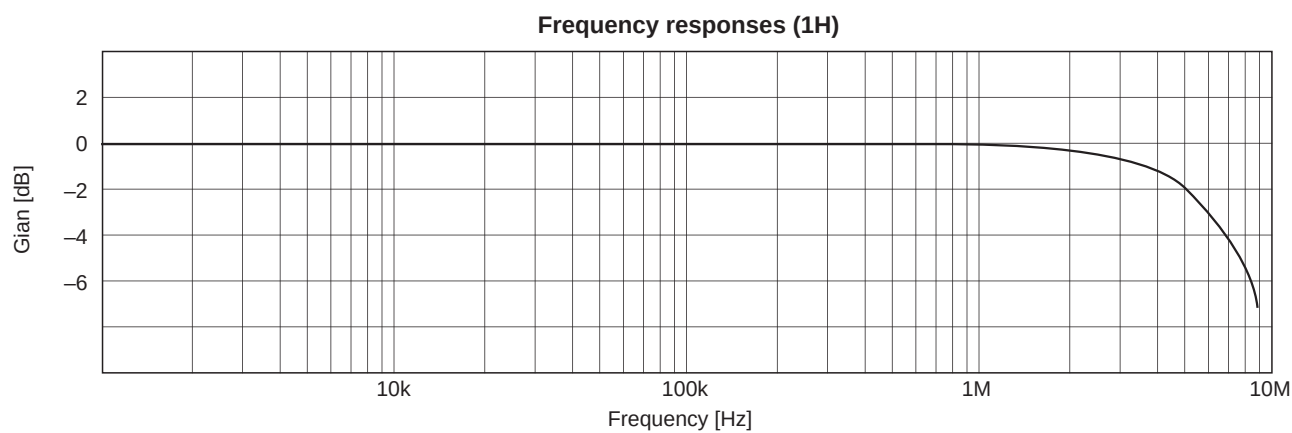


Differential gain (1H) vs. Ambient temperature



Differential gain (2H) vs. Ambient temperature



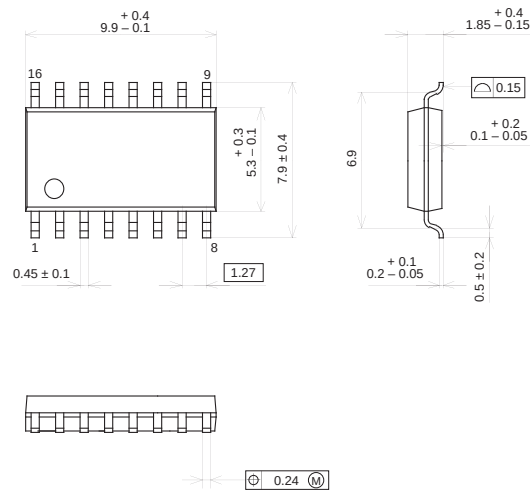


**Note)** 1H means 1H output; 2H means 2H output.

Package Outline      Unit: mm

CXL5509M

16PIN SOP (PLASTIC)



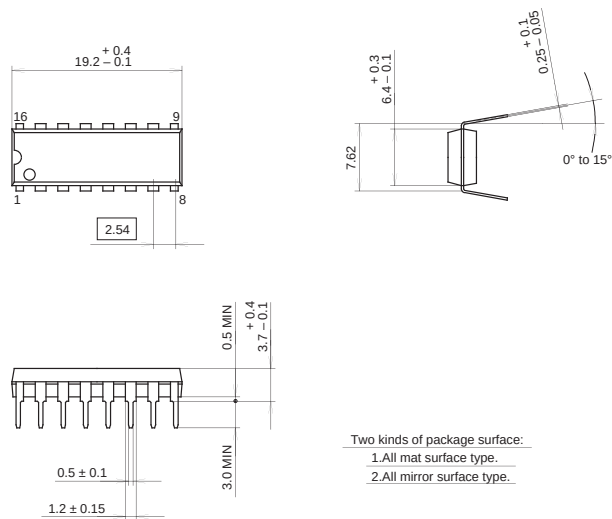
PACKAGE STRUCTURE

|            |               |
|------------|---------------|
| SONY CODE  | SOP-16P-L01   |
| EIAJ CODE  | SOP016-P-0300 |
| JEDEC CODE |               |

|                  |                |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN    |
| LEAD TREATMENT   | SOLDER PLATING |
| LEAD MATERIAL    | COPPER ALLOY   |
| PACKAGE MASS     | 0.2g           |

CXL5509P

16PIN DIP (PLASTIC)



Two kinds of package surface:

- 1.All mat surface type.
- 2.All mirror surface type.

PACKAGE STRUCTURE

|            |                      |
|------------|----------------------|
| SONY CODE  | DIP-16P-01           |
| EIAJ CODE  | DIP016-P-0300        |
| JEDEC CODE | Similar to MO-001-AE |

|                  |                |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN    |
| LEAD TREATMENT   | SOLDER PLATING |
| LEAD MATERIAL    | COPPER ALLOY   |
| PACKAGE MASS     | 1.0 g          |