HT6550
Super I/O Controller

Features

- 100% compatible to IBM PC AT/XT
- Fully uPD765b and IBM-BIOS compatible floppy disk controller
  - 48mA floppy drive interface buffers
  - Support two floppy drives with capability of supporting up to four drives with an external decoder
  - Support 360K/720K/1.2M/1.44M formats
  - Support 250Kb/s, 300Kb/s, 500Kb/s data rate
- Digital data separator eliminates critical analog adjustments
- Two 16450/8250 compatible UARTs
  - Independent control of transmit,receive,line status and data set interrupts on each channel
  - Individual modem control signals for each channel
  - Programmable serial interface characteristics for each channel:
    # 5-, 6-, 7-, or 8-bit characters
    # Even,odd or no parity bit generation and detection
    # 1-, 1.5-, or 2-stop bit generation
  - Programmable baud rate generator for each channel which allows division of the timing reference clock input by 1 to (2^{16}-1)
- Only one 24MHz crystal for FDC and UARTs
- One IBM PC AT/XT bidirection parallel port for printer
- One parallel bus mouse compatible to IBM, Logitech and Zwix Bus Mouse
- Support AT/XT Game port decode
- Support AT/XT hard disk IDE interface
- Hardware/software configuration setup available
- Individual disable feature available
- Power saving feature available
- 100 pin PQFP package

Applications

- Super (Multi) I/O interface card

General Description

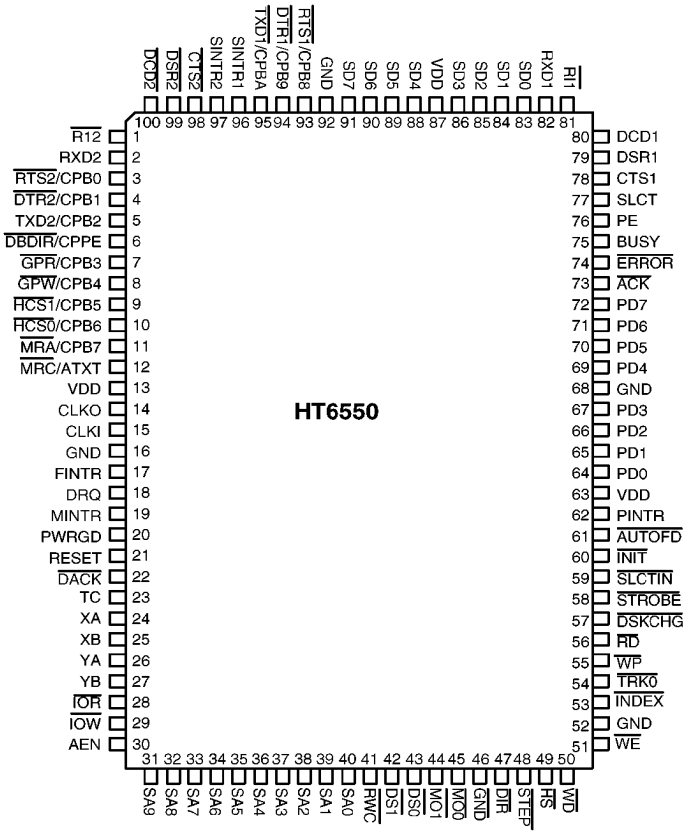
The HT6550 super Multi I/O chip, is an advanced CMOS single chip controller offering the complete I/O solutions for the IBM AT/XT environments. It incorporates one floppy disk controller (FDC), two full function UARTs, one parallel port, one bus mouse port, one game port controller, IDE hard disk drive interface, standard AT/XT address decoding for on-chip function and four configuration registers in one chip. It is fabricated with HOLTEK's high-reliability CMOS technology.

The HT6550 super Multi I/O chip contains one floppy disk controller which supports two floppy drives with capability of supporting up to four drives with an external decoder and is compatible to support 360K, 720K, 1.2M, 1.44M formats. Two full function UARTs of HT6550 which can be programmed serial interface characteristics for each channel, and a programmable baud rate generator is also included that can divide the timing reference clock input by a divisor between 1 and (2^{16}-1) and can produce a 16X clock for driving the internal transmitter logic. Provisions are also included to use this 16X clock to drive the receiver logic.

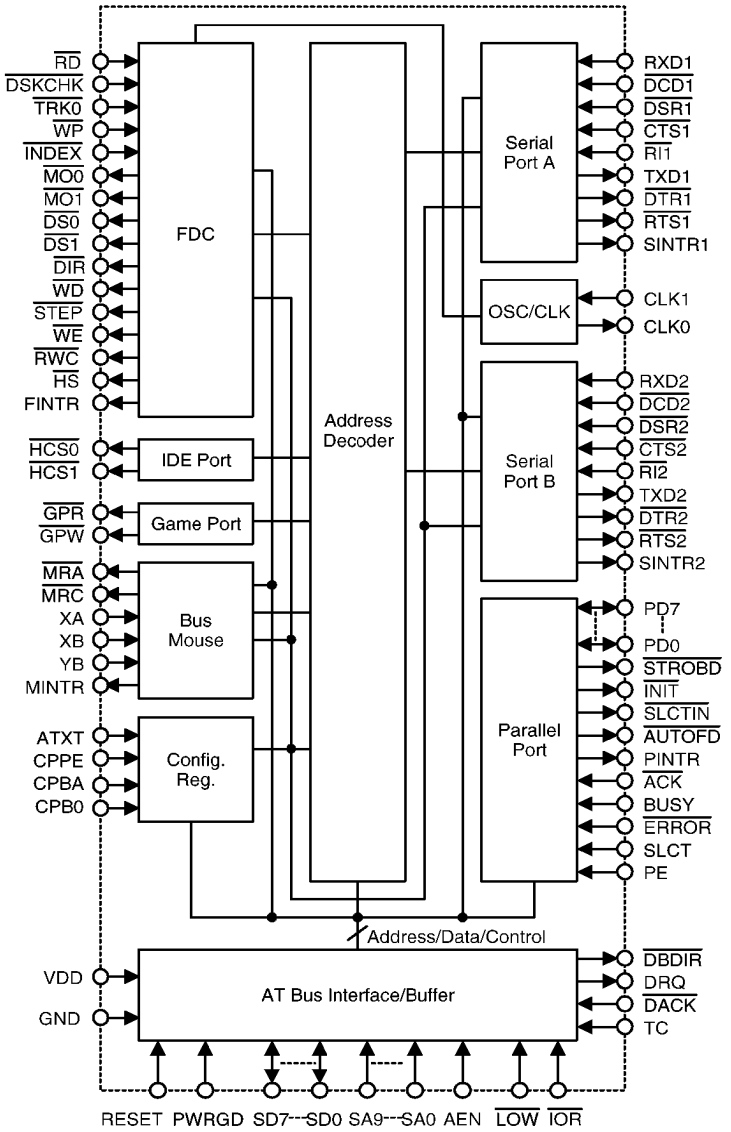
The HT6550 also contains one parallel Bus Mouse controller which is compatible to IBM, Logitech and Zwix Bus Mouse and works with any application software which uses the Microsoft concept. It supports all Bus Mouse signal transfers and 4 IRQ selections.

The IDE (Intelligent Drive Electronics) port of HT6550 decoding strobes IDE type Winchester drives and supports data buffer. The Game port controller decoding strobes Game port for read and write. The HT6550 has 4 very flexible and easy to select configuration registers. It will be also easy to enable or disable any supported functions. For a cost effective and space efficient design, the HT6550 is packaged in an industry standard 100-pin EIA-J PQFP package.

Pin Assignment



Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
Host Interface (30 pins)			
31~40	SA9~SA0	I	Host address bus
83~86, 88~91	SD0~SD7	I/O	Host data bus
28	$\overline{\text{IOR}}$	I	Active low I/O read
29	$\overline{\text{IOW}}$	I	Active low I/O write
21	RESET	I	Schmitt-trigger input reset from host
30	AEN	I	DMA address enable active high
22	$\overline{\text{DACK}}$	I	Active low DMA acknowledge from host
18	DRQ	O	DMA request to host
23	TC	I	Terminate DMA data transfer
19	MINTR	O	Mouse port interrupt request
17	FINTR	O	Floppy controller interrupt request
96	SINTR1	O	Serial port COM1 interrupt request
97	SINTR2	O	Serial port COM2 interrupt request
62	PINTR	O	Parallel port interrupt request
Parallel port Interface (17 pins)			
58	$\overline{\text{STROBE}}$	O	Data strobe, This signal indicates to the peripheral that the data at the parallel port is valid
59	$\overline{\text{SLCTIN}}$	O	Line printer select, This signal is used to select the printer when it is low
60	$\overline{\text{INIT}}$	O	Printer initialize, This signal initializes the printer when it is low
61	$\overline{\text{AUTOFD}}$	O	Autofeed, When this output is low the printer should automatically line feed after each line printed
73	$\overline{\text{ACK}}$	I	Acknowledge. This signal is set low by the printer to indicate that it has received data and is ready for next data
74	$\overline{\text{ERROR}}$	I	Printer error. This input is set by the printer when it has detected an error
75	BUSY	I	Printer busy. This input is set high by the printer when it can't accept another character
76	PE	I	Paper empty. This input is set high by the printer when it is out of paper

Pin No.	Pin Name	I/O	Description
77	SLCT	I	Printer select. This input is set by the printer when it is selected
64~67, 69~72	PD0~PD7	I/O	Parallel port data bus
Bus Mouse Controller (6 pins)			
24	XA	I	X-direction input from bus mouse
25	XB	I	X-direction input from bus mouse
26	YA	I	Y-direction input from bus mouse
27	YB	I	Y-direction input from bus mouse
11	$\overline{\text{MRA}}$/CPB7	I/O	During normal operation this pin is mouse port A read signal. When RESET is high this pin becomes CPB7 input and reads data for IDE hardware setup
12	$\overline{\text{MRC}}$/ATXT	I/O	During normal operation this pin is mouse port C read signal. When RESET is high this pin becomes AT/XT input and reads data for AT/XT mode selection, 1=AT mode, 0=XT mode
IDE Interface (2 pins)			
10	$\overline{\text{HCS0}}$/CPB6	I/O	During normal operation this pin is IDE port enable to enable 1F0-1F7H/170-177H (AT), 320-323H(XT) When RESET is high this pin becomes CPB6 input and reads data for FDC hardware setup
9	$\overline{\text{HCS1}}$/CPB5	I/O	During normal operation this pin is IDE port enable to enable 3F6-3F7H/376-377H When RESET is high this pin becomes CPB5 input and reads data for bus mouse hardware setup
Game port Interface (2 pins)			
7	$\overline{\text{GPR}}$/CPB3	I/O	During normal operation this pin is game port read signal When RESET is high this pin becomes CPB3 input and reads data for FDC, IDE hardware setup
8	$\overline{\text{GPW}}$/CPB4	I/O	During normal operation this pin is game port write signal When RESET is high this pin becomes CPB4 input and reads data for game port hardware setup
Floppy Interface (15 pins)			

Pin No.	Pin Name	I/O	Description
45	$\overline{MO0}$	O	FDD motor A enable, active low open drain output
44	$\overline{MO1}$	O	FDD motor B enable, active low open drain output
43	$\overline{DS0}$	O	FDD drive A enable, active low open drain output
42	$\overline{DS1}$	O	FDD drive B enable, active low open drain output
47	$\overline{DIR}$	O	Direction of the head stepper motor, open drain output, 1=outward, 0=inward motion movement
50	$\overline{WD}$	O	Write data, active low open drain output
48	$\overline{STEP}$	O	Step output pulses, active low open drain output
51	$\overline{WE}$	O	Enable write to FDD, active low open drain output
41	$\overline{RWC}$	O	Reduced write current, open drain output used to select the transfer rate, 0=250 Kb/s, 1=500 Kb/s
49	$\overline{HS}$	O	Head select, open drain output
56	$\overline{RD}$	I	Read data from FDD, schmitt-trigger input
57	$\overline{DSKCHG}$	I	Diskette change, schmitt-trigger input
54	$\overline{TRK0}$	I	Track 00, head is on track 0, schmitt-trigger input
55	$\overline{WP}$	I	Write protected, schmitt-trigger input
53	$\overline{INDEX}$	I	FDC index,indicates the beginning of a disk track
Serial port interface (16 pins)			
78	$\overline{CTS1}$	I	Serial 1 clear to send input, active low
79	$\overline{DSR1}$	I	Serial 1 data set ready input, active low
80	$\overline{DCD1}$	I	Serial 1 data carrier detect input, active low
81	$\overline{RI1}$	I	Serial 1 ring indicator input active low
82	RXD1	I	Serial 1 receive data input
93	$\overline{RTS1}$/CPB8	I/O	During normal operation this pin is serial 1 request to send. When RESET is high this pin becomes CPB8 input and reads data for UARTs hardware setup
94	$\overline{DTR1}$/CPB9	I/O	During normal operation this pin is serial 1 data terminal ready. When RESET is high this pin becomes CPB9 input and reads data for UARTs hardware setup

Pin No.	Pin Name	I/O	Description
95	TXD1/CPBA	I/O	During normal operation this pin is serial 1 transmit data. When RESET is high this pin becomes CPBA input and reads data for UARTs hardware setup
98	$\overline{\text{CTS2}}$	I	Serial 2 clear to send input, active low
99	$\overline{\text{DSR2}}$	I	Serial 2 data set ready input, active low
100	$\overline{\text{DCD2}}$	I	Serial 2 data carrier detect input, active low
1	$\overline{\text{RI2}}$	I	Serial 2 ring indicator input, active low
2	RXD2	I	Serial 2 receive data input
3	$\overline{\text{RTS2}}$/CPB0	I/O	During normal operation this pin is serial 2 request to send. When RESET is high this pin becomes CPB0 input and reads data for parallel port hardware setup
4	$\overline{\text{DTR2}}$/CPB1	I/O	During normal operation this pin is serial 2 data terminal ready. When RESET is high this pin becomes CPB1 input and reads data for parallel port hardware setup
5	TXD2/CPB2	I/O	During normal operation this pin is serial 2 transmit data. When RESET is high this pin becomes CPB2 input and reads data for parallel port hardware setup
Miscellaneous (12 pins)			
6	$\overline{\text{DBDIR}}$/CPPE	I/O	During normal operation this pin is data bus direction control sIgnal When RESET is high this pin becomes CPPE input and reads data for configuration setup select. 1=software setup, 0=hardware setup
20	PWRGD	I	HT6550 is fully function when PWRGD is high If PWRGD is low and VDD still active then HT6550 is isolated from the reset of the circuit, all inputs are disabled and all outputs tri-stated
15	CLKI	I	Oscillator input (24 MHz)
14	CLKO	O	Oscillator driver output
13,63,87	VDD	I	+5V supply
16,46,52, 68,92	GND	I	Ground

Absolute Maximum Ratings

Supply voltage.....–0.3V to 5.5V

Input/Output voltage.....V_{SS}—0.3 to V_{DD}+0.3

Storage temperature .....–50°C to 125°C

Operating temperature .....0°C to 70°C

Electrical Characteristics

DC Characteristics

(V_{DD}=5V, TA=25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Host Interface (SD0~SD7, DRQ, MINTR, FINTR, SINTR1, SINTR2 PINTR)						
V_{OLB}	Output Low Voltage	I_{OL}=10mA	—	—	0.4	V
V_{OHB}	Output High Voltage	I_{OH}=–2mA	2.4	—	V_{DD}	V
I_{LOB}	Leakage Current	V_{IN}=5V	—	—	10	μA
		V_{IN}=0V	—	—	–10	μA
Clock Input (CLKI)						
V_{ILX}	Clock Input Low Voltage	—	–0.3	—	0.8	V
V_{IHX}	Clock Input High Voltage	—	2	—	V_{DD}	V
Floppy Interface Output						
V_{OLF}	Output Low Voltage	I_{OL}=48mA	—	—	0.4	V
IDE Interface Output						
V_{OLH}	Output Low Voltage	I_{OL}=10mA	—	—	0.4	V
V_{OHH}	Output High Voltage	I_{OH}=–2mA	2.4	—	V_{DD}	V
I_{LOH}	Leakage Current	V_{IN}=V_{DD}	—	—	10	μA
I_{LOL}	Leakage Current	V_{IN}=0	—	—	–10	μA
Parallel Interface Output						
V_{OL}	Output Low Voltage	I_{OL}=10mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=–2mA	2.4	—	V_{DD}	V
Bus Mouse, Floppy Interface Input and RESET						
V_{ILM}	Input Low Voltage	—	–0.3	—	0.8	V
V_{IHM}	Input High Voltage	—	2.4	—	V_{DD}	V
V_H	Input Hysteresis	—	0.25	—	—	V
Game Port, Bus Mouse, UART Interface output and $\overline{DBDIR}$						
V_{OLG}	Output Low Voltage	I_{OL}=2mA	—	—	0.4	V
V_{OHG}	Output High Voltage	I_{OH}=–400μA	2.4	—	V_{DD}	V
All Other Input						
V_{IL}	Input Low Voltage	—	–0.3	—	0.8	V
V_{IH}	Input High Voltage	—	2.4	—	V_{DD}	V
V_{LIH}	Input Leakage Current	V_{IN}=V_{DD}	—	—	10	μA
V_{LIL}	Input Leakage Current	V_{IN}=0	—	—	–10	μA

AC Characteristics (V_{DD}=5V, TA=25°C)

• UART/PARALLEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{IRS}	Delay From Initial IRQ Reset To Transmit Start	—	1/16	—	8/16	Baud Rate
T_{STI}	Delay From Stop To Interrupt	—	9/16	—	—	Baud Rate
T_{HR}	Delay From $\overline{IOW}$ To Reset Interrupt	100pf Loading	—	—	175	ns
T_{SI}	Delay From Initial $\overline{IOW}$ To Interrupt	—	9/16	—	16/16	Baud Rate
T_{IR}	Delay From $\overline{IOR}$ To Reset	100pf Loading	—	—	1	ns
T_{SINT}	Delay From Stop To Set Interrupt		—	—	1/2	Baud Rate
T_{RINT}	Delay Form $\overline{IOR}$ Reset Interrupt	100pf Loading	—	—	250	ns
T_{MWO}	Delay From $\overline{IOW}$ To Output	100pf Loading	—	—	200	ns
T_{SIM}	Set Interrupt Delay From MODEM Input	100pf Loading	—	—	250	ns
T_{RIM}	Reset Interrupt Delay From $\overline{IOR}$	100pf Loading	—	—	250	ns
T_{OAD}	Interrupt Active Delay	100pf Loading	—	—	30	ns
T_{IID}	Interrupt Inactive Delay	100pf Loading	—	—	30	ns
N	Baud Rate Divisor	100pf Loading	—	—	2^{16}–1	unit

• FDC: Data rate= 500 /300 /250 KB/SEC

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{AR}	SA9–SA0, AEN, $\overline{DACK}$ Setup Time To $\overline{IOR}\downarrow$	—	25	—	—	ns
T_{RA}	SA9–SA0, AEN, $\overline{DACK}$ Hold Time From $\overline{IOR}\uparrow$	100pf Loading	0	—	—	ns
T_{RR}	IOR Width	100pf Loading	200	—	—	ns
T_{FD}	Data Access Time From $\overline{IOR}\downarrow$	100pf Loading	—	—	80	ns
T_{DH}	Data Hold Time From $\overline{IOR}\downarrow$	—	10	—		ns
T_{DF}	SD To Float From $\overline{IOR}\uparrow$	—	10	—	50	ns

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{RI}	IRQ Delay From $\overline{IOR}\uparrow$	—	—	—	360/ 570/ 675	ns
T_{AW}	SA9–SA0, AEN, $\overline{DACK}$ Setup Time To $\overline{IOW}\downarrow$	—	25	—	—	ns
T_{WA}	SA9–SA0, AEN, $\overline{DACK}$ Hold Time From $\overline{IOW}\uparrow$	—	0	—	—	ns
T_{WW}	$\overline{IOW}$ Width	—	200	—	—	ns
T_{DW}	Data Setup Time To $\overline{IOW}\uparrow$	—	60	—	—	ns
T_{WD}	Data Hold Time From $\overline{IOW}\uparrow$	—	0	—	—	ns
T_{WI}	IRQ Delay From $\overline{IOW}\uparrow$	—	—	—	360/ 570/ 675	ns
T_{MCY}	DMA Cycle Time	—	27	—	—	µs
T_{AM}	DMA Reset Delay Time From $\overline{DACK}\downarrow$	—	—	—	50	ns
T_{MA}	DRQ To $\overline{DACK}$ Delay	—	0	—	—	ns
T_{AA}	$\overline{DACK}$ Width	—	260/ 430/ 510	—	—	ns
T_{MR}	$\overline{IOR}$ Delay From DRQ	—	0	—	—	ns
T_{MW}	$\overline{IOW}$ Dleay From DRQ	—	0	—	—	ns
T_{MRW}	$\overline{IOW}$ Or $\overline{IOR}$ Response Time From DRQ	—	—	—	12/ 20 24	µs
T_{TC}	TC Width	—	135/ 220/ 260	—	—	ns
T_{RST}	RESET Width	—	1.8/ 3.0/ 3.5	—	—	µs
T_{IDX}	$\overline{INDEX}$ Width	—	0.5/ 0.9/ 1.0	—	—	µs
T_{DST}	$\overline{DIR}$ Setup Time To $\overline{STEP}$	—	1.0/ 1.6/ 2.0	—	—	µs

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{STD}	$\overline{DIR}$ Hold Time From $\overline{STEP}$	—	24/ 40/ 48	—	—	μs
T_{STP}	$\overline{STEP}$ Pulse Width	—	6.8/ 11.5/ 13.8	7.0/ 11.7/ 14	7.2/ 11.9/ 14.2	μs
T_{SC}	$\overline{STEP}$ Cycle Time	—	**	**	**	μs
T_{WDD}	$\overline{WD}$ Pulse Width	—	100/ 188/ 225	125/ 210/ 250	150/ 235/ 275	ns
T_{WPC}	Write Precompensation	—	100/ 138/ 225	125/ 210/ 250	150/ 235/ 275	μs

Notes:

* Typical nsvalues for TA=25°C and nominal value for supply voltage.

**Programmable from 2ms to 32ms in 2ms increments.

• Game port & bus mouse

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{GMRW}	Game Command delay time from RD/WR Game Port	—	—	150	ns
T_B	Bus Mouse delay time between XA (YA) AND XB (YB)	—	2.4	—	μs

Functional Description

I/O Port Address

Function	* Possible Port Address	Comment
Serial port 1	3F8—3FFH 3E8—3EFH	COM1 COM3
Serial port 2	2F8—2FFH 2E8—2EFH	COM2 COM4
Parallel port	3BC—3BFH 378—37BH 278—27BH	PRT1 PRT2 PRT3
FDC port	3F2, 3F4, 3F5, 3F7, 1F7H 372, 374, 375, 377, 177H	FDC1 FDC2
IDE port	1F0—1F7H, 3F6, 3F7H 170—177H, 376, 377H 320—323H	IDE1 (AT) IDE2 (AT) ** (XT)
Bus mouse port	23C—23EH	
Game port	201H	

* These ports are selected by configuration registers.
** AT/XT mode is selected by AT/XT (pin 12) during RESET.

• Configuration setup

There are four configuration registers CR # 00,01,02,0FH which are write only. CR# 00,01H can be either hardware or software setup, CR# 02, 0FH can only be accessed through software. Pin 6 CPPE is used to select hardware/software system setup during the RESET. Hardware setup when CPPE is low level and software setup when CPPE is high level.

* Hardware setup

CPPE low indicates hardware setup for CR# 00H and CR# 01H. During RESET goes high,the HT6550 will read the inputs from the following pins and setup the configuration registers CR# 00H and CR# 01H.

Pin Name	CPBA	CPB9	CPB8	CPB7	CPB6	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0
Pin No.	95	94	93	11	10	9	8	7	5	4	3

Note: CPBA–CPB8 : Serial port selection

CPBA	CPB9	CPB8	UART1	UART2
0	0	0	disable	disable
0	0	1	COM1 (3F8–3FFH)	disable
0	1	0	disable	COM2 (2F8–2FFH)
0	1	1	COM1 (3F8–3FFH)	COM2 (2F8–2FFH)
1	0	0	COM3 (3E8–3EFH)	COM4 (2E8–2EFH)
1	0	1	disable	COM1 (3F8–3FFH)
1	1	0	COM2 (2F8–2FFH)	disable
1	1	1	COM2 (2F8–2FFH)	COM1 (3F8–3FFH)

CPB7: IDE enable. 0=disable, 1=enable.
CPB6: FDC enable. 0=disable, 1=enable.
CPB5: MOUSE enable. 0=disable, 1=enable.
CPB4: GAME enable. 0=disable, 1=enable.
CPB3: Secondary IDE,FDC selection. 0=secondary selected, 1=primary selected.

CPB2: Printer mode selection 0=extended mode, 1=normal mode.
CPB1,0: Parallel port selection.

CPB1	CPB0	Parallel port
0	0	disable
0	1	PRT1 (3BC—3BFH)
1	0	PRT2 (378—37BH)
1	1	PRT3 (278—27BH)

* Software setup

CPPE high indicates software setup. After RESET the default values will be loaded into the configuration registers.
The procedures for setting up the configuration registers are described as follow:

- To enter configuration mode:
  # Write 55H to 2FAH.
  # Follow by writing AAH to 3FAH.
- To program configuration register:
  # Write XXH to 3FAH, where XXH is the configuration register index.
  # Follow by writing YYH to 2FAH, where YYH is the data for CR# XXH.
- To exit from configuration mode:
  # Write 0FH to 3FAH, then write any value YYH to 2FAH.
  # or write AAH to 3FAH.

The following describes the bit functions of each configuration registers (CR# 00, 01, 02 and 0FH)

* Configuration register — CR# 00H (write only)

Bit No.	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPB7	CPB6	CPB5	CPB4	CPB3	CBP2	CPB1	CPB0

Note:

CPB7: IDE enable. 0=disable, 1=enable (default).
CPB6: FDC enable. 0=disable, 1=enable (default).
CPB5: Mouse enable. 0=disable, 1=enable (default).
CPB4: GAME enable. 0=disable, 1=enable (default).
CPB3: Secondary IDE, FDC selection. 0=secondary selected, 1= primary selected (default).
CPB2: Printer mode selection. 0=extended mode, 1=normal mode (default).
CPB1,0: Parallel port selection.

CPB1	CPB0	Paralled port
0	0	disable
0	1	PRT1 (3BC–3BFH)
1	0	PRT2 (378–37BH) (default)
1	1	PRT3 (278–27BH)

* Configuration register — CR# 01H(Write only)

Bit No.	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	CPBA	CPB9	CPB8

Note: CPBA~CPB8: Serial port selection.

CPBA	CPB9	CPB8	UART1	UART2
0	0	0	disable	disable
0	0	1	COM1 (3F8–3FFH)	disable
0	1	0	disable	COM2 (2F8–2FFH)
0	1	1	COM1 (3F8–3FFH)(default)	COM2 (2F8–2FFH) (default)
1	0	0	COM3 (3E8–3EFH)	COM4 (2E8–2EFH)
1	0	1	disable	COM1 (3F8–3FFH)
1	1	0	COM2 (2F8–2FFH)	disable
1	1	1	COM2 (2F8–2FFH)	COM1 (3F8–3FFH)

* Configuration register — CR# 02H (Write only)

Bit No.	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENB	$\overline{\text{MPD}}$	$\overline{\text{PDD}}$	$\overline{\text{SPD}}$	$\overline{\text{FPD}}$	$\overline{\text{HPD}}$	$\overline{\text{GPD}}$	—

Where

ENB:	1=valid configuration setup
MPD:	Mouse port power down, 0=power down, 1=normal (default)
PDD:	Printer port power down, 0=power down, 1=normal (default)
SPD:	Serial port power down, 0=power down, 1=normal (default)
FPD:	Floppy disk port power down, 0=power down, 1=normal (default)
HPD:	IDE port power down, 0=power down, 1=normal (default)
GPD:	Game port power down,0=power down, 1=normal (default)

* Configuration register — CR# 0FH (Write only)
Writing any value to CR# 0FH can bring the HT6550 out of the configuration mode.

Serial port

The serial ports of HT6550 are fully compatible to the 16450/8250 ACE register. The programmable features allows data rates ranging from 50 baud to 56K baud; they also provide 5 to 8-bit character size with 1 start bit and 1/1.5/2 stop bits; even/odd/sticky/no parity of parity check; and prioritized interrupts.

There are three types of internal registers that used in each channel. They are control, status and data registers. The control registers are the Bit Rate Select Register DLL (Divisor latch LSB), DLM (Divisor latch MSB), LCR (Line Control Register), IER (Interrupt Enable Register), and MCR (Modem Control Register). The status registers are the LSR (Line Status Register) and MSR (Modem Status Register). The data registers are the RBR (Receiver Buffer Register) and the THR (Transmitter Holding Register). The divisor latch access bit (DLAB) in the Line Control Register (LCR) is used to decide which register to be accessed during a read or write operation. See Table 1 for the details.

The Transmitter Buffer Register (TBR) and Receiver Buffer Register (RBR) are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The data registers of HT6550 are double-buffered so that all read, write operations and serial-to-parallel, paralled-to-serial conversion can be performed at the same time.

DLAB	COM1	COM2	COM3	COM4	Read	Write
0	3F8H	2F8H	3E8H	2E8H	RBR	THR
0	3F9H	2F9H	3E9H	2E9H	IER	IER
0	3FAH	2FAH	3EAH	2EAH	IIR	—
X	3FBH	2FBH	3EBH	2EBH	LCR	LCR
X	3FCH	2FCH	3ECH	2ECH	MCR	MCR
X	3FDH	2FDH	3EDH	2EDH	LSR	LCR
X	3FEH	2FEH	3EEH	2EEH	MSR	MSR
X	3FFH	2FFH	3EFH	2EFH	SCR	SCR
1	3F8H	2F8H	3E8H	2E8H	DLL	DLL
1	3F9H	2F9H	3E9H	2E9H	DLM	DLM

X: means “don’t care”

Table 1. Serial Channel Internal Registers

• Line control register (LCR)

The system programmer specifies the format of the asynchronous data communication exchange through the Line Control Register and sets the Divisor latch access bit via the Line Control Register (LCR). In addition to controlling the format, the programmer may be read the contents of the Line Control Register for inspection. The contents of the LCR are described as follow.

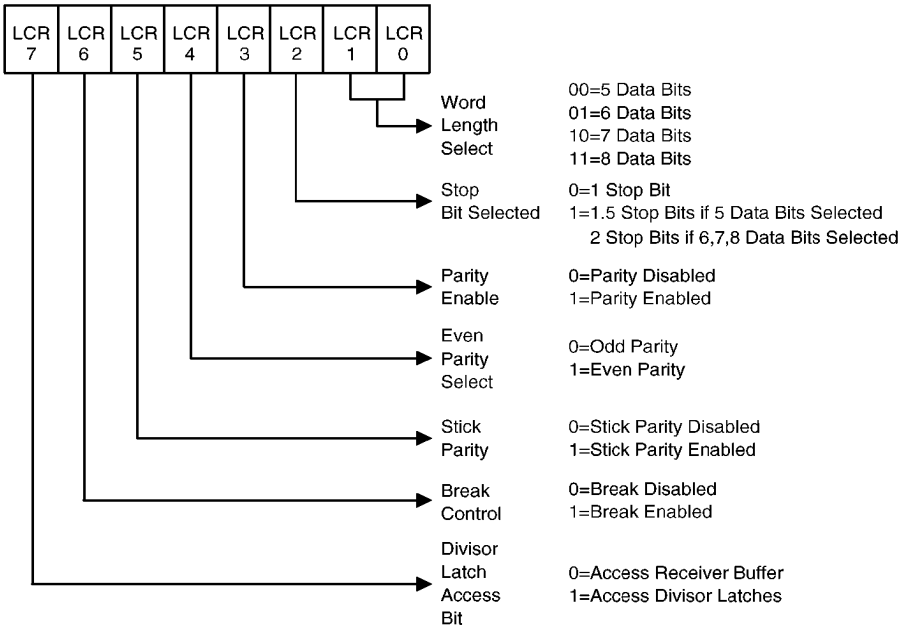


Figure 1. Line Control Register

Note:

LCR(0~1): Specify the number of bits in each serial character that is sent or received. The encoding of LCR(0) and LCR(1) is as follows:

LCR (1)	LCR (0)	Word Length
0	0	5
0	1	6
1	0	7
1	1	8

LCR(2): Specifies the number of stop bits in each serial character that is sent or received. If LCR(2) is in logic 0, one stop bit is generated or checked in the data sent or received. If LCR(2) is logic 1 when a 5-bit word length is selected through LCR(0) and LCR(1), one and a half stop bits are generated or checked. If LCR(2) is in logic 1 when either a 6, 7, or 8-bit word length is selected, 2 stop bits are generated or checked.

LCR(3): Specifies the parity enable. When LCR(3) is logic 1, a parity bit is generated (transmit data mode) or checked (receive data mode) between the last data word and stop bit of the serial data.

Note: The parity bit is used to productan even or odd number of 1's when the data-word bits and parity bit are summed.

LCR(4): Specifies the even parity select. When LCR(3) is in logic 1 and LCR(4) is in logic 0, an odd number of logic 1's is sent or checked in the data word bits and parity bit. When LCR(3) is in logic 1 and LCR(4) is in logic 1, an even number of logic 1's is sent or checked.

LCR(5): Specifies the stick parity. When LCR(3) is in logic 1 and LCR(5) is in logic 1, the parity bit is sent and then detected by the receiver as logic 0, if LCR(4) is in logic 1; or detected by the receiver as logic 1, if LCR(4) is in logic 0. If LCR(5) is in logic 0. Stick Parity is disabled.

LCR(6): Specifies the break control. When LCR(6) is set to a logic 1, the transmit data (TXD) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic 0. The Break Control bit acts only on TXD and has no effect on the transmitter logic. Break Control enables the CPU to alter a terminal in a computer communications system.

LCR(7): Specifies the divisor latch access bit (DLAB). This bit must be set to high to gain access to the divisor latches of the baud rate generator during a read or write operation. It must be set to low to gain access to the receiver buffer, the transmitter holding register, or the interrupt enable register.

- Line status register (LSR)

  The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the HT6550. The contents of the Line Status Register are described as below:

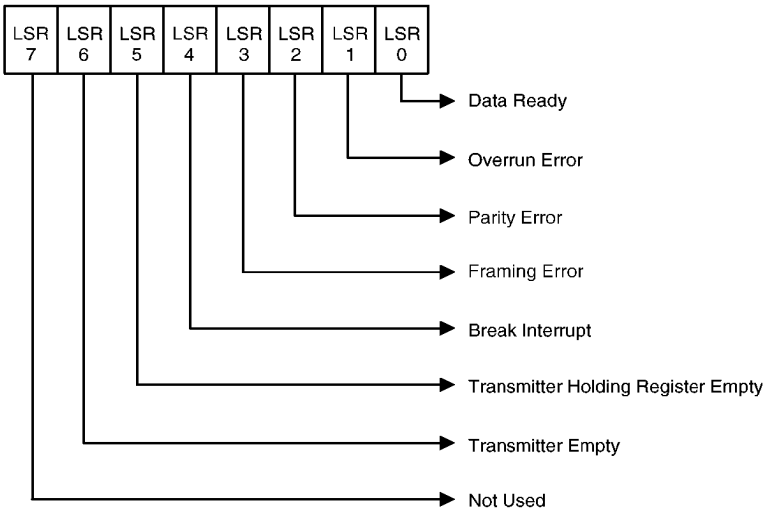


Figure 2. Line Status Register

Note:

LSR(0): This bit is the receiver data ready (DR) indicator. It is set to logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer register. Bit 0 may be reset to logic 0 by the processor reading the data in the receiver buffer register.

LSR(1): This bit is the overrun error (OE) indicator. It indicates that data in the Receiver Buffer Register was not read by the processor before the next character was transferred into the register, thereby destroyed previous character. The OE indicator is reset whenever the processor reads the contents of the line status Register.

LSR(2): This bit is the parity error (PE) indicator. It indicates the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit LCR(4). The PE bit is set to logic 1 upon detection of a parity error, and is reset to logic 0 whenever the processor reads the contents of the Line Status Register.

LSR(3): This bit is the framing error (FE) indicator. It indicates the received character does not have a valid stop bit. LSR(3) is set to logic 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(4): This bit is the break interrupt (BI) indicator. It is set to logic 1 whenever the received data input is held in the spacing state (logic 0) for longer than a full word transmission time (total time of the start bit+data bits+parity+stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(5): This bit is the Transmitter Holding Register Empty (THRE) indicator. It indicates that the UART is ready to accept a new character for transmission. The LSR(5) bit is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset to logic 0 by loading the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR. In addition, this bit causes the HT6550 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high in Interrupt Enable Register (IER).

LSR(6): This bit is the Transmitter Empty (TEMT) indicator. LSR(6) is set to logic 1 when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset to logic 0 when a character is loaded into the TSR. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is not used and always 0.

- Modem control register (MCR)

  The Modem Control Register (MCR) controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the Modem Control Register are described as follow:

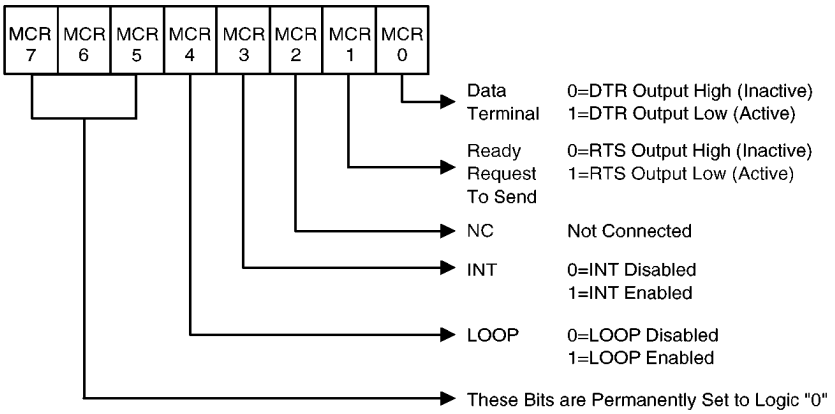


Figure 3. Modem Control Register

Note:

MCR(0): This bit controls the $\overline{\text{DTR}}$ output. When MCR(0) is set to logic 1, the $\overline{\text{DTR}}$ output is forced low. When MCR(0) is reset to logic 0, the $\overline{\text{DTR}}$ output is forced inactive. The $\overline{\text{DTR}}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the MODEM or data set.

MCR(1): This bit controls the $\overline{\text{RTS}}$ output. MCR(1) forces the $\overline{\text{RTS}}$ output in a manner identical to that described above for MCR(0).

MCR(2): This bit is not connected.

MCR(3): The enable of the interrupt output can be set to an active state by programming this bit to a logic 1.

MCR(4): This bit provides a local loop back feature for diagnostic testing of the channel. When MCR(4) is set high, Serial output (TXD) is set to the marking state (logic "1"), and the receiver data input Serial input (RXD) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three MODEM control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, and $\overline{\text{RI}}$) are disconnected. The MODEM control outputs ($\overline{\text{DTR}}$ and $\overline{\text{RTS}}$) are internally connected to associated bits in Modem Control Register. The MODEM control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Bits MCR(5)~MCR(7): These bits are permanently set to logic 0.

- Modem status register (MSR)

  The MSR provides the CPU with status of the modem input lines from the MODEM or peripheral devices. The MSR allows the CPU to read each of the several channel modem signal inputs by accessing the data bus interface of the HT6550 in addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta starts bits are set high when a control input from the MODEM changes state, and reset low when the CPU reads the MSR.

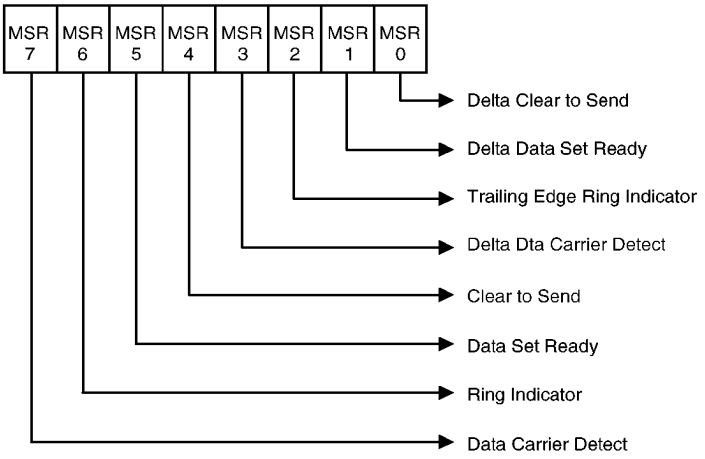


Figure 4. Modem Status Register

Note:

MSR(0): This bit is the delta clear to send (DCTS) indicator. It indicates the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the processor.

MSR(1): This bit is the delta data set ready (DDSR) indicator. It indicates the $\overline{DSR}$ input to the chip has changed state since last time it was read by the processor.

MSR(2): This bit is the trailing edge ring indicator (TERI). It indicates that the $\overline{RI}$ input to the serial channel has changed state from low to high since last time it was read by the CPU.

MSR(3): This bit is the delta data carrier detect (DDCD) indicator. It indicates the $\overline{DCD}$ input to the serial channel has changed state the last time it was read by the CPU.

MSR(4): This bit is the opposite of the $\overline{CTS}$ input. If MCR(4) of the MCR is set to a logic 1, this bit is equivalent to RTS of the MCR. It is the status of the CTS input from the modem indicating to the serial channel that the MODEM is ready to receive data from the serial channel's transmitter output (TXD).

MSR(5): This bit is the opposite of the $\overline{DSR}$ input. If MCR(4) of the MCR is set to a logic 1, this bit is equivalent to DTR of the MCR. It is a status of the DSR input from the MODEM to the serial channel which indicates that the MODEM is ready to provide received data to the serial channel receiver circuit.

MSR(6): This bit is the opposite of the $\overline{RI}$ input. It indicates the status to the $\overline{RI}$ input. If MCR(4) of the MCR is set to a logic 1, this bit is not connected in the MCR.

MSR(7): This bit is the opposite of the $\overline{DCD}$ input. If MCR(4) of MCR is set to a logic 1, this bit is equivalent to INT of the MCR.

- Interrupt identification register (IIR)

The Interrupt Identification Register (IIR) of each serial channel of the HT6550 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are listed as follows:

* Receiver Line Status (Priority 1)
* Received Data Ready (Priority 2)
* Transmitter Holding Register Empty (Priority 3)
* Modem Status (Priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

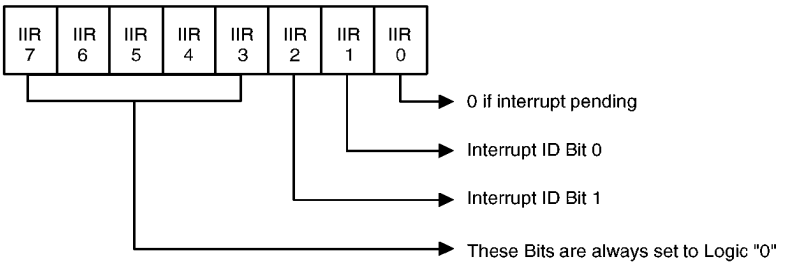


Figure 5. Interrupt Identification Register

Note:

IIR(0): This bit can be used in either a hard–wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is logic 0, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is logic 1, no interrupt is pending, and polling continues.

IIR(1)~(2): These two bit identify the pending interrupt that has the highest priority, as shown in Table 2 below.

IIR(3)~(7): These five bits are always logic 0.

Interrupt Identification				**Interrupt Set and Reset Functions**		
Bit2	Bit1	Bit0	Priority Level	Interrupt Flag	Interrupt Flag	Interrupt Reset Control
X	X	1		None	None	None
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the interrupt Source or THR write
0	0	0	Fourth	Modem Status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, $\overline{DCD}$	MSR Read

x=Not Defined.

Table 2. Interrupt Identification Register

- Interrupt enable register (IER)

  The Interrupt Enable Register (IER) is used to independently enable the four serial channel interrupts which activate the interrupt (SINTR1 or SINTR2) output. All interrupts are disable by resetting IER(0)~IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the SINTR1 or SINTR2 output signal. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are described below.

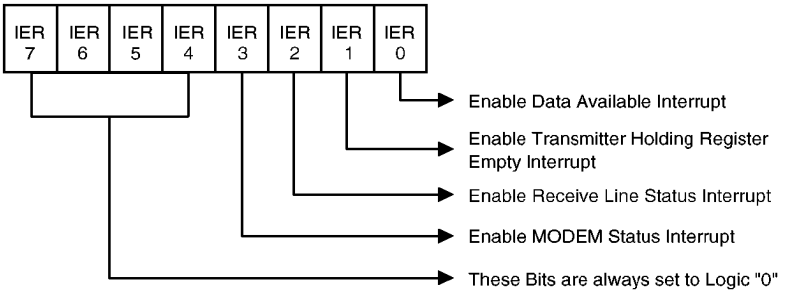


Figure 6. Interrupt Enable Register

Note:

IER(0): When this bit is set to logic 1, it enables the Receive Data Available Interrupt.

IER(1): When this bit is set to logic 1, it enables the Transmitter Holding Register Empty Interrupt.

IER(2): When this bit is set to logic 1, it enables the Receive Line Status Interrupt.

IER(3): When this bit is set to logic 1, it enables the Modem Status Interrupt.

IER(4)~(7): These four bits are always set to logic 0.

The table below summarize all serial channel registers:

Reg.	Register Bit Number							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
RBR (R)	Data Bit7 (MSB)	Data Bit6	Data Bit5	Data Bit4	Data Bit3	Data Bit2	Data Bit1	Data Bit0 (LSB)*
THR (W)	Data Bit7	Data Bit6	Data Bit5	Data Bit4	Data Bit3	Data Bit2	Data Bit	Data Bit0
DLL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DLM	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

Reg.	Register Bit Number							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Intertupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Receiver Data Available Interrupt
IIR (R)	0	0	0	0	0	Interrupt ID Bit(1)	Interrupt ID Bit(0)	"0" if Interrupt Pending
LCR	(DLAB) Divisor Latch Access bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit1	(WLSB0) Word Length Select Bit0
MCR	0	0	0	Loop	Interrupt	Not Connected	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

(W): Write only.
(R): Read only.
LSB Data Bit 0 is the first bit transmitted or received.

Table 3. Serial Channel Accessible Registers

• Baud rate generator (BRG)

The Baud Rate Generator is used to generate the 16X baud rate for the UART function. It is obtained by dividing the timing reference clock input by a divisor between 1 and (2^{16}–1) which is programmable by two divisor latches: DLM and DLL. The HT6550 uses 24MHz to generate the 1.8432MHz timing reference frequency. With the frequencies, standard bit rate from 50 to 38.5 Kb/s are available. Table 4 illusrates the divisors needed to obtain standard rates using a baud rate generator with crystal frequency of 1.8432MHz. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	–
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Table 4. Baud Rate Using 1.8432MHz.

• Reset

After power on,the RESET input of the HT6550 should be held low for 500 ns to reset the HT6550 circuits to an idle mode until initialization. The effects of a reset on the HT6550 are summarized in Table 5.

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All Bits Low
Interrupt Identification Register	Reset	Bit 0 is high and Bits 1–7 are low
Line Control Register	Reset	All Bits Low
Line Status Register	Reset	Bits 5, 6 are high, others are low
Modem Status Register	Reset	Bits 0–3 low, Bits 4–7 input signais
TXD1, TXD2	Reset	High
$\overline{\text{RTS0}}$, $\overline{\text{RTS1}}$, $\overline{\text{DTR0}}$, $\overline{\text{DTR1}}$	Reset	High

Table 5. Reset Control of Register and Pinout Signals

• Programming

Each serial channel of the HT6550 is programmed by the control registers LCR, IER, DLL, DLM and MCR. These control words define the length of character, number of stop bits, parity, baud rate, and MODEM interface. While the control registers can be written in any order, the IER should be written to last, because it controls the interrupt enables. Once a serial channel is programmed and operated, these registers can be updated any time the HT6550 serial channel is not transmitting or receiving data.

- Software reset

  A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a software reset consists of writing to the LCR, Divisor Latches, and MCR registers.

  The LSR and RBR registers should be read prior to enable interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operations.

Printer port (parallel port)

The printer port of HT6550 interfaces the device to a Centronics-type printer. When $\overline{\text{SLCTIN}}$ (pin 59) is low, the printer port is selected. The printer port is compatible to the IBM PC/AT printer port. When printer port is disabled, all outputs and register contents are preserved. In power down mode, all register are accessible but the input signals are tri-stated.

Upon power up the control signals are inactive, the data register is cleared and the status register reflects the status. There are three registers of printer port, the Data Register, Status Register and Control Register. They are listed in Table 6 and are described individually as following.

PRT1	PRT2	PRT3	Read	Write
3BCH	378H	278H	Data Register	Data Register
3BDH	379H	279H	Status Register	—
3BEH	37AH	27AH	Control Register	Control Register

Table 6. Printer Port Registers Address

- Data register

  The data written to this register is transmitted to the printer. Data read from this register is identical to that which was last written.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Note :

Bit0~7: These 8 bits provide the data bits of printer port to be write in and read out.

- Status register

  Parallel port status Register is a read only register that provides the CPU to read the status of the printer. These bits are described as below.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUSY	$\overline{\text{ACK}}$	PE	SLCT	$\overline{\text{ERROR}}$	—	—	—

Note :

Bit0~2: These three bits are not used.

Bit3: This bit is an error indicator. When this bit is a logic 0, it means that the printer has encountered are error condition.

Bit4: This bit is a select indicator. When this bit is a logic 1, it means that the printer is selected.

Bit5: This bit is a paper empty indicator. When this bit is a logic 1, it means that the printer has detected the empty of paper.

Bit6: This bit represents the current state of the printer's $\overline{ACK}$ signal. When this bit is a logic 0, it means that the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{BUSY}$ stops.

Bit7: This bit become logic 0 during data entry, when the printer is off–line during printing, or when the print head is changing position or in an error state. When Bit7 is logic 0, the printer is busy and can not accept data.

• Control register

Printer control register is a read/write register that provides the CPU to send the information or command to the printer. These bits are described as below.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	$\overline{POE}$	PINTEN	SLCTIN	$\overline{INIT}$	AUTOFD	STROBE

Note :

Bit0: This bit represents the strobe signal. When this bit is a logic 1, it generates $\overline{STROBE}$ signal. A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microsecond before and after the strobe pulse.

Bit1: This bit represents the auto line–feed signal. When this bit is a logic 1, it causes the printer to line–feed after a line is printed.

Bit2: This bit represents the printer initialize signal. When this bit is a logic 0, it initializes the printer.

Bit3: This bit represents the printer selected signal. When this bit is a logic 1, it means that the printer is selected.

Bit4: This bit is the parallel interrupt enable signal. When this bit is a logic 1, it generates an interrupt when $\overline{ACK}$ change from low state to high state.

Bit5: This bit is the direction control bit. When this bit is a logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when this bit is a logic 0, they work as a printer port. This bit is used only in extended mode.

Bit6~7 These two bits are not used.

The above three registers are summarized in the following table (Table 7).

	Register Bit Number							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	—	—	—
Control	—	—	$\overline{POE}$	PINTEN	SLCTIN	$\overline{INIT}$	AUTOFD	STROBE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table 7. Printer Port Registers

Game port

The Game Port of HT6550 is located at 201H. The $\overline{GPR}$ and $\overline{GPW}$ signals of HT6550 together with the standard AT data signals (D7~D0) comprised the required interface signals to implement the game port.

Bus mouse controller

The Bus Mouse port of HT6550 is located at 23C~23FH. It is compatible to IBM, Logitech and Zwix Bus Mouse. The Bus Mouse can select system interrupt IRQ 2, 3, 4 and 5. Each one can be chosen as the interrupt signal by setting corresponding Jumper in hardware configuration.

Users may use the Mouse Controller on different types of computers without any conflict with other serial ports or I/O Controllers which also issue interrupts. The Bus Mouse port of HT6550 includes three registers, the Mouse Input Register, Mouse Control Register, and Mouse Control Port. They are described as follows.

- Mouse input register

The Mouse Input Register is a read-only register and is located at 23CH. The contents of the Mouse Input Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LB	MB	RB	—	CNT3	CNT2	CNT1	CNT0

Note :

Bit0~3: These four bits represent a 4-bits counter. These 4 bits store the Mouse Displacement Counter data.

Bit4: This bit is reserved and not used.

Bit5: This bit is a Right Button input indicator.

Bit6: This bit is a Middle Button input indicator.

Bit7: This bit is a Left Button input indicator.

- Mouse control register

The Mouse Control Register is also a read–only register and is located at 23EH. It indicates which interrupt request is used. The contents of the Mouse Control Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	—	IRQ2	IRQ3	IRQ4	IRQ5

Note :

Bit0: This bit is a interrupt request 5 indicator. When this bit is a logic 1, it means that Bus Mouse uses interrupt request 5 (IRQ5).

Bit1: This bit is a interrupt request 4 indicator. When this bit is a logic 1, it means that Bus Mouse uses interrupt request 4 (IRQ4).

Bit2: This bit is a interrupt request 3 indicator. When this bit is a logic 1, it means that Bus Mouse uses interrupt request 3 (IRQ3).

Bit3: This bit is a interrupt request 2 indicator. When this bit is a logic 1, it means that Bus Mouse uses interrupt request 2 (IRQ2).

Bit4~7: These four bits are used as Mouse Control Port, and will describe in “Mouse Control Port” for details.

• Mouse control port

The Mouse Control Port is a write-only port and is located at 23EH. It is used to latch counter data and reset counter, to select low 4 bits or high 4 bits for X-axis or Y-axis Counter. The contents of the Mouse Control Port are described as below :

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDCNT	MS1	MS0	$\overline{\text{MINTE}}$	—	—	—	—

Note :

Bit0~3: These four bits are used as Mouse Control Register, and are described in "Mouse Control Register" above.

Bit4: This bit is an interrupt enable signal. When this bit is a logic 0, it will enable the interrupt.

Bit5~6: These two bits are used to select one of the four combinations of 4-bits counter data. When one of the four combinations is selected, the value of counter will be read through low bits of address 23CH (Bit0~3 of Mouse Input Register).

These four combination are as follows:

Bit6	Bit5	Selected Counter Data
0	0	Low 4 bits of X-axis Counter
0	1	High 4 bits of X-axis Counter
1	0	Low 4 bits of Y-axis Counter
1	1	High 4 bits of Y-axis Counter

Bit7: This bit is used to latch counter data and reset counter. When this bit is a logic 1, it will latch the counter data that are read into Bit0~3 of Mouse Input Register. When this bit is a logic 0, it will reset the counter.

Floppy disk controller (FDC)

The Floppy Disk Controller of HT6550 supports up to four floppy disk drives. It is compatible with the IBM system 34 double density format (MFM), and Sony EMCA format. Using a 24MHz crystal input, the HT6550 generates 8MHz and 4MHz to handle standard data rates of 500 and 250 Kb/s and 4.8MHz to support a 300 Kb/s data rate. The Floppy Disk Controller of HT6550 also contains a Data separator. The Data separator uses the Digital Phase Lock Loop (DPLL) approach and is designed to address high performance error rates on floppy disk drives. The HT6550 FDC is capable of performing the following 15 different commands:

- READ DATA
- READ DELETED DATA
- WRITE DATA
- WRITE DELETED DATA
- READ A TRACK
- READ ID
- FORMAT A TRACK
- SCAN EQUAL
- SCAN LOW OR EQUAL
- SCAN HIGH OR EQUAL
- RECALIBRATE
- SENSE INTERRUPT STATUS
- SPECIFY
- SENSE DEVICE STATUS
- SEEK

There are 5 types of register contained in the HT6550 they are described individually as follows.

- FDC operation register (digital output register)

The FDC Operation Register (or Digital Output Register) is an writeonly register that controlling the drive motors, drive selection, and feature enable. It is located at address 3F2H/372H, all bits are cleared by the I/O interface reset line. The contents of the FDC Operation Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	MO1	MO0	DMAEN	$\overline{\text{SRST}}$	—	DS0

Note :

Bit0: This bit is a drive select signal. When this bit is a logic 0, the drive A is selected. When this bit is a logic 1, the drive B is selected.

Bit1: This bit is reserved.

Bit2: This bit is a soft reset signal. When this bit is a logic 0, the diskette function will be reset.

Bit3: This bit is a DMA enable signal. When this bit is a logic 1, it will enable diskette interrupts and DMA.

Bit4: This bit is a Drive A Motor Enable signal. When this bit is a logic 1, it enables the Motor of Drive A.

Bit5: This bit is a Drive B Motor Enable signal. When this bit is a logic 1, it enables the Motor of Drive B.

Bit6~7: These two bits are reserved.

- Digital input register

The Digital Input Register is a an 8-bit, read-only register used for the purposes of diagnosis. It is located at address 3F7H/377H. The contents of the Digital Input Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DSKCHG	—	—	—	—	—	—	—

Note :

Bit0~6: These seven bits are not used in the read-only register.

Bit7: This bit is floppy disk change status indicator. When this bit is a logic 1, it means that the floppy diskette in the floppy disk drive has been changed.

• FDC control register (transfer rate register)

The FDC Control Register (or Transfer Rate Register) is a 2-bit, write-only register. It controls a programmable divider and provides 8M/4.8M/4MHz clocks for three different data transfer rates (500K b/s, 300Kb/s and 250Kb/s). It is located at address 3F7H/377H. The contents of the FDC Control Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	—	—	—	RS1	RS0

Note :

Bit0~1: These two bits are used to select the transfer rate and control the reduce write current.

The relationship of these two bits, transfer rate, clock rate, and reduce write current enable are summarized in the following table:

Bit1	Bit0	Transtar Rates	Clock Rates	Reduce Write
0	0	500k bps	8 MHz	0
0	1	300k bps	4,8 MHz	1
1	0	250k bps	4 MHz	1
1	1	reserved	reserved	1

Bit2~7: These six bits are not used in the write-only register.

• FDC data register

The FDC Data Register actually consists of several registers in a stack and only one register is presented to the data bus at a time when storing data commands and parameters, or providing diskette-drive status informations. It is located at address 3F5H/375H. The contents of the FDC data Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Note :

Bit0~7: These eight bits are used to store the data of FDC.

- FDC main staus register

The FDC Main Status Register indicates the status of the flopp disk controller. It is a 8-Bit, Read-Only register and located at addres 3F4H/374H. The contents of the FDC Main Status Register are described as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RQM	DIO	EXM	FCB	FB3	FB2	FB1	FB0

Note :

Bit0~3: These four bits are floppy disk drive busy indicators. When one of Bit0~3 is a logic 1, it indicates that floppy disk drive 0~3 is busy respectively and will not accept READ or WRITE command.

Bit4: This bit is a FDC busy indicator. When this bit is a logic 1, it means that a READ or WRITE command is in progress.

Bit5: This bit is a Non-DMA Mode indicator. This bit is set only during execution phase in non-DMA mode. When this bit goes low, execution phase has ended and result phase has started.

Bit6: This bit is a Data Input/Output indicator. It indicates the transfer direction between the FDC and the processor. When this bit is a logic 0, the transfer direction is from the data register to the processor. When this bit is a logic 1, the transfer direction is from the processor to the data register.

Bit7: This bit is a Request for master indicator. When this bit is a logic 1, it indicates that the data register is ready to send or receive data.

IDE controller

The IDE controller of HT6550 provides the $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$ control signals for the IDE interface and the IDE buffer. It supports 8-bit or 16-bit programmed I/O. The $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$ control signals are described as follows.

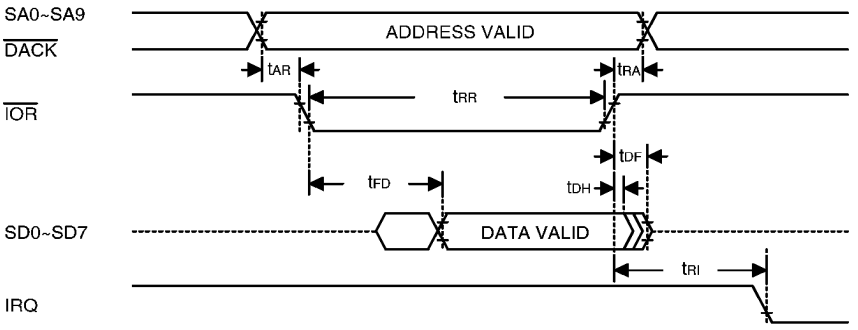
$\overline{\text{HCS0}}$: This is a hard disk chip select signal
decodes 1F0–1F7H /170–177H (AT)
decodes 320~323H (XT)

$\overline{\text{HCS1}}$: This is a floppy disk chip select signal
decodes 3F6~3F7H/376~377H (AT)
decodes 3F1H (XT).

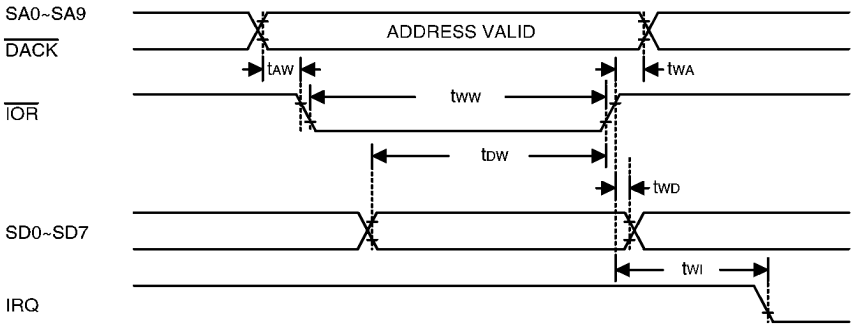
Timing Diagram

FDC

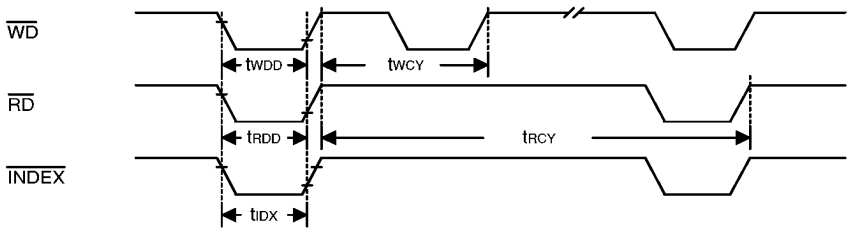
• Processor read operation



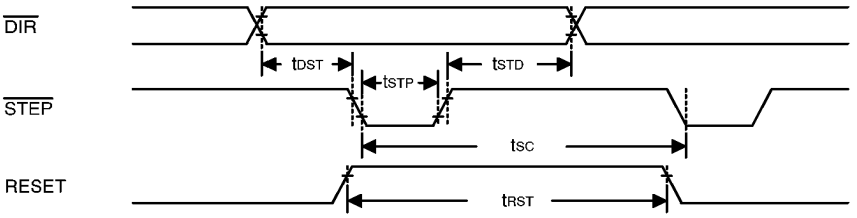
• Processor write operation



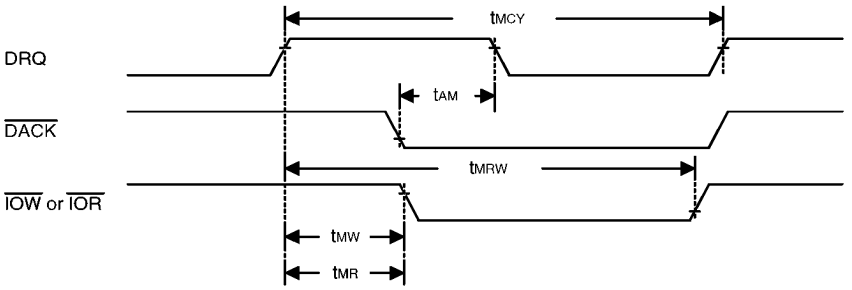
• FDD write/read operation



• Seek operation

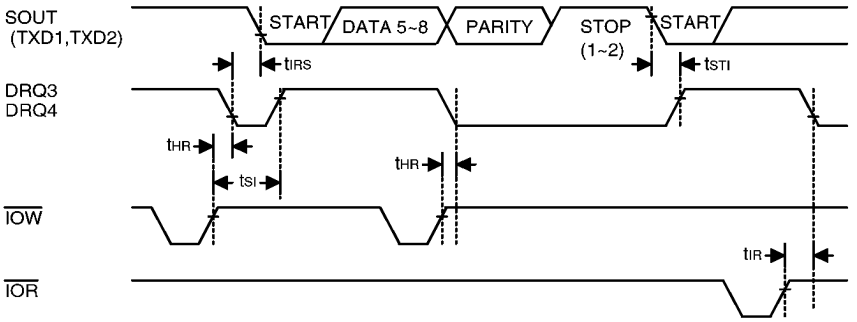


• DMA operation

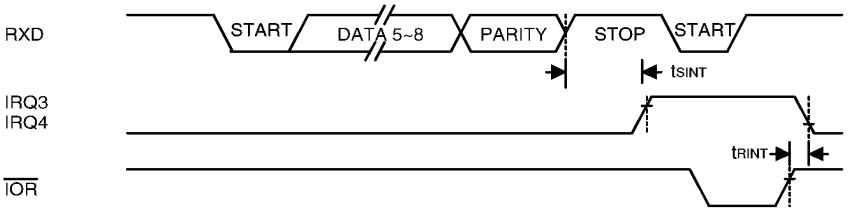


UART/Parallel port

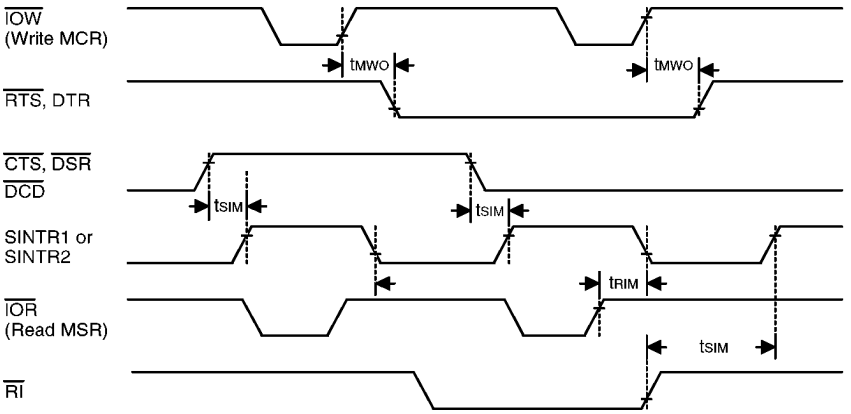
• Transmitter timing



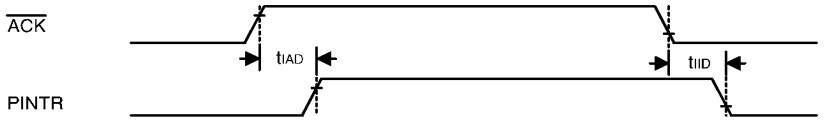
- Receiver timing



- MODEM control timing

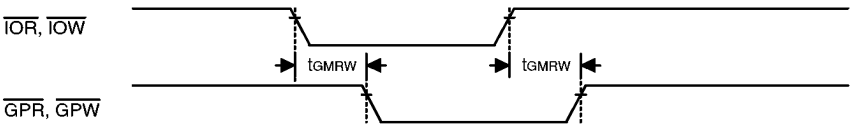


- Printer interrupt timing

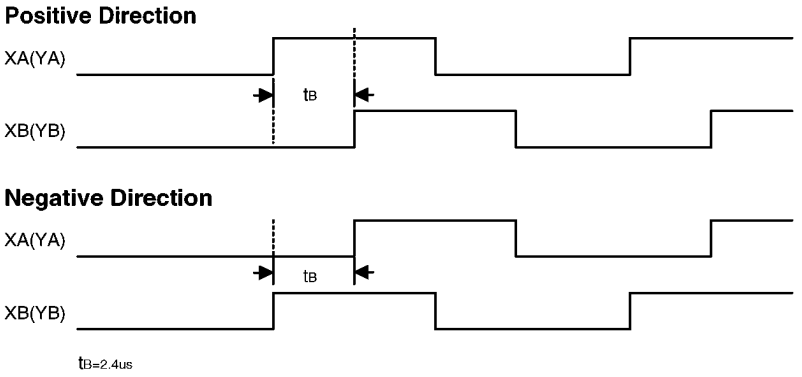


Game port & Bus mouse

• Game port



• Bus mouse



Application Circuit