Integrated Circuit Systems, Inc.

ICS9169-03

High-Drive Clock Generator for Personal Computers

General Description

The **ICS9169-03** generates all clocks required for high speed microprocessor systems based on the latest processors. Three standard CPU frequencies and 5% frequency (turbo) modes are externally selectable with smooth frequency transitions. These frequencies can be customized for specific applications. A test and tristate mode are provided to drive all clocks directly.

High drive BCLK outputs provide greater than 1V/ns slew rate into 30pF loads. PCLK outputs provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle.

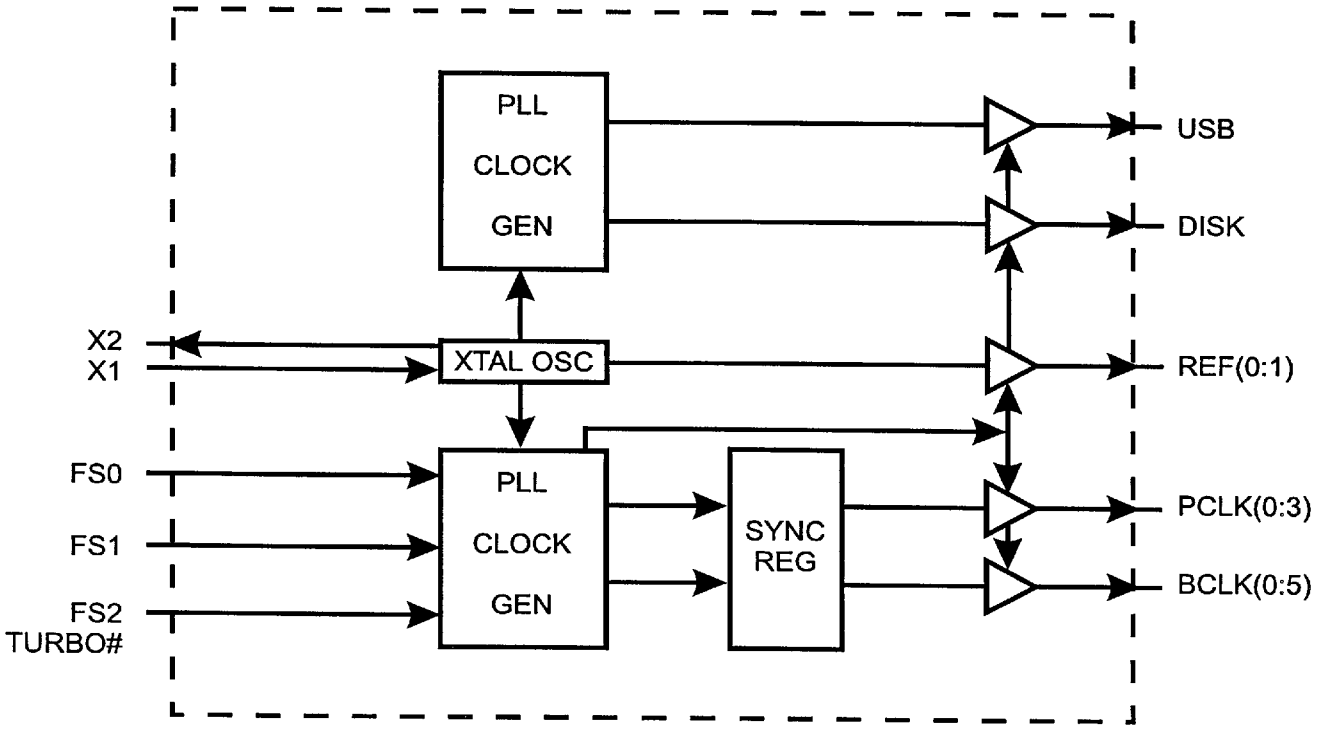
Features

- 5% accelerated CPU and BUS clock mode
- Generates 4 early processor and 6 bus clocks, plus USB, disk and 2 reference clocks
- Processor clocks early by 3±2ns
- Synchronous clocks skew matched to ±200ps
- Test clock and tristate modes ease system design and test
- Outputs drive 30pF with 1V/ns slew
- Custom configurations available
- 3.0V - 5.5V supply range
- 28-pin SOIC or SSOP package

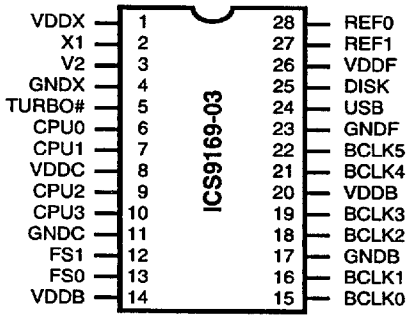
Applications

- Ideal for high speed PC systems

Block Diagram



Pin Configuration



28-Pin SOIC

Functionality

3.0 - 5.5V, 0-70^{0}C

TURBO#	FS1	FS0	X1, REF (MHz)	PCLK(0:3) (MHz)	BCLK(0:5) (MHz)	USB, DISK (MHz)
0	0	0	14.318	52.5	26.3	48, 24
0	0	1	14.318	70.0	35.0	48, 24
0	1	0	14.318	63.0	31.5	48, 24
0	1	1	Tristate	Tristate	Tristate	Tristate
1	0	0	14.318	50.0	25.0	48, 24
1	0	1	14.318	66.6	33.3	48, 24
1	1	0	14.318	60.0	30.0	48, 24
1	1	1	TCLK	TCLK/2	TCLK/4	TCLK/2, /4

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDX	PWR	Power for oscillator.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 MHz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4	GNDX	PWR	Ground for oscillator.
5	TURBO#	IN	Accelerates CPU & BUS clocks. This input has an internal pull-up device.
6, 7, 9, 10	PCLK(0:3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
8	VDDF	PWR	Power for fixed (DISK & USB) clock output buffers.
11	GNDC		Ground for CPU clock output buffers.
12, 13	FS(0:1)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull-up devices.
14, 20	VDDB	PWR	Power for BUS clock output buffers.
15, 16, 18, 19, 21, 22	BCLK(0:5)	OUT	Bus clock outputs are fixed at one half the PCLK frequency.
17	GNDB	PWR	Ground for BUS clock output buffers.
23	GNDF	PWR	Ground for fixed frequency output buffers.
24	USB	OUT	The USB clock is fixed at 48 MHz (with 14.318 MHz input).
25	DISK	OUT	The DISK controller clock is fixed at 24 MHz (with 14.318 MHz input).
26	VDD	PWR	Power for fixed frequency output buffers.
28, 27	REF(0:1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Note: BCLK buffers cannot be supplied with 5 volts (Pins 14 and 20) if CPU and fixed frequencies (Pins 1, 8 and 26) are being supplied with 3.3 volts.

Absolute Maximum Ratings

Supply Voltage 7.0V

Logic Inputs ..... GND –0.5V to V_{DD} +0.5V

Ambient Operating Temperature ..... 0 to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 –70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-28.0	-10.5	-	µA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for PCLKS & BCLKS	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V; for PCLKS & BCLKS	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for PCLKS & BCLKS	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA; for PCLKS & BCLKS	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.5 MHz; all outputs unloaded	-	55	110	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 –70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% PCLK & BCLK	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% PCLK & BCLK	-	1.4	2.4	ns
Duty Cycle[1]	D_t	20pF load @ V_{OUT}=1.4V	45	50	55	%
Jitter, One Sigma[1]	T_{jis1}	PCLK & BCLK Clocks; Load=20pF, FOUT>25 MHz	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK Clocks; Load=20pF, FOUT>25 MHz	-250	-	250	ps
Jitter, One Sigma[1]	T_{jis2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1 st crossing of 66.5 MHz V_{DD} supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0V

V_{DD} = 4.5 - 5.5 V, T_A = 0-70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.4	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-45	-15	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	µA
Output Low Current1	I_{OL}	V_{OL}=0.8V; for PCLKS & BCLKS	36.0	62.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for PCLKS & BCLKS	-	-152	-90.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	30.0	50.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-110.0	-65.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=20mA; for PCLKS & BCLKS	-	0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-70mA; for PCLKS & BCLKS	2.4	4.0	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for fixed CLKs	-	0.2	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-50mA; for fixed CLKs	2.4	4.7	-	V
Supply Current	I_{DD}	@66.5 MHz; all outputs unloaded	-	80.0	160.0	mA

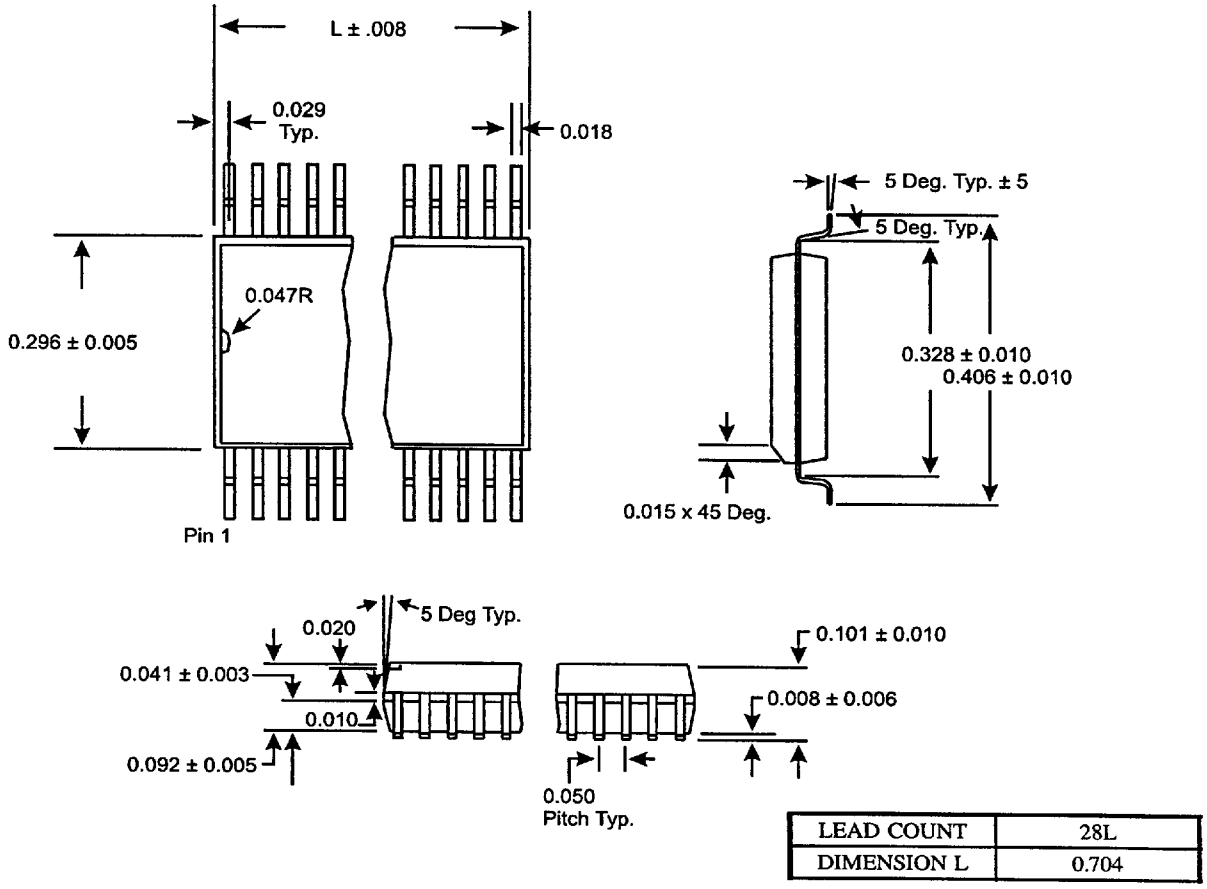
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0V

V_{DD} = 4.5 - 5.5 V, T_A = 0-70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.55	0.95	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.52	0.90	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% PCLK & BCLK	-	1.2	2.1	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% PCLK & BCLK	-	1.1	2.0	ns
Duty Cycle[1]	D_{t1}	20pF load @ V_{OUT}=1.4V	52	57	62	%
Duty Cycle[1]	D_{t2}	20pF load @ V_{OUT}=50%	45	50	55	%
Jitter, One Sigma[1]	T_{jis1}	PCLK & BCLK Clocks; Load=20pF, R_S=33W FOUT>25 MHz	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK Clocks; Load=20pF, R_S=33W FOUT>25 MHz	-250	-	250	ps
Jitter, One Sigma[1]	T_{jis2}	Fixed CLK; Load=20pF R_S=33W	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF R_S=33W	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1st crossing of 66.5 MHz V_{DD} supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



LEAD COUNT	28L
DIMENSION L	0.704

SOIC Package

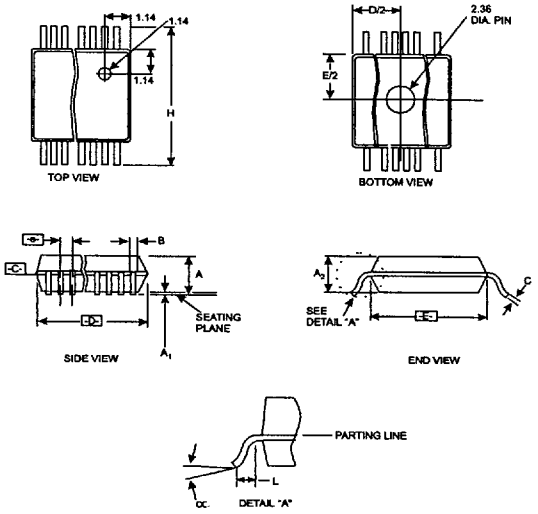
Ordering Information

ICS9169M-03

Example:

ICS XXXX M- PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	0.068	0.073	0.078	AA	0.239	0.244	0.249	14
A1	0.002	0.005	0.008	AB	0.239	0.244	0.249	16
A2	0.066	0.068	0.070	AC	0.278	0.284	0.289	20
B	0.010	0.012	0.015	AD	0.318	0.323	0.328	24
C	0.005	0.006	0.008	AE	0.397	0.402	0.407	28
D	See Variations			AF	0.397	0.402	0.407	30
E	0.205	0.209	0.212					
e		0.026 BSC						
H	0.301	0.307	0.311					
L	0.022	0.030	0.037					
N	See Variations							
∝	0°	4°	8°					

SSOP Package

This table in inches.

Ordering Information

ICS9169F-03

Example:

ICS XXXX M- PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device