

ASSP

# Dual Serial Input PLL Frequency Synthesizer

## MB15F74UL

### ■ DESCRIPTION

The Fujitsu MB15F74UL is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 4000 MHz and a 2000 MHz prescalers. A 64/65 or a 128/129 for the 4000 MHz prescaler, and a 32/33 or a 64/65 for the 2000 MHz prescaler can be selected for the prescaler that enables pulse swallow operation.

The BiCMOS process is used, as a result a supply current is typically 9.0 mA at 3.0 V. The supply voltage range is from 2.7 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial date. The pin assignments are the same as MB15F78UL. Fast locking is achieved for adopting the new circuit.

The new package (BCC20) decreases a mount area of MB15F74UL more than 30% comparing with the former BCC16 (for dual PLL).

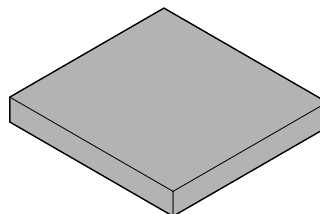
### ■ FEATURES

- High frequency operation : RF synthesizer : 4000 MHz Max  
: IF synthesizer : 2000 MHz Max
- Low power supply voltage :  $V_{CC} = 2.7$  to 3.6 V
- Ultra low power supply current :  $I_{CC} = 9.0$  mA Typ  
( $V_{CC} = V_p = 3.0$  V,  $T_a = +25$  °C,  $SW_{IF} = SW_{RF} = 0$  in IF/RF locking state)

*(Continued)*

### ■ PACKAGE

20-pad plastic BCC



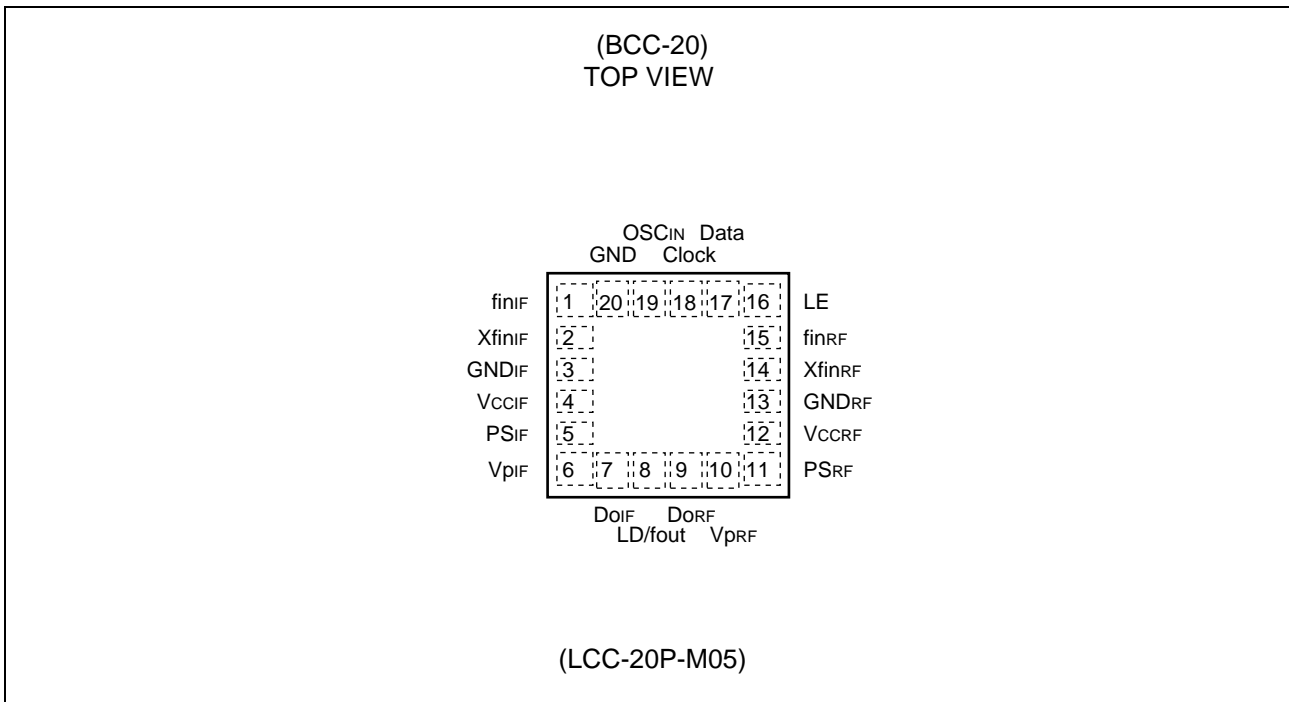
(LCC-20P-M05)

# MB15F74UL

(Continued)

- Direct power saving function : Power supply current in power saving mode  
Typ 0.1  $\mu$ A ( $V_{CC} = V_p = 3.0$  V,  $T_a = +25$  °C)  
Max 10  $\mu$ A ( $V_{CC} = V_p = 3.0$  V)
- Software selectable charge pump current : 1.5 mA/6.0 mA Typ
- Dual modulus prescaler : 4000 MHz prescaler (64/65 or 128/129) /2000 MHz prescaler (32/33 or 64/65)
- 23 bit shift register
- Serial input binary 14-bit programmable reference divider : R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter : 0 to 127
  - Binary 11-bit programmable counter : 3 to 2,047
- Built-in high-speed tuning, low-noise phase comparator, current-switching type constant current circuit
- On-chip phase control for phase comparator
- On-chip phase comparator for fast lock and low noise
- Built-in digital locking detector circuit to detect PLL locking and unlocking
- Operating temperature :  $T_a = -40$  °C to  $+85$  °C

## ■ PIN ASSIGNMENTS

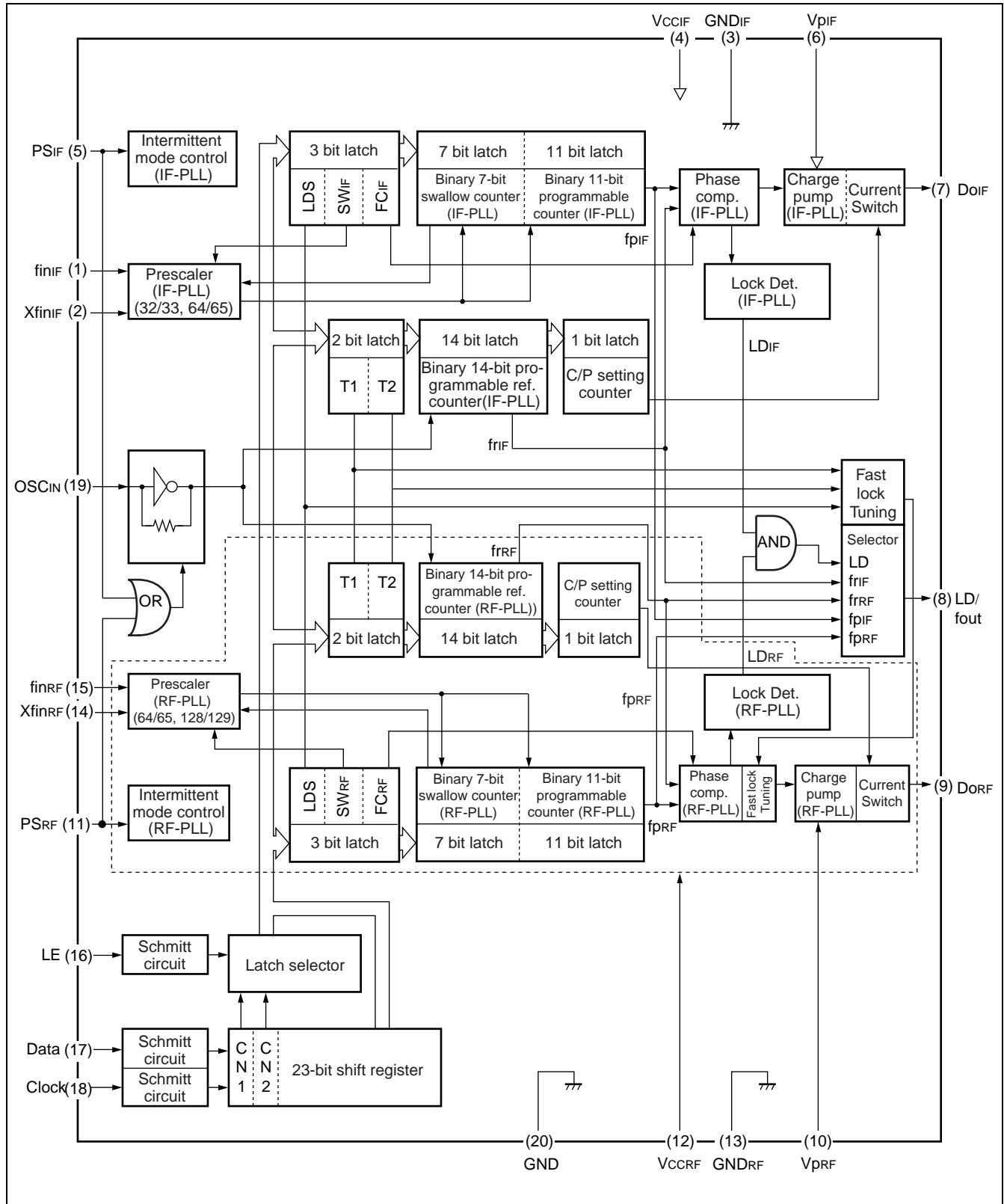


## ■ PIN DESCRIPTION

| Pin no. | Pin name           | I/O | Descriptions   |
|---------|--------------------|-----|--|
| 1       | fin <sub>IF</sub>  | I   | Prescaler input pin for the IF-PLL.<br>Connection to an external VCO should be AC coupling.  |
| 2       | Xfin <sub>IF</sub> | I   | Prescaler complimentary input for the IF-PLL section.<br>This pin should be grounded via a capacitor.  |
| 3       | GND <sub>IF</sub>  | —   | Ground pin for the IF-PLL section.   |
| 4       | V <sub>CCIF</sub>  | —   | Power supply voltage input pin for the IF-PLL section (except for the charge pump circuit) , the shift register and the oscillator input buffer.   |
| 5       | PS <sub>IF</sub>   | I   | Power saving mode control pin for the IF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.)<br>PS <sub>IF</sub> = “H” ; Normal mode/PS <sub>IF</sub> = “L” ; Power saving mode  |
| 6       | V <sub>pIF</sub>   | —   | Power supply voltage input pin for the IF-PLL charge pump.   |
| 7       | DO <sub>IF</sub>   | O   | Charge pump output for the IF-PLL section.   |
| 8       | LD/fout            | O   | Lock detect signal output (LD) /phase comparator monitoring output (fout) pin. The output signal is selected by LDS bit in a serial data.<br>LDS bit = “H” ; outputs fout signal/LDS bit = “L” ; outputs LD signal               |
| 9       | DO <sub>RF</sub>   | O   | Charge pump output for the RF-PLL section.   |
| 10      | V <sub>pRF</sub>   | —   | Power supply voltage input pin for the RF-PLL charge pump.   |
| 11      | PS <sub>RF</sub>   | I   | Power saving mode control for the RF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited. )<br>PS <sub>RF</sub> = “H” ; Normal mode/PS <sub>RF</sub> = “L” ; Power saving mode     |
| 12      | V <sub>CCRF</sub>  | —   | Power supply voltage input pin for the RF-PLL section (except for the charge pump circuit)   |
| 13      | GND <sub>RF</sub>  | —   | Ground pin for the RF-PLL section  |
| 14      | Xfin <sub>RF</sub> | I   | Prescaler complimentary input pin for the RF-PLL section.<br>This pin should be grounded via a capacitor.  |
| 15      | fin <sub>RF</sub>  | I   | Prescaler input pin for the RF-PLL.<br>Connection to an external VCO should be via AC coupling.  |
| 16      | LE                 | I   | Load enable signal input pin (with the schmitt trigger circuit)<br>When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.                       |
| 17      | Data               | I   | Serial data input pin (with the schmitt trigger circuit)<br>Data is transferred to the corresponding latch (IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data. |
| 18      | Clock              | I   | Clock input pin for the 23-bit shift register (with the schmitt trigger circuit)<br>One bit data is shifted into the shift register on a rising edge of the clock.   |
| 19      | OSC <sub>IN</sub>  | I   | The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.  |
| 20      | GND                | —   | Ground pin for OSC input buffer and the shift register circuit.  |

# MB15F74UL

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter            | Symbol     | Rating   |                | Unit |
|----------------------|------------|----------|----------------|------|
|                      |            | Min      | Max            |      |
| Power supply voltage | $V_{CC}$   | -0.5     | 4.0            | V    |
|                      | $V_p$      | $V_{CC}$ | 4.0            | V    |
| Input voltage        | $V_i$      | -0.5     | $V_{CC} + 0.5$ | V    |
| Output voltage       | LD/fout    | GND      | $V_{CC}$       | V    |
|                      | DOIF, DORF | GND      | $V_p$          | V    |
| Storage temperature  | $T_{stg}$  | -55      | +125           | °C   |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter             | Symbol   | Value    |     |          | Unit | Remarks               |
|-----------------------|----------|----------|-----|----------|------|-----------------------|
|                       |          | Min      | Typ | Max      |      |                       |
| Power supply voltage  | $V_{CC}$ | 2.7      | 3.0 | 3.6      | V    | $V_{CCRF} = V_{CCIF}$ |
|                       | $V_p$    | $V_{CC}$ | 3.0 | 3.6      | V    |                       |
| Input voltage         | $V_i$    | GND      | —   | $V_{CC}$ | V    |                       |
| Operating temperature | $T_a$    | -40      | —   | +85      | °C   |                       |

Note : •  $V_{CCRF}$ ,  $V_{PRF}$ ,  $V_{CCIF}$  and  $V_{PIF}$  must supply equal voltage.

Even if either RF-PLL or IF-PLL is not used, power must be supplied to  $V_{CCRF}$ ,  $V_{PRF}$ ,  $V_{CCIF}$  and  $V_{PIF}$  to keep them equal.

It is recommended that the non-use PLL is controlled by power saving function.

- Although this device contains an anti-static element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device.
  - When storing and transporting the device, put it in a conductive case.
  - Before handling the device, confirm the (jigs and) tools to be used have been uncharged (grounded) as well as yourself. Use a conductive sheet on working bench.
  - Before fitting the device into or removing it from the socket, turn the power supply off.
  - When handling (such as transporting) the device mounted board, protect the leads with a conductive sheet.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB15F74UL

## ■ ELECTRICAL CHARACTERISTICS

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

| Parameter                     | Symbol                 | Condition   | Value   |                    |     | Unit               |               |
|-------------------------------|------------------------|---|---|--------------------|-----|--------------------|---------------|
|                               |                        |   | Min   | Typ                | Max |                    |               |
| Power supply current          | $I_{CCIF}^{*1}$        | $f_{inIF} = 2000\text{ MHz}$<br>$V_{CCIF} = V_{pIF} = 3.0\text{ V}$ | 2.1   | 2.5                | 3.2 | mA                 |               |
|                               | $I_{CCRF}^{*1}$        | $f_{inRF} = 2500\text{ MHz}$<br>$V_{CCRF} = V_{pRF} = 3.0\text{ V}$ | 5.7   | 6.5                | 8.4 | mA                 |               |
| Power saving current          | $I_{PSIF}$             | $PS_{IF} = PS_{RF} = \text{"L"}$                                    | —   | $0.1^{*2}$         | 10  | $\mu\text{A}$      |               |
|                               | $I_{PSRF}$             | $PS_{IF} = PS_{RF} = \text{"L"}$                                    | —   | $0.1^{*2}$         | 10  | $\mu\text{A}$      |               |
| Operating frequency           | $f_{inIF}^{*3}$        | $f_{inIF}$  | IF PLL  | 200                | —   | 2000               | MHz           |
|                               | $f_{inRF}^{*3}$        | $f_{inRF}$  | RF PLL  | 2000               | —   | 4000               | MHz           |
|                               | $OSC_{IN}$             | $f_{OSC}$   | —   | 3                  | —   | 40                 | MHz           |
| Input sensitivity             | $f_{inIF}$             | $P_{finIF}$   | IF PLL, $50\ \Omega$ system   | -15                | —   | +2                 | dBm           |
|                               | $f_{inRF}$             | $P_{finRF}$   | RF PLL, $50\ \Omega$ system   | -10                | —   | +2                 | dBm           |
| Input available voltage       | $OSC_{IN}$             | $V_{OSC}$   | —   | 0.5                | —   | $V_{CC}$           | $V_{P-P}$     |
| "H" level input voltage       | Data LE                | $V_{IH}$  | Schmitt trigger input   | $0.7 V_{CC} + 0.4$ | —   | —                  | V             |
| "L" level input voltage       | Clock                  | $V_{IL}$  | Schmitt trigger input   | —                  | —   | $0.3 V_{CC} - 0.4$ | V             |
| "H" level input voltage       | $PS_{IF}$              | $V_{IH}$  | —   | $0.7 V_{CC}$       | —   | —                  | V             |
| "L" level input voltage       | $PS_{RF}$              | $V_{IL}$  | —   | —                  | —   | $0.3 V_{CC}$       | V             |
| "H" level input current       | Data LE                | $I_{IH}^{*4}$   | —   | -1.0               | —   | +1.0               | $\mu\text{A}$ |
| "L" level input current       | Clock PS               | $I_{IL}^{*4}$   | —   | -1.0               | —   | +1.0               | $\mu\text{A}$ |
| "H" level input current       | $OSC_{IN}$             | $I_{IH}$  | —   | 0                  | —   | +100               | $\mu\text{A}$ |
| "L" level input current       |                        | $I_{IL}^{*4}$   | —   | -100               | —   | 0                  | $\mu\text{A}$ |
| "H" level output voltage      | LD/<br>$f_{out}$       | $V_{OH}$  | $V_{CC} = V_p = 3.0\text{ V}$ , $I_{OH} = -1\text{ mA}$                         | $V_{CC} - 0.4$     | —   | —                  | V             |
| "L" level output voltage      |                        | $V_{OL}$  | $V_{CC} = V_p = 3.0\text{ V}$ , $I_{OL} = 1\text{ mA}$                          | —                  | —   | 0.4                | V             |
| "H" level output voltage      | $DO_{IF}$              | $V_{DOH}$   | $V_{CC} = V_p = 3.0\text{ V}$ , $I_{DOH} = -0.5\text{ mA}$                      | $V_p - 0.4$        | —   | —                  | V             |
| "L" level output voltage      | $DO_{RF}$              | $V_{DOL}$   | $V_{CC} = V_p = 3.0\text{ V}$ , $I_{DOL} = 0.5\text{ mA}$                       | —                  | —   | 0.4                | V             |
| High impedance cutoff current | $DO_{IF}$<br>$DO_{RF}$ | $I_{OFF}$   | $V_{CC} = V_p = 3.0\text{ V}$<br>$V_{OFF} = 0.5\text{ V to }V_p - 0.5\text{ V}$ | —                  | —   | 2.5                | nA            |
| "H" level output current      | LD/<br>$f_{out}$       | $I_{OH}^{*4}$   | $V_{CC} = V_p = 3.0\text{ V}$   | —                  | —   | -1.0               | mA            |
| "L" level output current      |                        | $I_{OL}$  | $V_{CC} = V_p = 3.0\text{ V}$   | 1.0                | —   | —                  | mA            |

(Continued)

(Continued)

( $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ )

| Parameter                | Symbol                             | Condition   | Value        |      |      | Unit |    |
|--------------------------|------------------------------------|---|--------------|------|------|------|----|
|                          |                                    |   | Min          | Typ  | Max  |      |    |
| “H” level output current | DoIF <sup>*8</sup><br>DoRF         | I <sub>DOH</sub> <sup>*4</sup><br>$V_{CC} = V_p = 3.0\text{ V}$ ,<br>$V_{DOH} = V_p / 2$ ,<br>$T_a = +25\text{ }^\circ\text{C}$ | CS bit = “H” | -8.2 | -6.0 | -4.1 | mA |
|                          |                                    |   | CS bit = “L” | -2.2 | -1.5 | -0.8 | mA |
| “L” level output current | DoIF <sup>*8</sup><br>DoRF         | I <sub>DOL</sub><br>$V_{CC} = V_p = 3.0\text{ V}$ ,<br>$V_{DOL} = V_p / 2$ ,<br>$T_a = +25\text{ }^\circ\text{C}$               | CS bit = “H” | 4.1  | 6.0  | 8.2  | mA |
|                          |                                    |   | CS bit = “L” | 0.8  | 1.5  | 2.2  | mA |
| Charge pump current rate | I <sub>DOL</sub> /I <sub>DOH</sub> | I <sub>DOMT</sub> <sup>*5</sup><br>$V_{DO} = V_p / 2$   | —            | 3    | 10   | %    |    |
|                          | vs V <sub>DO</sub>                 | I <sub>DOVD</sub> <sup>*6</sup><br>$0.5\text{ V} \leq V_{DO} \leq V_p - 0.5\text{ V}$   | —            | 10   | 15   | %    |    |
|                          | vs T <sub>a</sub>                  | I <sub>DOTA</sub> <sup>*7</sup><br>$-40\text{ }^\circ\text{C} \leq T_a \leq 85\text{ }^\circ\text{C}$ ,<br>$V_{DO} = V_p / 2$   | —            | 5    | 10   | %    |    |

\*1 : Conditions ; fosc = 12.8 MHz, T<sub>a</sub> = +25 °C, SW = “L” in locking state.

\*2 : V<sub>CCIF</sub> = V<sub>pIF</sub> = V<sub>CCRF</sub> = V<sub>pRF</sub> = 3.0 V, fosc = 12.8 MHz, T<sub>a</sub> = +25 °C, in power saving mode.

PS<sub>IF</sub> = PS<sub>RF</sub> = GND

V<sub>IH</sub> = V<sub>CC</sub>, V<sub>IL</sub> = GND (at CLK, Data, LE)

\*3 : AC coupling. 1000 pF capacitor is connected under the condition of Min operating frequency.

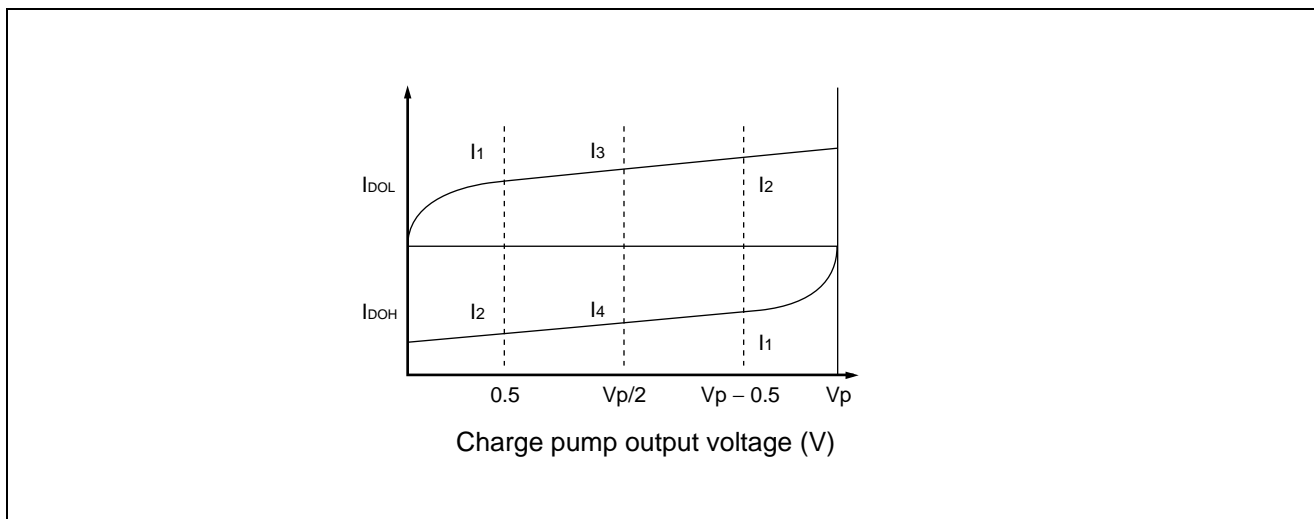
\*4 : The symbol “-” (minus) means the direction of current flow.

\*5 :  $V_{CC} = V_p = 3.0\text{ V}$ ,  $T_a = +25\text{ }^\circ\text{C}$   $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100\text{ }(\%)$

\*6 :  $V_{CC} = V_p = 3.0\text{ V}$ ,  $T_a = +25\text{ }^\circ\text{C}$   $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100\text{ }(\%)$  (Applied to both I<sub>DOL</sub> and I<sub>DOH</sub>)

\*7 :  $V_{CC} = V_p = 3.0\text{ V}$ ,  $[|I_{DO} (+85\text{ }^\circ\text{C})| - |I_{DO} (-40\text{ }^\circ\text{C})|] / 2 / [|I_{DO} (+85\text{ }^\circ\text{C})| + |I_{DO} (-40\text{ }^\circ\text{C})|] \times 100\text{ }(\%)$  (Applied to both I<sub>DOL</sub> and I<sub>DOH</sub>)

\*8 : When Charge pump current is measured, set LDS = “L”, T1 = “L” and T2 = “H”.



# MB15F74UL

## ■ FUNCTIONAL DESCRIPTION

### 1. Pulse swallow function

$$f_{VCO} = [(P \times N) + A] \times f_{osc} \div R$$

$f_{VCO}$  : Output frequency of external voltage controlled oscillator (VCO)

$P$  : Preset divide ratio of dual modulus prescaler (32 or 64 for IF-PLL, 64 or 128 for RF-PLL)

$N$  : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)

$A$  : Preset divide ratio of binary 7-bit swallow counter ( $0 \leq A \leq 127, A < N$ )

$f_{osc}$  : Reference oscillation frequency ( $OSC_{IN}$  input frequency)

$R$  : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

### 2. Serial Data Input

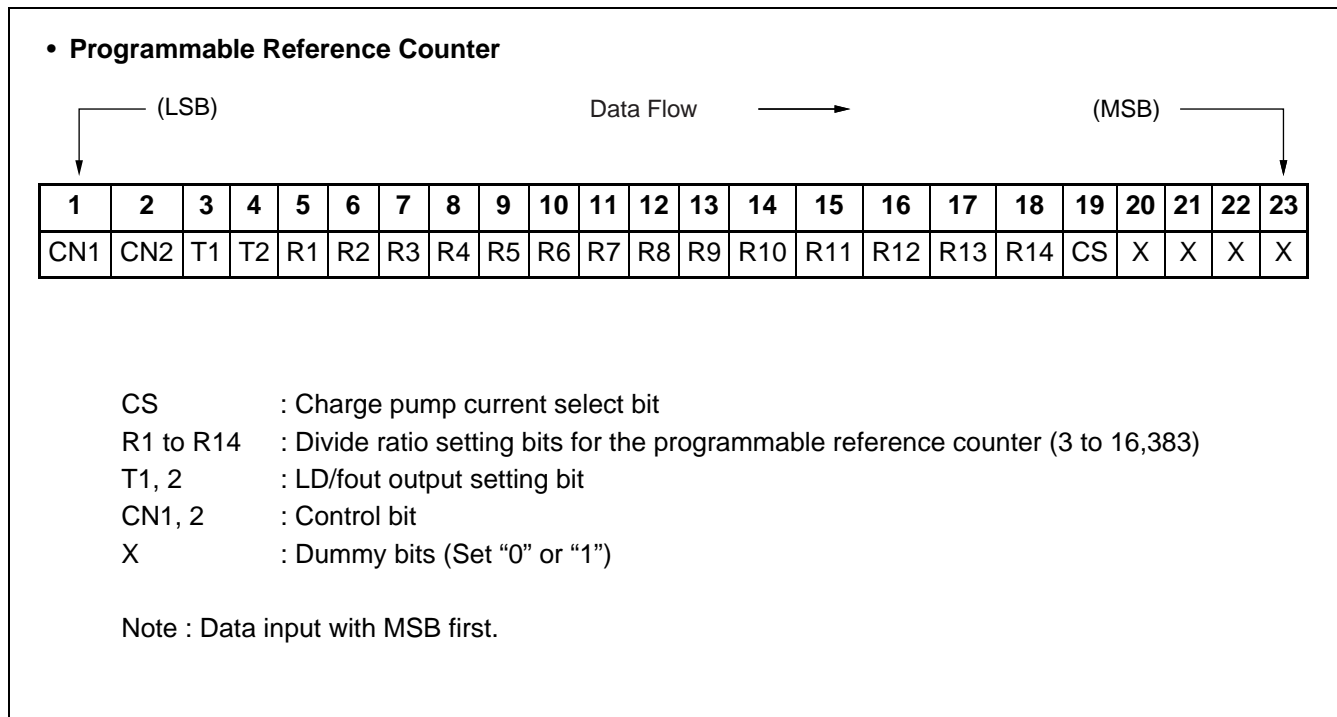
The serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.

The serial data of binary data is entered through Data pin.

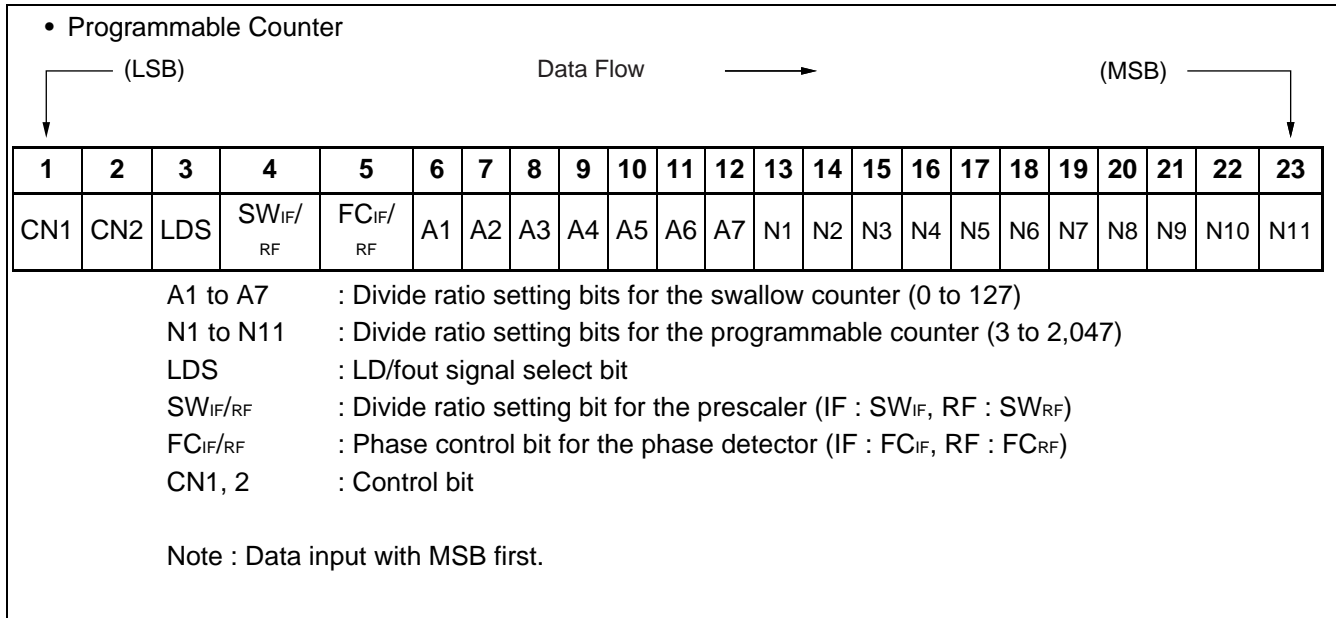
On rising edge of Clock, one bit of the serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latches depending upon the control bit data setting.

|     | The programmable reference counter for the IF-PLL | The programmable reference counter for the RF-PLL | The programmable counter and the swallow counter for the IF-PLL | The programmable counter and the swallow counter for the RF-PLL |
|-----|---|---|---|---|
| CN1 | 0   | 1   | 0   | 1   |
| CN2 | 0   | 0   | 1   | 1   |

#### (1) Shift Register Configuration







## (2) Data setting

### • Binary 14-bit Programmable Reference Counter Data Setting

| Divide ratio | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|--------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|
| 3            | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  |
| 4            | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| •            | •   | •   | •   | •   | •   | •  | •  | •  | •  | •  | •  | •  | •  | •  |
| •            | •   | •   | •   | •   | •   | •  | •  | •  | •  | •  | •  | •  | •  | •  |
| •            | •   | •   | •   | •   | •   | •  | •  | •  | •  | •  | •  | •  | •  | •  |
| 16383        | 1   | 1   | 1   | 1   | 1   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

Note : Divide ratio less than 3 is prohibited.

### • Binary 11-bit Programmable Counter Data Setting

| Divide ratio | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 |
|--------------|-----|-----|----|----|----|----|----|----|----|----|----|
| 3            | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  |
| 4            | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| •            | •   | •   | •  | •  | •  | •  | •  | •  | •  | •  | •  |
| •            | •   | •   | •  | •  | •  | •  | •  | •  | •  | •  | •  |
| •            | •   | •   | •  | •  | •  | •  | •  | •  | •  | •  | •  |
| 2047         | 1   | 1   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

Note : Divide ratio less than 3 is prohibited

### • Binary 7-bit Swallow Counter Data Setting

| Divide ratio | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|--------------|----|----|----|----|----|----|----|
| 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 1            | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| •            | •  | •  | •  | •  | •  | •  | •  |
| •            | •  | •  | •  | •  | •  | •  | •  |
| •            | •  | •  | •  | •  | •  | •  | •  |
| 127          | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

# MB15F74UL

- Prescaler Data Setting

| Divide ratio                  | SW = "H" | SW = "L" |
|-------------------------------|----------|----------|
| Prescaler divide ratio IF-PLL | 32/33    | 64/65    |
| Prescaler divide ratio RF-PLL | 64/65    | 128/129  |

- Charge Pump Current Setting

| Current value | CS |
|---------------|----|
| ±6.0 mA       | 1  |
| ±1.5 mA       | 0  |

- LD/fout output Selectable Bit Setting

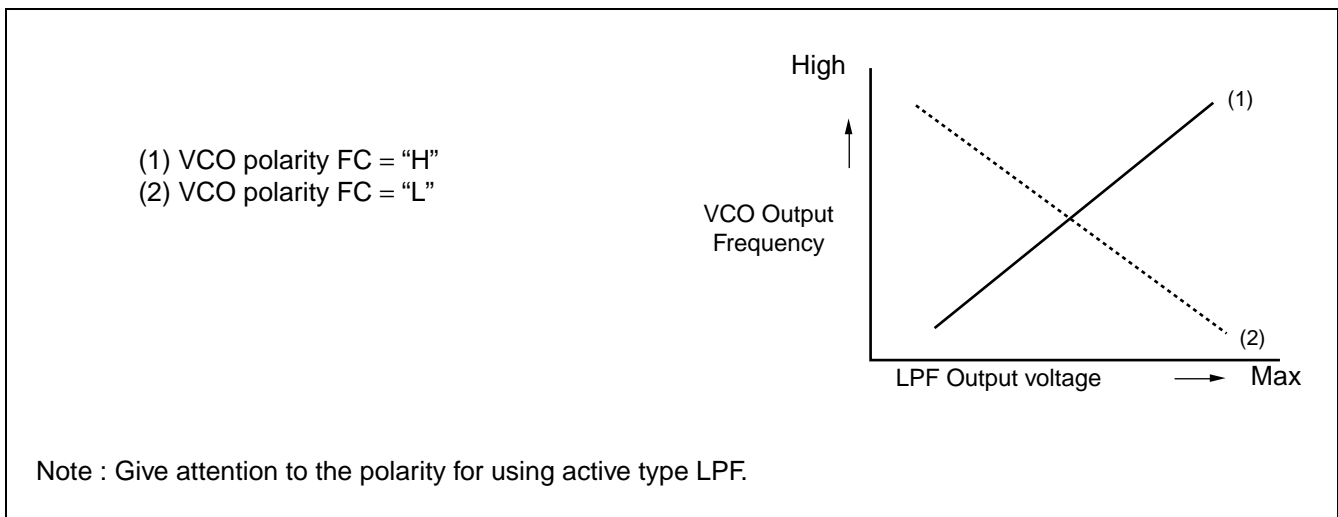
| LD/fout pin state |      | LDS | T1 | T2 |
|-------------------|------|-----|----|----|
| LD output         |      | 0   | 0  | 0  |
|                   |      | 0   | 1  | 0  |
|                   |      | 0   | 1  | 1  |
| fout output       | frIF | 1   | 0  | 0  |
|                   | frRF | 1   | 1  | 0  |
|                   | fpIF | 1   | 0  | 1  |
|                   | fpRF | 1   | 1  | 1  |

- Phase Comparator Phase Switching Data Setting

| Phase comparator input | FC <sub>IF, RF</sub> = "H" | FC <sub>IF, RF</sub> = "L" |
|------------------------|----------------------------|----------------------------|
|                        | Do <sub>IF, RF</sub>       | Do <sub>IF, RF</sub>       |
| fr > fp                | H                          | L                          |
| fr < fp                | L                          | H                          |
| fr = fp                | Z                          | Z                          |

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.



### 3. Power Saving Mode (Intermittent Mode Control Circuit)

| Status            | PS pin |
|-------------------|--------|
| Normal mode       | H      |
| Power saving mode | L      |

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

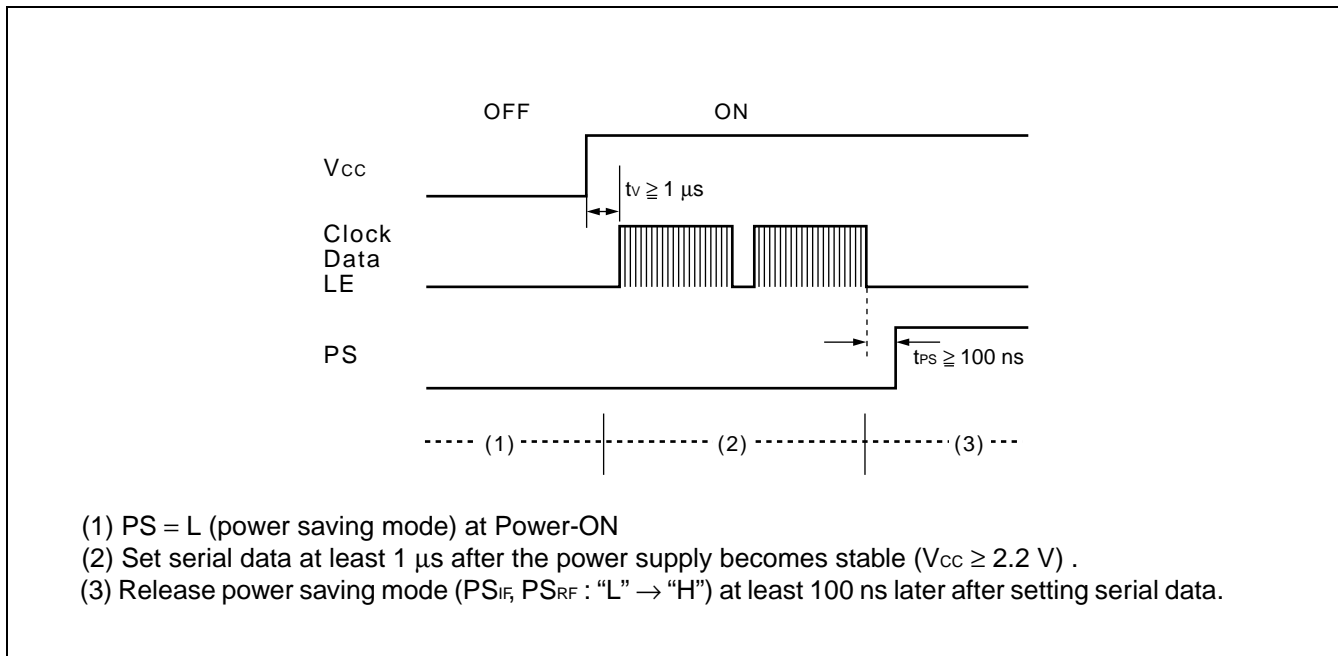
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency ( $f_p$ ) and the reference frequency ( $f_r$ ) which can cause a major change in the comparaoor output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Notes : • When power (VCC) is first applied, the device must be in standby mode.

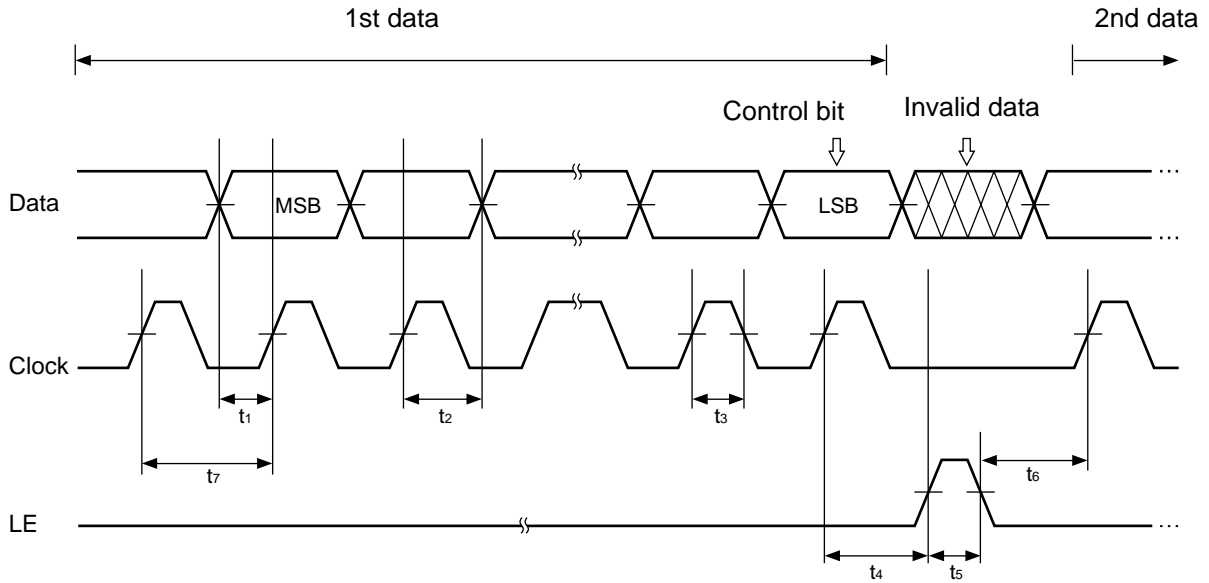
- PS pin must be set "L" at Power-ON.



# MB15F74UL

## 4. Serial Data Data Input Timing

Divide ratio is performed through a serial interface using the Data pin, Clock pin, and LE pin. Setting data is read into the shift register at the rise of the Clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

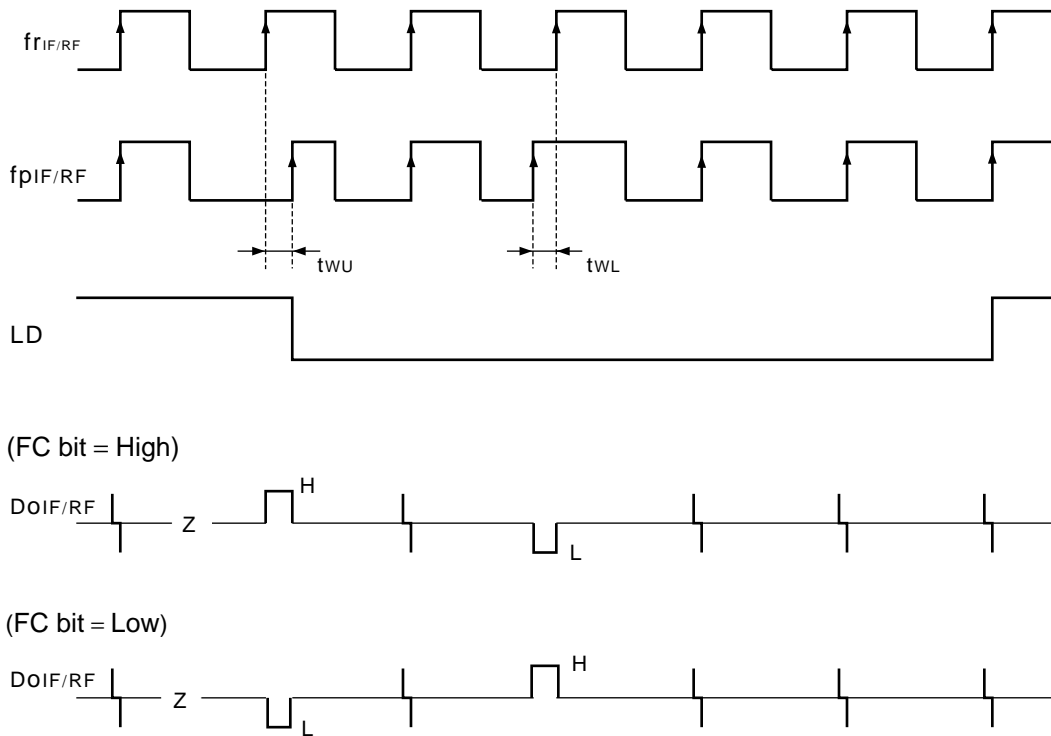


| Parameter | Min | Typ | Max | Unit |
|-----------|-----|-----|-----|------|
| $t_1$     | 20  | —   | —   | ns   |
| $t_2$     | 20  | —   | —   | ns   |
| $t_3$     | 30  | —   | —   | ns   |
| $t_4$     | 30  | —   | —   | ns   |

| Parameter | Min | Typ | Max | Unit |
|-----------|-----|-----|-----|------|
| $t_5$     | 100 | —   | —   | ns   |
| $t_6$     | 20  | —   | —   | ns   |
| $t_7$     | 100 | —   | —   | ns   |

Note : LE should be "L" when the data is transferred into the shift register.

## ■ PHASE COMPARATOR OUTPUT WAVEFORM



### • LD Output Logic

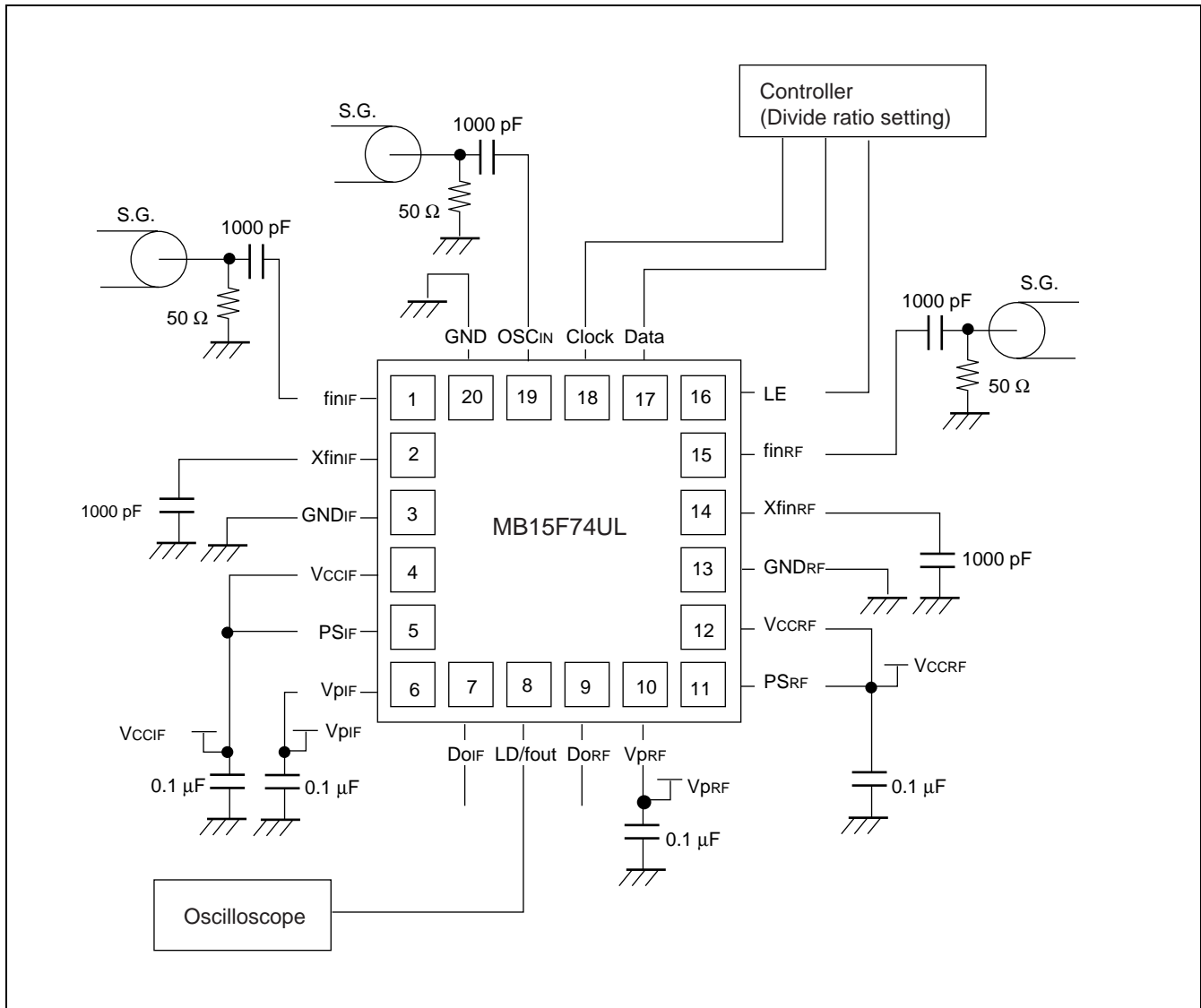
| IF-PLL section                   | RF-PLL section                   | LD output |
|----------------------------------|----------------------------------|-----------|
| Locking state/Power saving state | Locking state/Power saving state | H         |
| Locking state/Power saving state | Unlocking state                  | L         |
| Unlocking state                  | Locking state/Power saving state | L         |
| Unlocking state                  | Unlocking state                  | L         |

Notes : • Phase error detection range =  $-2\pi$  to  $+2\pi$

- Pulses on DOIF/RF signals during locking state are output to prevent dead zone.
- LD output becomes low when phase error is  $t_{WU}$  or more.
- LD output becomes high when phase error is  $t_{WL}$  or less and continues to be so for three cycles or more.
- $t_{WU}$  and  $t_{WL}$  depend on OSC<sub>IN</sub> input frequency as follows.
  - $t_{WU} \geq 2/f_{osc}$  : e.g.  $t_{WU} \geq 156.3$  ns when  $f_{osc} = 12.8$  MHz
  - $t_{WU} \leq 4/f_{osc}$  : e.g.  $t_{WU} \leq 312.5$  ns when  $f_{osc} = 12.8$  MHz

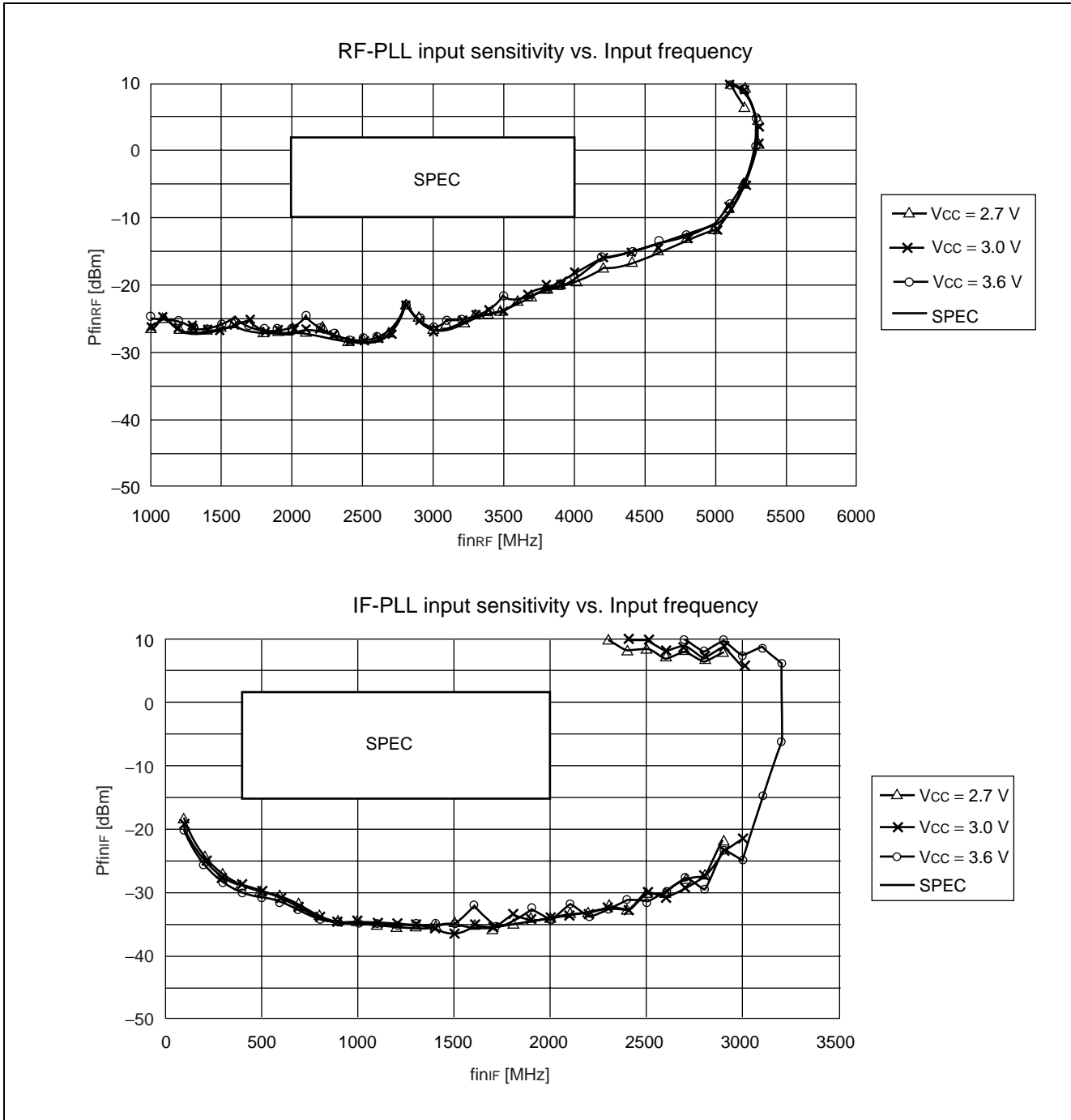
# MB15F74UL

## ■ TEST CIRCUIT (for Measuring Input Sensitivity $fin/OSC_{IN}$ )



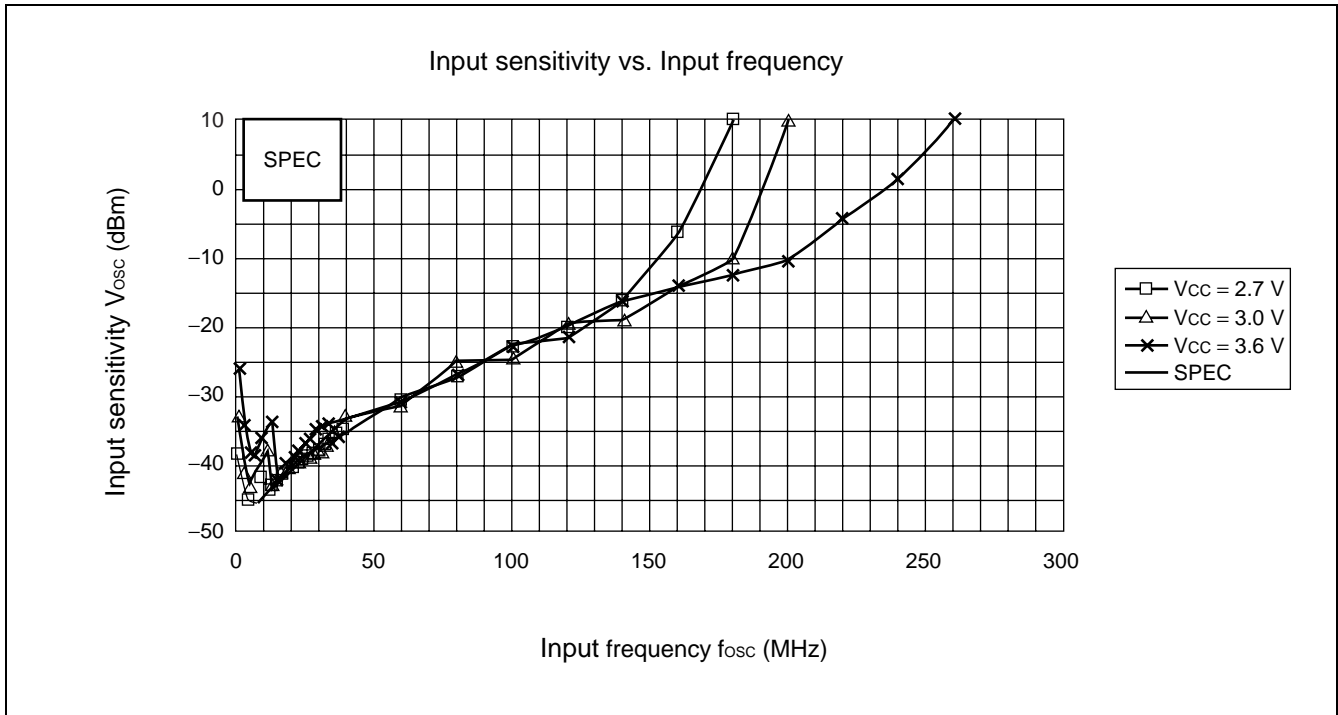
## TYPICAL CHARACTERISTICS

### 1. fin input sensitivity



# MB15F74UL

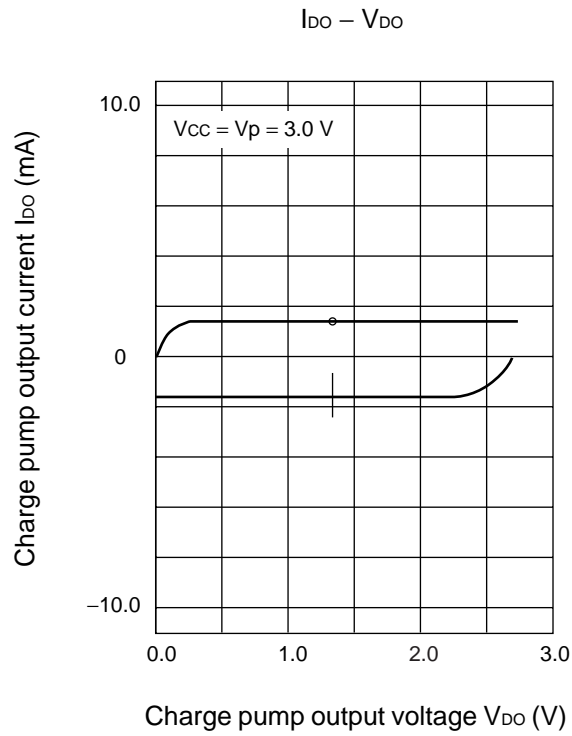
## 2. OSC<sub>IN</sub> input sensitivity



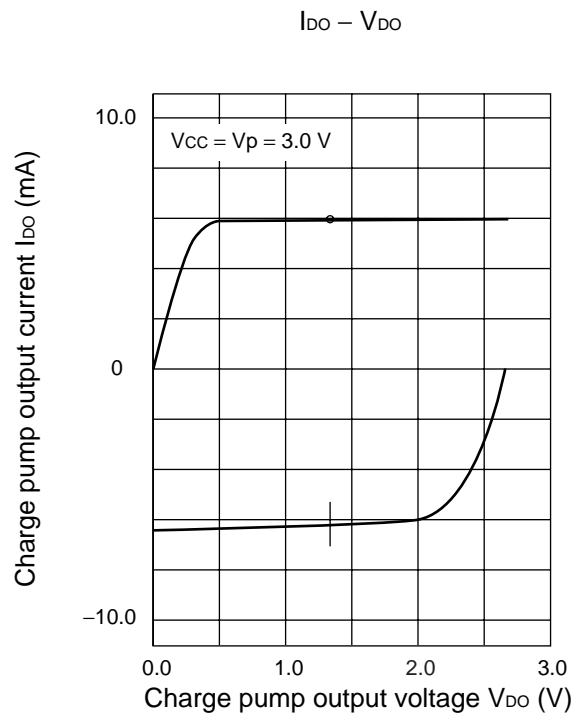


## 3. RF-PLL Do output current

- 1.5 mA mode

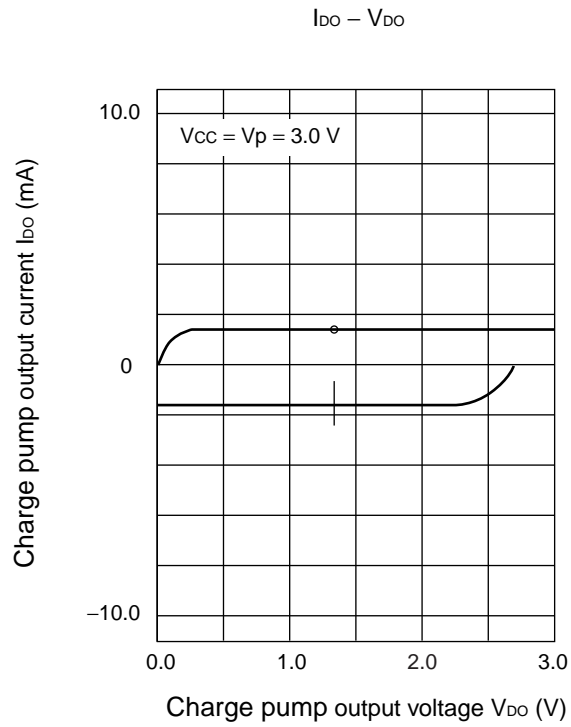


- 6.0 mA mode

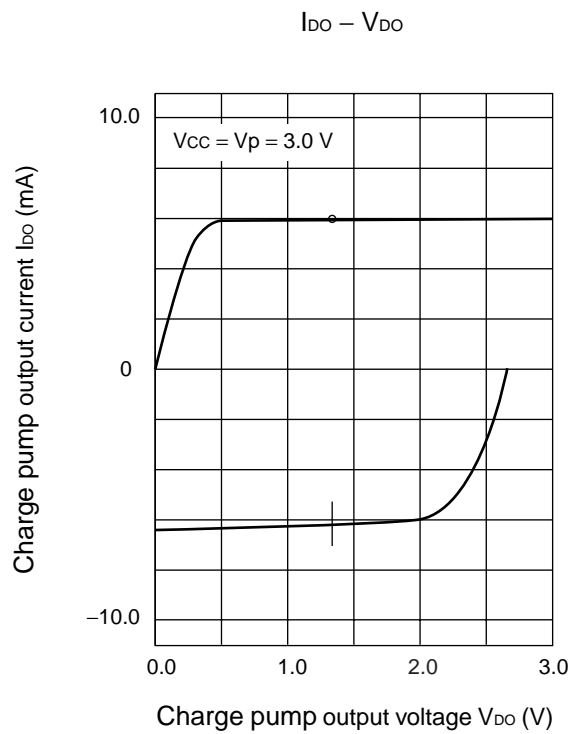


## 4. IF-PLL Do output current

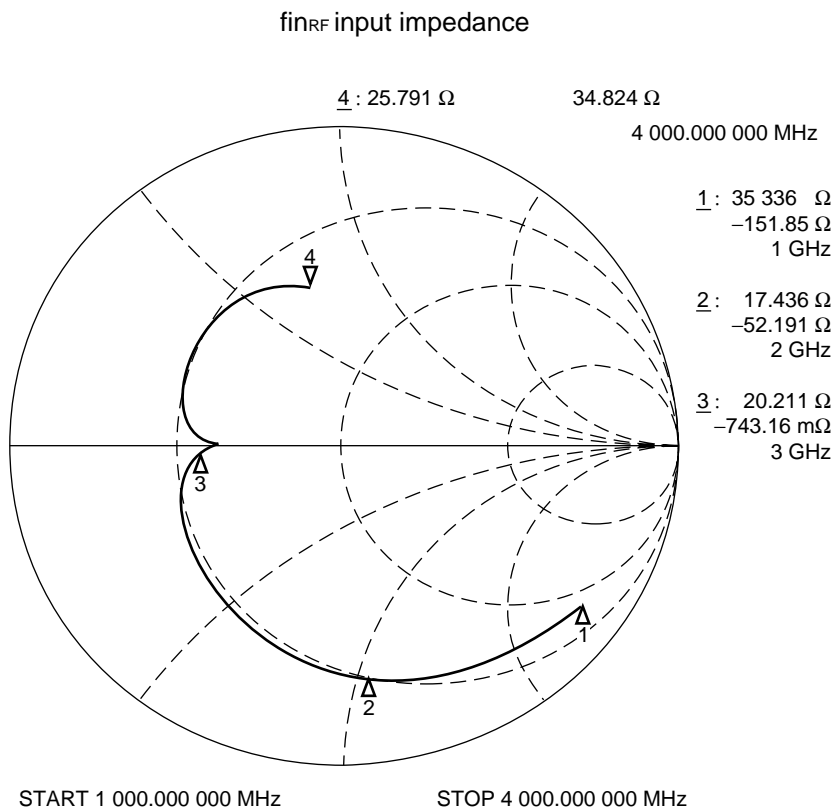
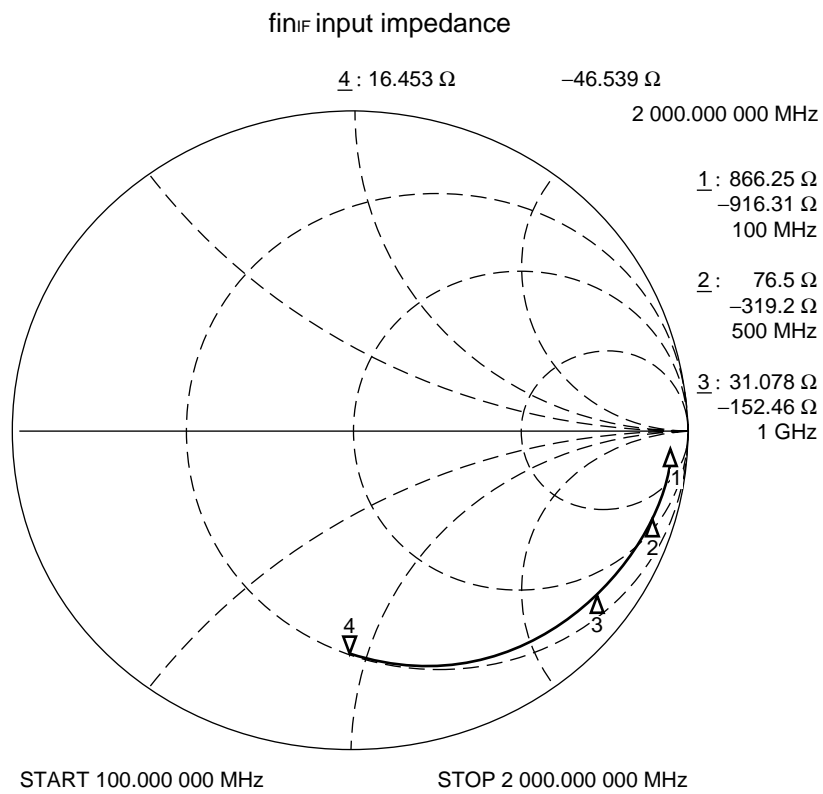
- 1.5 mA mode



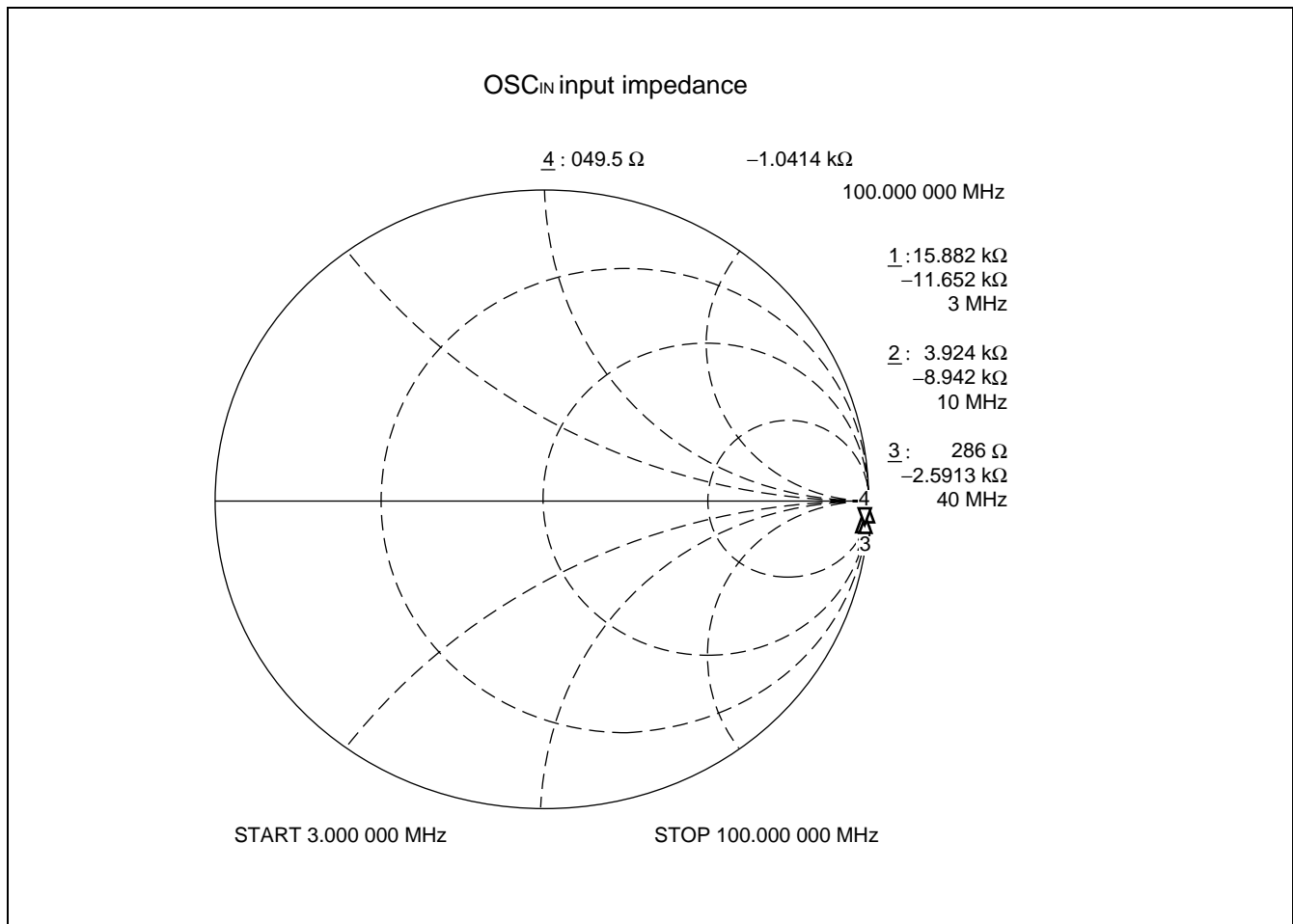
- 6.0 mA mode



## 5. fin input impedance

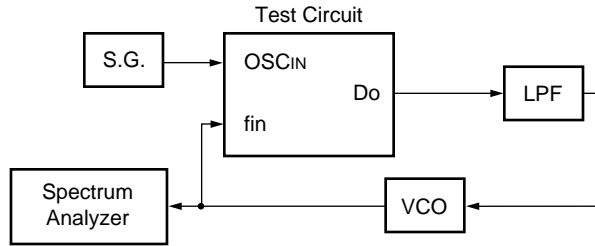


## 6. OSC<sub>IN</sub> input impedance

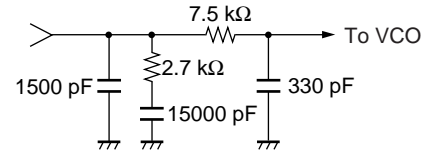


## REFERENCE INFORMATION

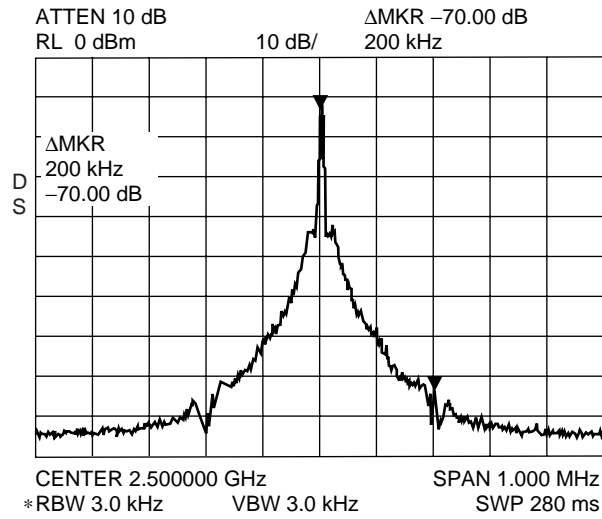
(for Lock-up Time, Phase Noise and Reference Leakage)



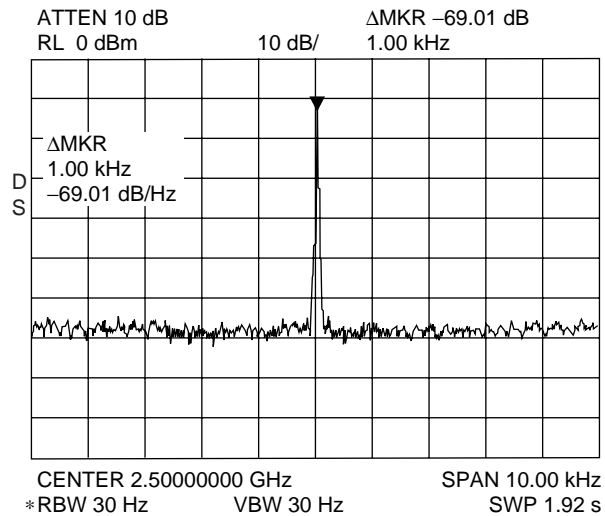
$f_{VCO} = 2500 \text{ MHz}$      $V_{CC} = 3.0 \text{ V}$   
 $K_v = 50 \text{ MHz/V}$      $T_a = +25 \text{ }^\circ\text{C}$   
 $f_r = 200 \text{ kHz}$      $CP : 6 \text{ mA mode}$   
 $f_{osc} = 13 \text{ MHz}$   
 LPF



### • PLL Reference Leakage



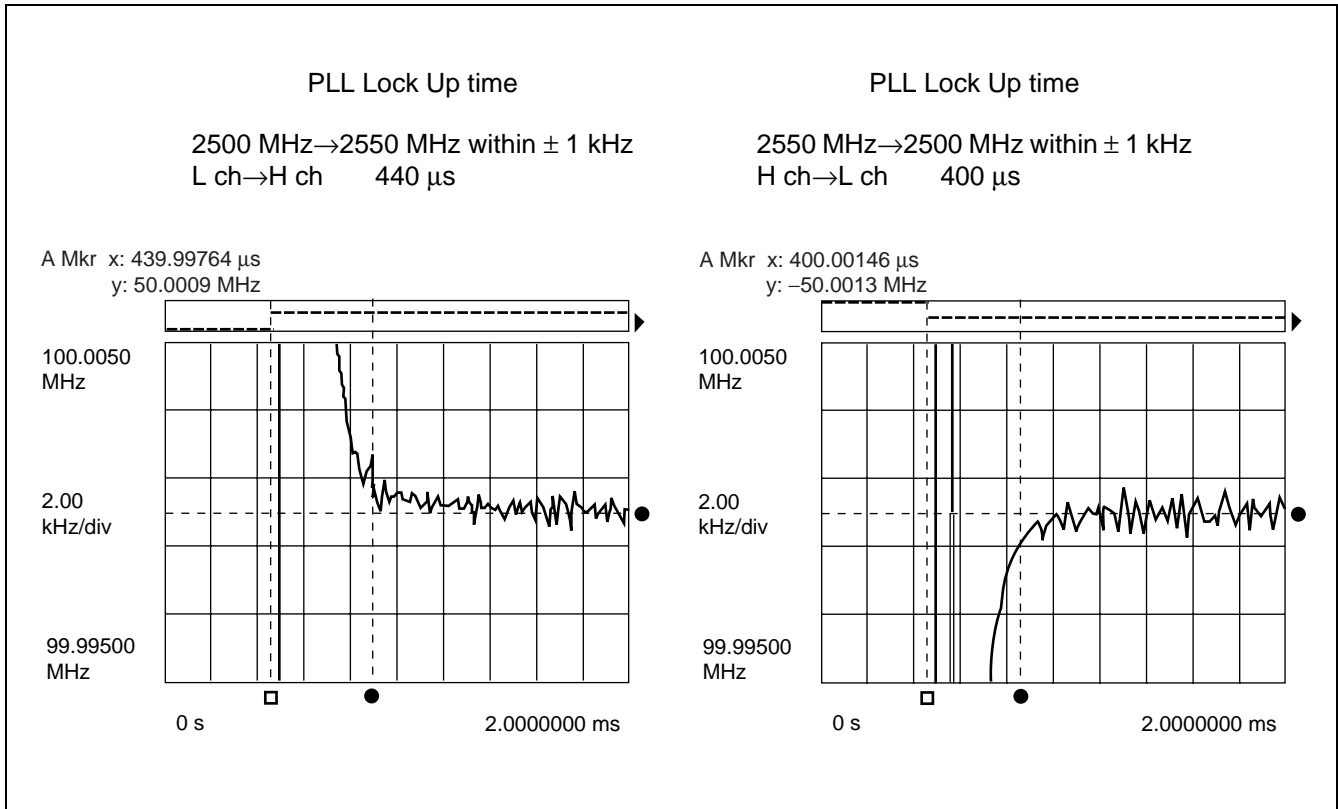
### • PLL Phase Noise



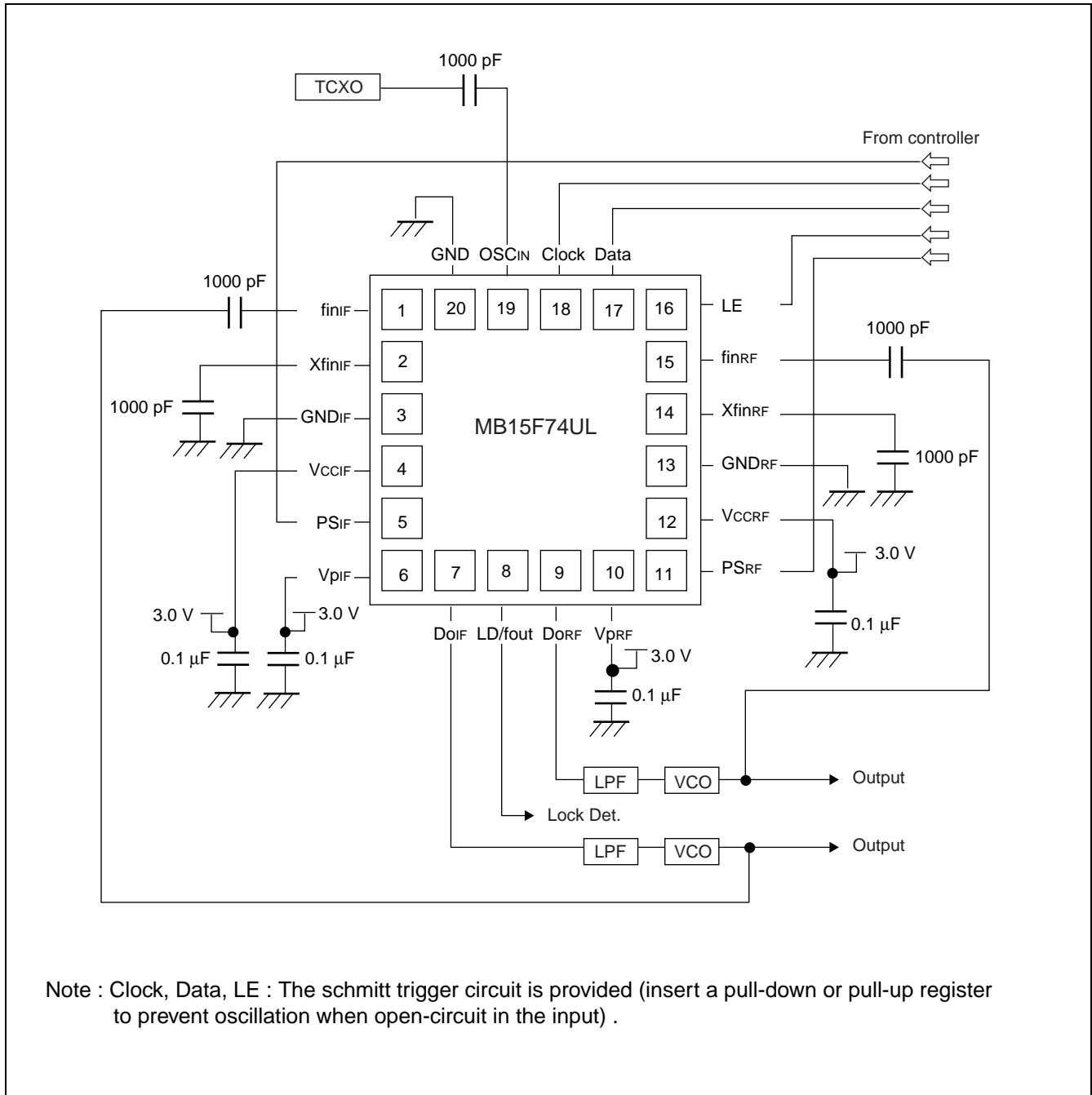
(Continued)

# MB15F74UL

(Continued)



## APPLICATION EXAMPLE



Note : Clock, Data, LE : The schmitt trigger circuit is provided (insert a pull-down or pull-up register to prevent oscillation when open-circuit in the input) .

# MB15F74UL

## ■ USAGE PRECAUTIONS

(1)  $V_{CCRF}$ ,  $V_{PRF}$ ,  $V_{CCIF}$  and  $V_{PIF}$  must be equal voltage.

Even if either RF-PLL or IF-PLL is not used, power must be supplied to  $V_{CCRF}$ ,  $V_{PRF}$ ,  $V_{CCIF}$  and  $V_{PIF}$  to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions :

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device

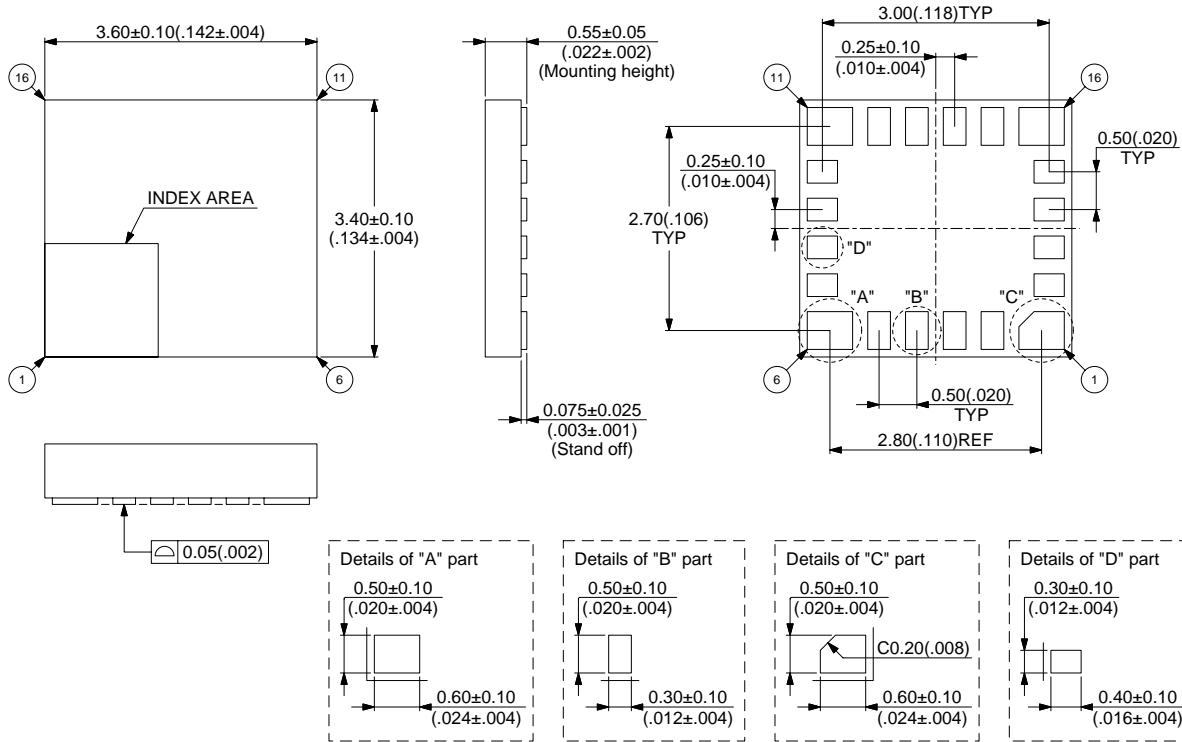
## ■ ORDERING INFORMATION

| Part number  | Package                             | Remarks |
|--------------|-------------------------------------|---------|
| MB15F74ULPVA | 20-pad plastic BCC<br>(LCC-20P-M05) |         |



## ■ PACKAGE DIMENSION

20-pad plastic BCC  
(LCC-20P-M05)



© 2001 FUJITSU LIMITED C20056S-c-2-1

Dimensions in mm (inches)

## FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.