REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, t_S19, correct footnote. Editorial changes throughout.	1990 AUG 22	Weckman

REV																								
SHEET																								
REV	A	A	A																					
SHEET	22	23	24																					
REV STATUS OF SHEETS	REV	A		A					A				A							A				
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 8 APRIL 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, BIPOLAR CLOCK GENERATOR/MICROCYCLE LENGTH CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88598

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1744

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88598	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Maximum operating frequency
01	2925	Clock generator	31 MHz
02	2925A	Clock generator	50 MHz

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	660 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases L and 3	(See MIL-M-38510, appendix C)
Junction temperature (T_J)	+175°C
DC voltage applied to outputs for high output state	-0.5 V dc to +V_{CC} maximum
DC output current into outputs	30 mA
DC input current	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V dc
Maximum low level input voltage (V_{IL})	+0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardization Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Function tables. The function tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified			Group A subgroups	Device type	Limits		Unit
							Min	Max	
Output high voltage	V_{OH}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -1.0 mA		1,2,3	All	2.5		V
Input low voltage	V_{OL}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}		I_{OL} = 4.0 mA				0.4	V
			$\overline{WAITACK}$ C_1, C_2 C_3, C_4	I_{OL} = 8.0 mA				0.45	
				I_{OL} = 12 mA				0.5	
			F_O	I_{OL} = 16 mA				0.5	
Input high level 1/	V_{IH}	Guaranteed input logical HIGH voltage for all inputs					2.0		V
Input low level 1/	V_{IL}	Guaranteed input logical LOW voltage for all inputs						0.7	V
Input clamp voltage 1/	V_{IC}	V_{CC} = Min., I_{IN} = -18 mA						-1.5	V
Input low current	I_{IL}	V_{CC} = Max V_{IN} = 0.4 V	READY, $\overline{INIT}$, L_1, L_2, L_3					-0.4	mA
			$\overline{WAITREQ}$, X_1					-0.8	
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$					-1.0	
			C_X					-1.2	
			First/$\overline{LAST}$					-1.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +125^{\circ}C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input high current	I_{IH}	V_{CC} = Max, V_{IN} = 2.7	READY, INIT, L_1, L_2, L_3	1,2,3	All		20	µA
			WAITREQ				50	
			SSNO, SSNC, RUN, HALT				-500	
			C_X				70	
			First/LAST				-750	
			X_1				500	
Input high current	I_I	V_{CC} = Max, V_{IN} = 5.5 V	READY, INIT, L_1, L_2, L_3				100	µA
			WAITREQ, C_X				1.0	mA
			SSNO, SSNC, RUN, HALT				100	µA
			First/LAST				1.0	mA
		V_{CC} = Max, V_{IN} = 4.0 V	X_1				1.0	mA
Output short circuit current 2/	I_{OS}	V_{CC} = Max		1,2,3	All	-30	-85	mA
Power supply current 3/	I_{CC}	V_{CC} = Max					120	mA
Functional test		See 4.3.1c		7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
F_O frequency (TTL input) 4/ 5/	f_{MAX1}	C_L = 15 pF R_L = 280Ω See figure 4	9,10,11	01	31		MHz
				02	55		MHz
F_O frequency (crystal input) 4/ 5/	f_{MAX2}			01	31		MHz
				02	45		MHz
F_O (↑) to C_1, C_2, C_3, C_4, or $\overline{WAITACK}$ (↑)	t_{OFFSET} 3	C_L = 50 pF R_L = 2.0 kΩ See figure 4	9,10,11	All		8.5	ns
F_O (↑) to C_1, C_2, C_3, C_4, or $\overline{WAITACK}$ (↓)	t_{OFFSET} 4			01		18	ns
				02		8.5	ns
C_1 (↑) to C_2 (↑)	t_{SKEW} 5			01	-2	2	ns
				02	-5	5	ns
C_1 (↑) to C_3 (↑)	t_{SKEW} 6			01	-2	2	ns
				02	-5	5	ns
C_1 (↑) to C_4 (↓) opposite transition	t_{SKEW} 7			All	-11	11	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
L_1, L_2, L_3 to C_1 (↑) 6/	t_S 8	C_L = 50 pF R_L = 2.0 kΩ See figure 4	9,10,11	01	7		ns
				02	15		ns
L_1, L_2, L_3 to C_1 (↑) 6/	t_H 9			01	11		ns
				02	0		ns
C_X to F_0 (↑) 6/ 7/	t_S 10			01	25		ns
				02	15		ns
C_X to F_0 (↑) 6/ 7/	t_H 11			All	0		ns
$\overline{WAITREQ}$ to F_0 (↑) 6/ 8/	t_S 12			01	25		ns
				02	15		ns
$\overline{WAITREQ}$ to F_0 (↑) 6/ 8/	t_H 13			All	0		ns
$\overline{READY}$ to F_0 (↑) 6/ 8/	t_S 14			01	25		ns
				02	15		ns
$\overline{READY}$ to F_0 (↑) 6/ 8/	t_H 15			All	0		ns
$\overline{RUN}$, $\overline{HALT}$ (↓) to F_0 (↑) 6/ 8/ 9/	t_S 16			01	25		ns
				02	15		ns
SSNC, SSNO to F_0 (↑) 6/ 8/ 9/	t_H 17			01	25		ns
				02	15		ns

See footnotes at end of table.

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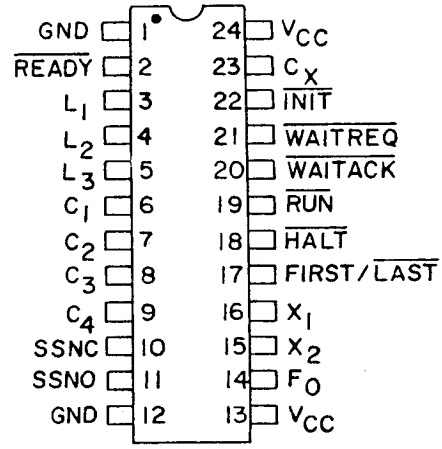
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
FIRST/$\overline{\text{LAST}}$ to F_0 (↑) 6/ 10/	t_S 18	C_L = 50 pF, R_L = 2.0 kΩ, See figure 4	9,10,11	01	35		ns
				02	20		ns
$\overline{\text{INIT}}$ (↑) to F_0 (↑) 6/ 8/	t_S 19			01	35		ns
				02	20		ns
$\overline{\text{INIT}}$ low pulse width	t_{PWL} 20		9,10,11	01	25		ns
				02	12		ns
$\overline{\text{INIT}}$ to WAITACK	t_{PLH}			01		27	ns
				02		17	ns
Propagation delay X_1 to F_0 11/ 12/	t_{PLH}	C_L = 15 pF, R_L = 280 kΩ, See figure 4	9,10,11	01		26	ns
				02		16	ns
Propagation delay X_1 to F_0 11/ 12/	t_{PHL}			01		23	ns
				02		13	ns

1/ Does not apply to X_1 and X_2.
2/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed 1 second.
3/ I_{CC} varies with temperature and oscillation frequency. This test is measured over full temperature range with F_0 = 0.
4/ The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or high. The C_X input load must be considered part of the 50 pF/2.0 kΩ clock output loading.
5/ f_{MAX} not tested. Guaranteed by characterization.
6/ Setup and hold not tested. Guaranteed by characterization.
7/ These setup and hold times apply to the F_0 low-to-high transition of the period in which C_X goes low.
8/ These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
9/ These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10/ FIRST/$\overline{\text{LAST}}$ normally wired high or low.
11/ Reference point of T offset has been moved forward which has increased T offsets.
12/ Test at 50 pF system load correlated to 15 pF.

Case L



Case 3

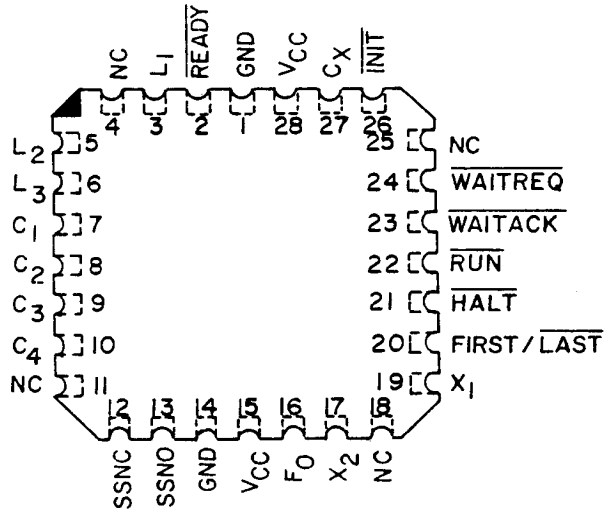
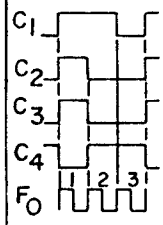
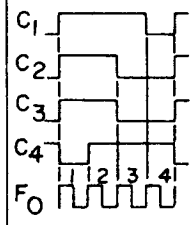
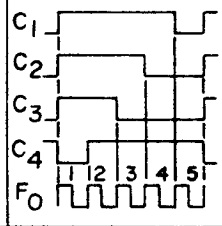
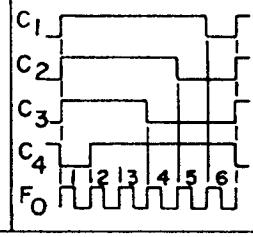


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
		REVISION LEVEL	SHEET 9

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—749-033

PATTERN INPUT CODE $L_3L_2L_1$	WAVEFORMS AND TIMING
F_3 LLL	
F_4 LLH	
F_5 HLH	
F_6 HHH	

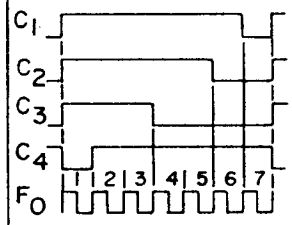
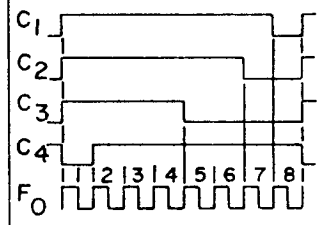
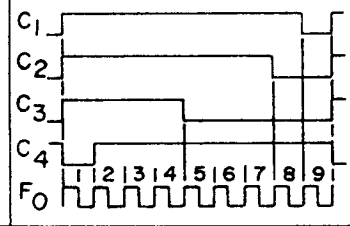
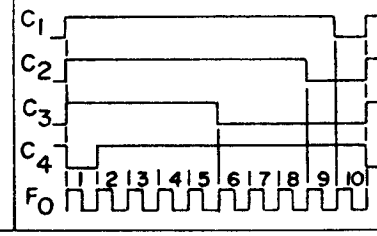
PATTERN INPUT CODE $L_3L_2L_1$	WAVEFORMS AND TIMING
F_7 LHH	
F_8 LHL	
F_9 HHL	
F_{10} HLL	

FIGURE 2. Function tables.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
		REVISION LEVEL	SHEET 10

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Functional descriptions

Pin number (see note)	Name	I/O	Description
6, 7, 8, 9	C_1-C_4	O	System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2, and L_3.
3, 4, 5	L_1-L_3	I	Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.
14	F_0	O	Buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{\text{WAITACK}}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.
18,19	$\overline{\text{HALT}}$, $\overline{\text{RUN}}$	I	Debounce inputs. These inouts determine whether the output clocks run or not. A LOW input on $\overline{\text{HALT}}$ ($\overline{\text{RUN}}$ = HIGH) will stop all clock outputs.
17	FIRST/$\overline{\text{LAST}}$	I	$\overline{\text{HALT}}$ time control input. A HIGH input in conjunction with a $\overline{\text{HALT}}$ command will cause a halt to occur when C_4 = LOW and C_1 = C_2 = C_3 = HIGH (see clock waveforms). A LOW input causes a $\overline{\text{HALT}}$ to occur when C_1 = C_2 = C_3 = LOW and C_4 = HIGH.
10,11	SSNO,SSNC	I	Single-step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{\text{HALT}}$ is activated LOW.
21	$\overline{\text{WAITREQ}}$	I	$\overline{\text{WAIT REQUEST}}$. When LOW this input will cause the outputs to halt during the next oscillator cycle after the C_X input goes LOW.
23	C_X	I	Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.

FIGURE 2. Function tables - Continued.

Functional descriptions

Pin number (see note)	Name	I/O	Description
20	WAITACK	O	WAIT ACKNOWLEDGE. When LOW, this output indicates that all clock outputs are in the "WAIT" state.
2	READY	I	READY. The READY active LOW input is used to continue normal clock output patterns after a wait stage.
22	INIT	I	INITIALIZE. This input is intended for use during power-up initialization of the system. When LOW all clock outputs free run regardless of the state of the Halt, Single Step, Wait, Request, and Ready inputs.
15,16	X_1, X_2	I/O	External crystal connections. X_1 can also be driven by a TTL frequency source. X_2 is a output for the crystal oscillator. It should be left floating if X_1 is driven directly.

NOTE: Pin numbers apply to case outline L only.

FIGURE 2. Function tables - Continued.

Device type 01

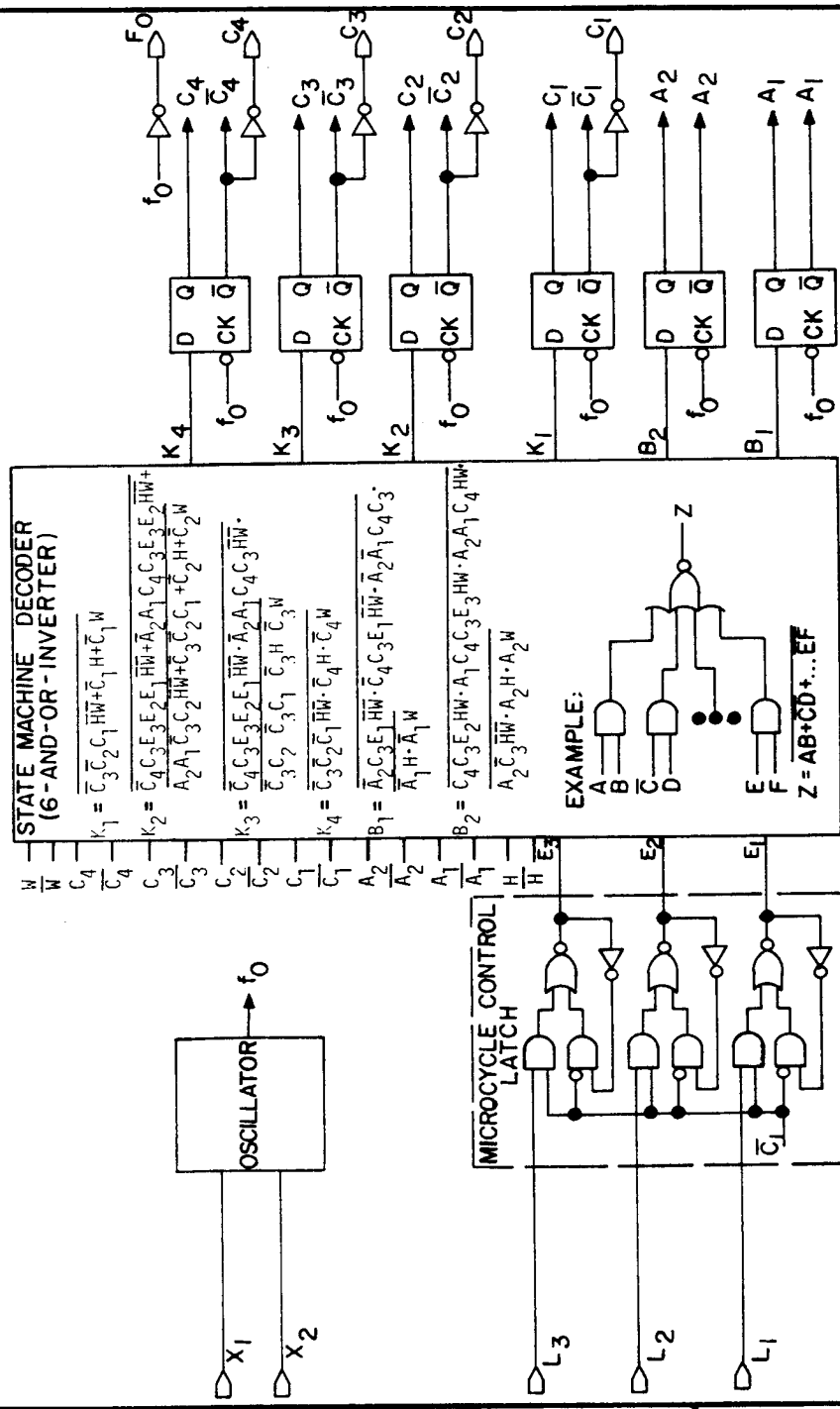

FIGURE 3. Logic diagrams.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
		REVISION LEVEL	SHEET 13

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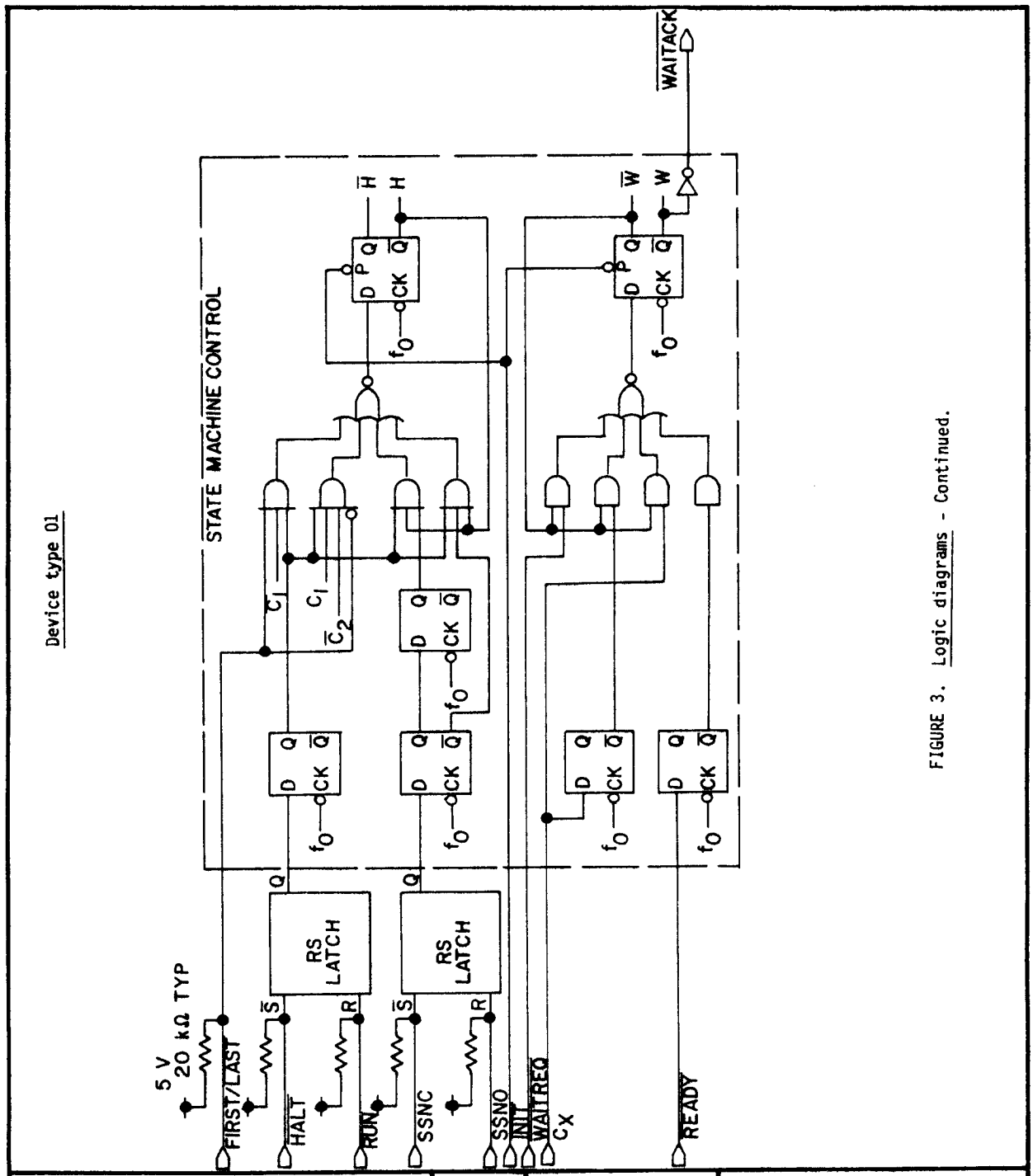

FIGURE 3. Logic diagrams - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
		REVISION LEVEL	SHEET 14

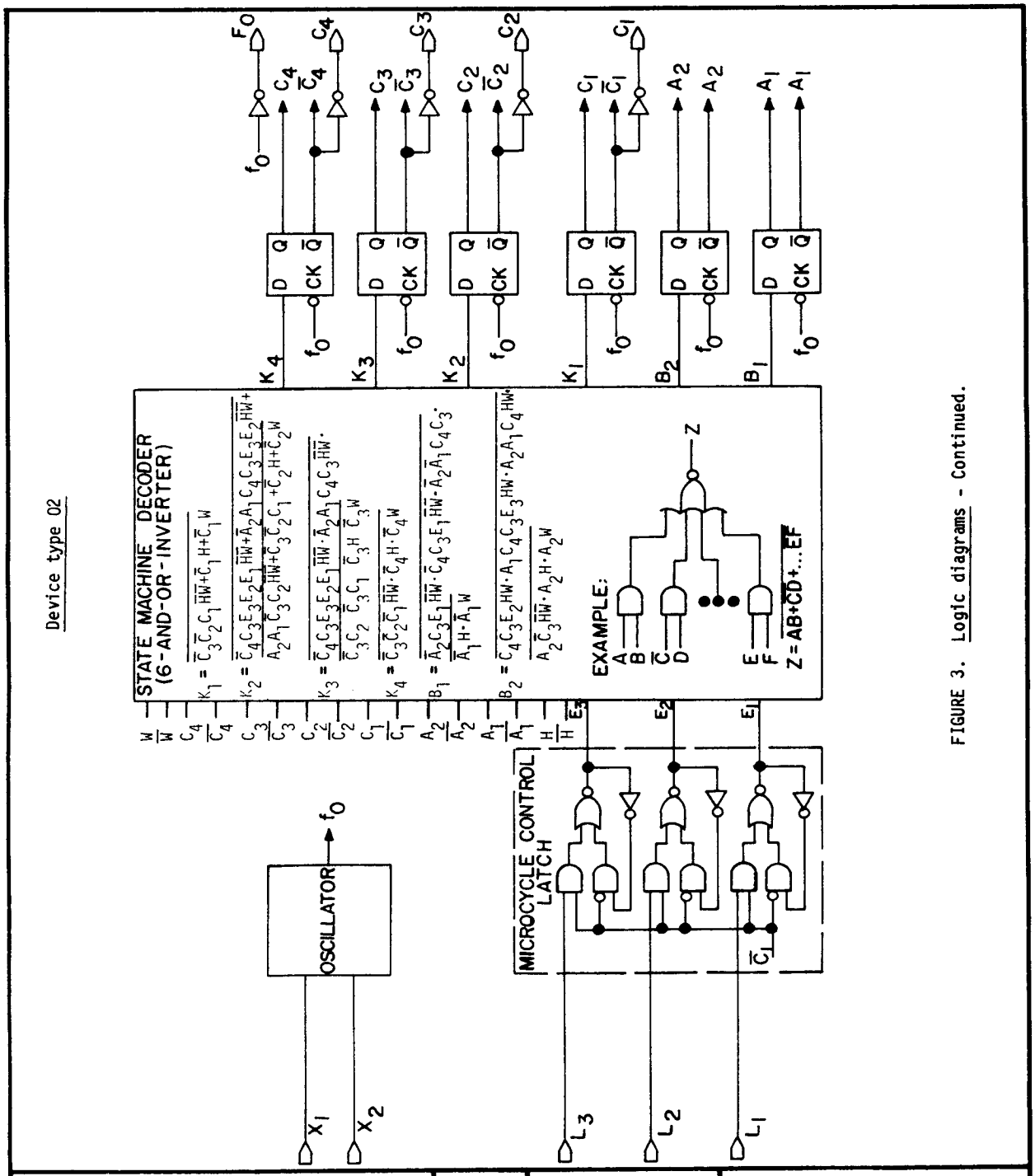

FIGURE 3. Logic diagrams - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
		REVISION LEVEL	SHEET 15

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SEP 87

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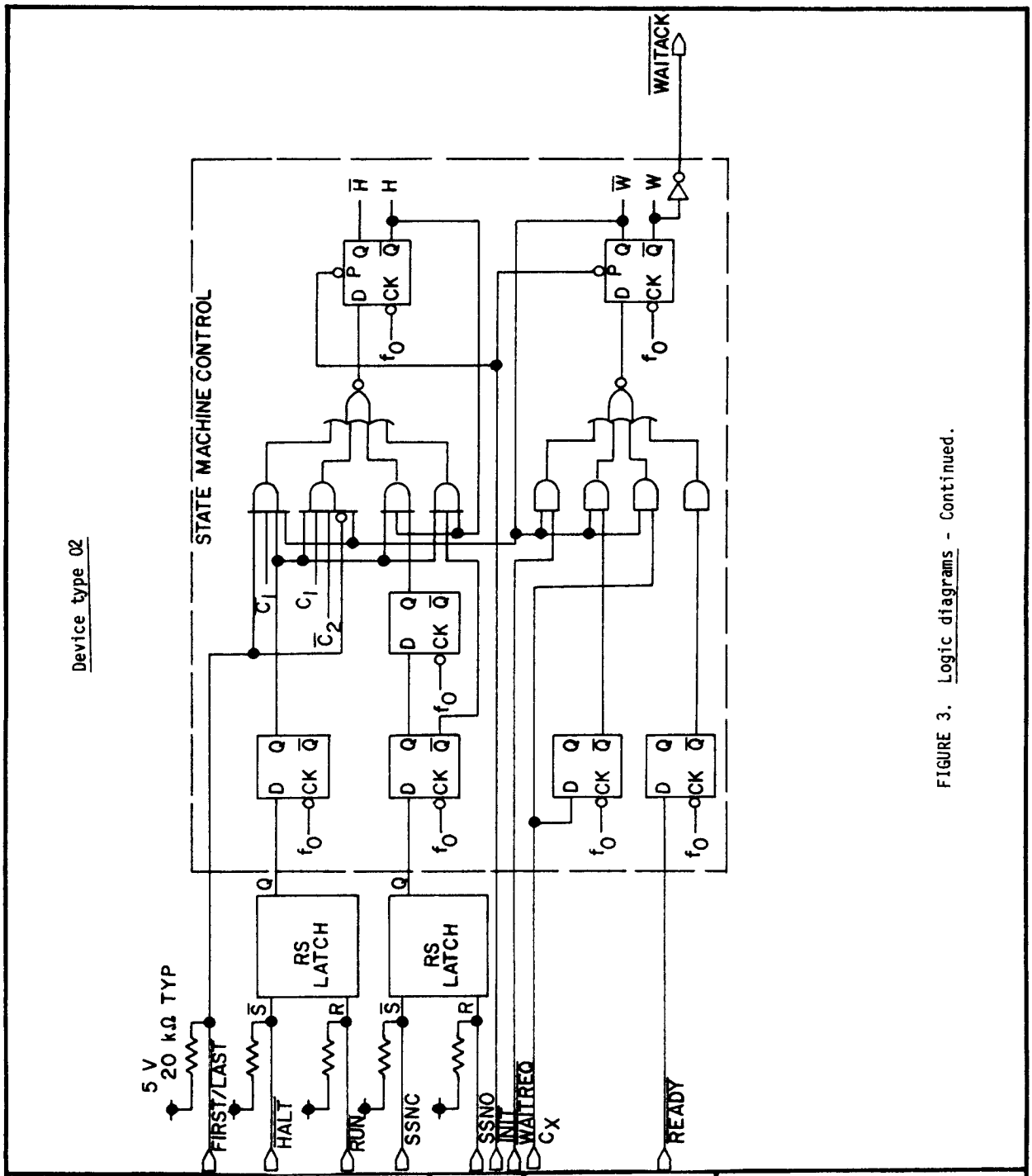

FIGURE 3. Logic diagrams - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
		REVISION LEVEL	SHEET 16

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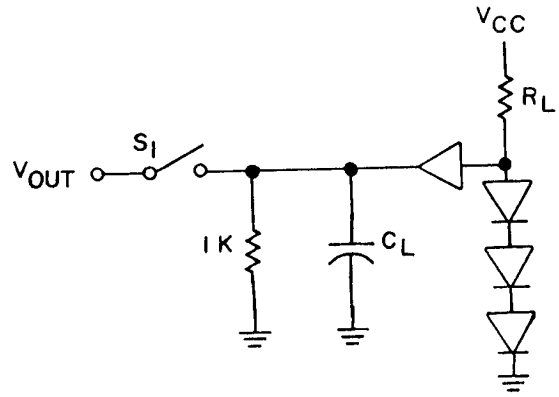
Switching test circuits



NOTES:
1. C_L and R_L values for various outputs indicated on the electrical performance tables.
2. C_L includes scope probe, wiring, and stray capacitances without a device in the test fixture.
3. Programmable loads are used for automatic testing.

Setup and hold times

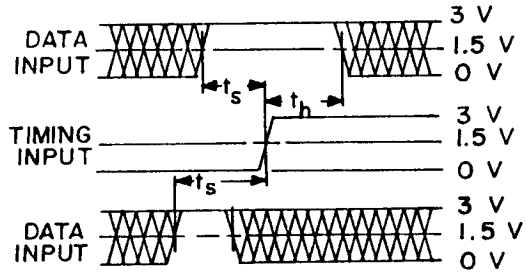
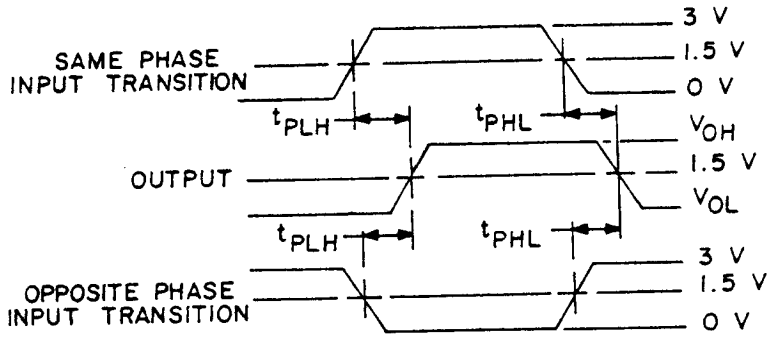


FIGURE 4. Switching waveforms and test circuit.

Propagation delay



Pusle width

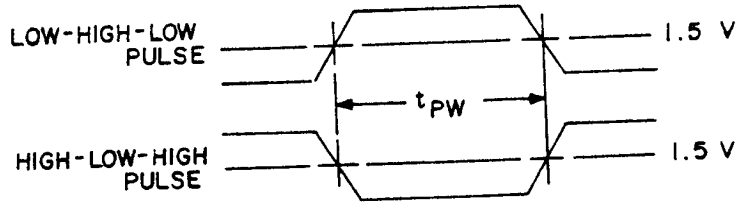


FIGURE 4. Switching waveforms and test circuit - Continued.

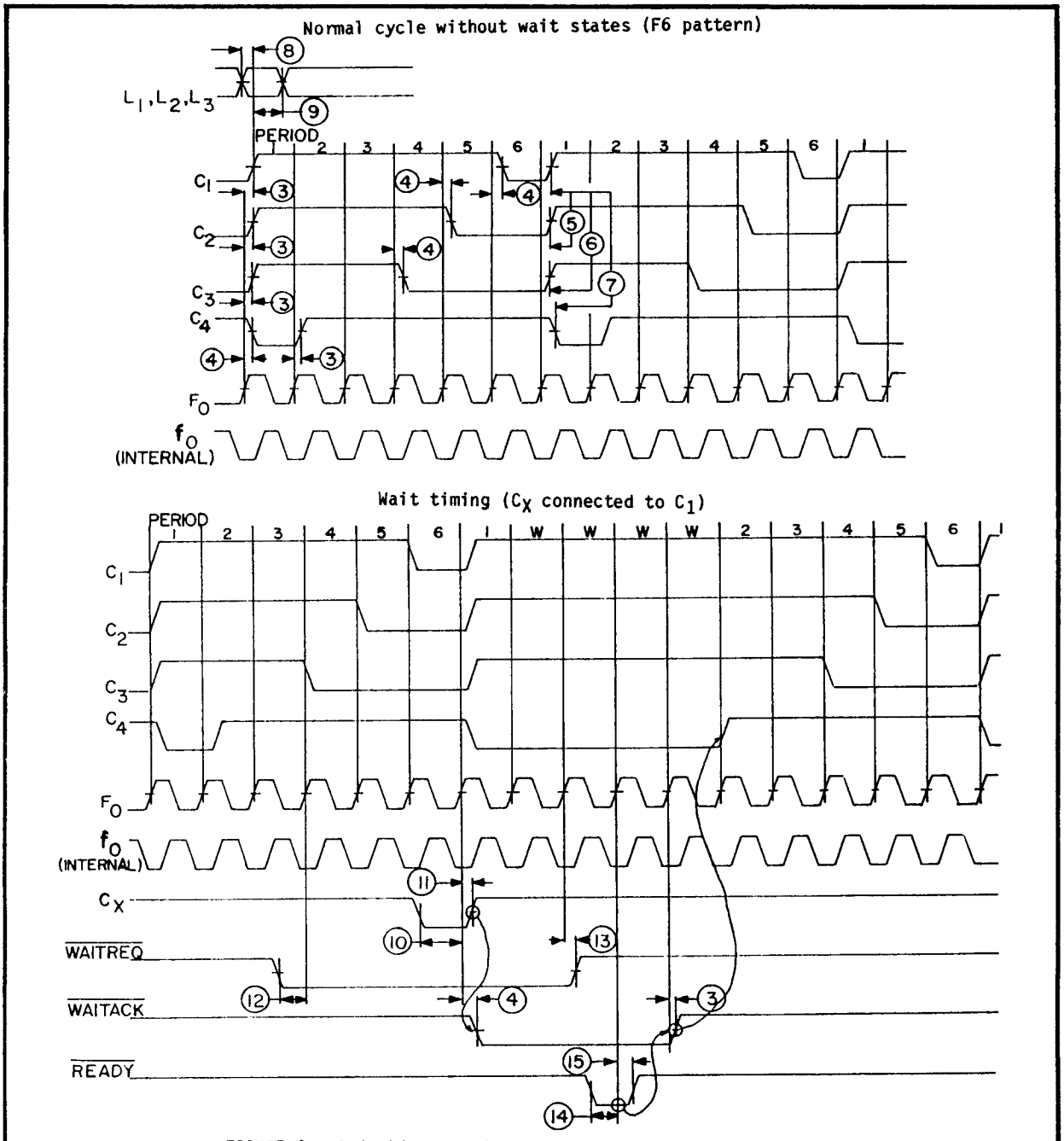


FIGURE 4. Switching waveforms and test circuit - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88598
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Normal cycle without wait states (F3 pattern)

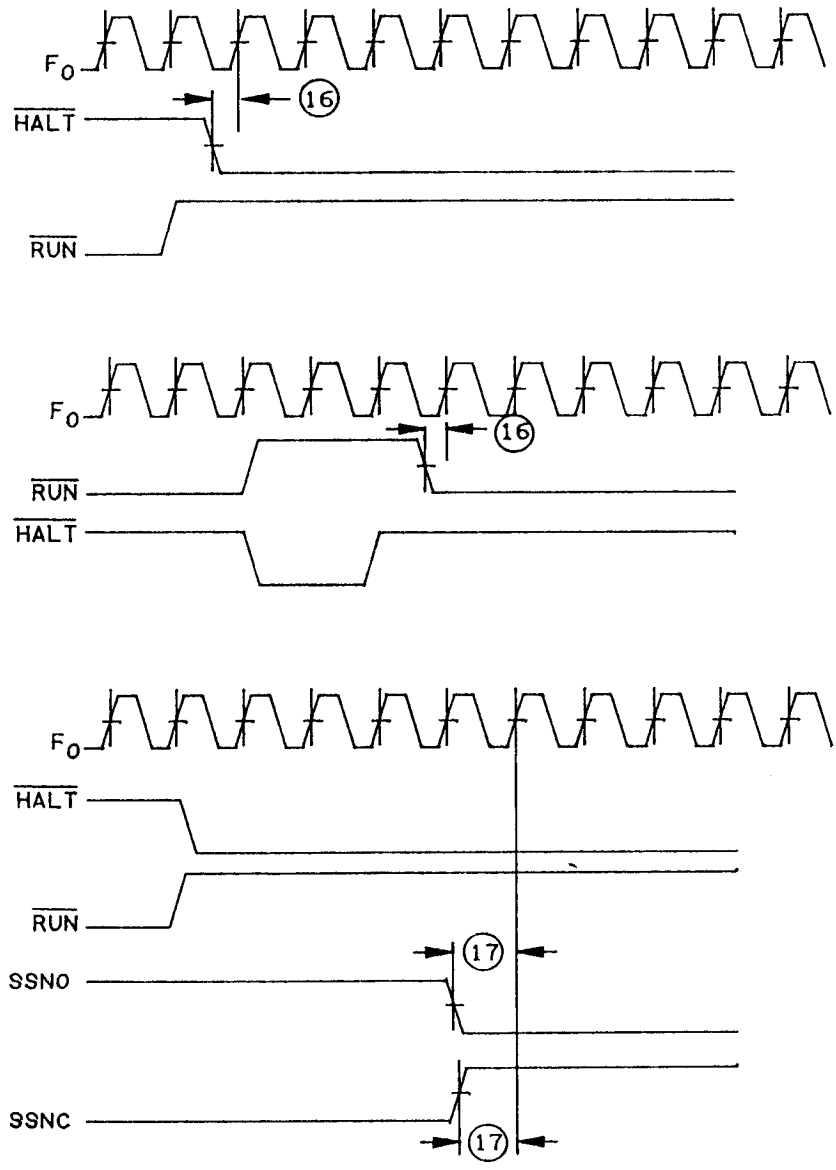
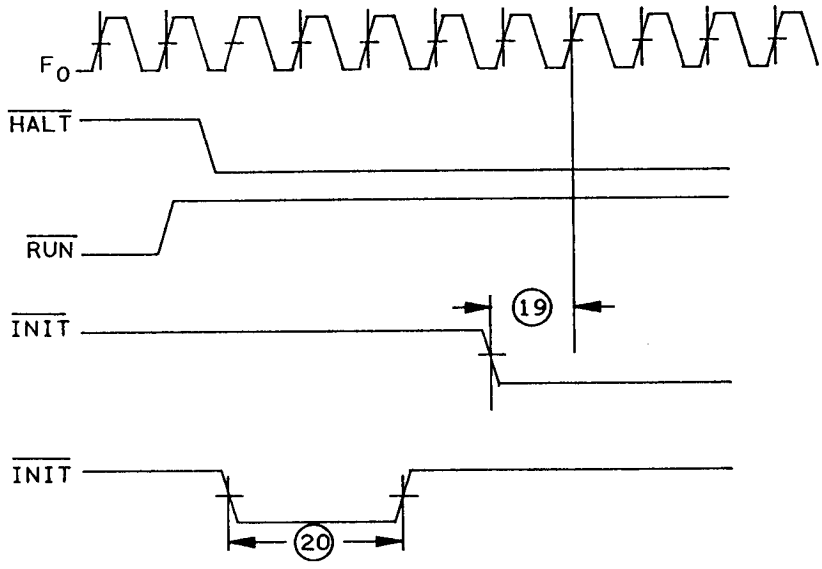


FIGURE 4. Switching waveforms and test circuits - Continued.

Normal cycle without wait states (F3 pattern)



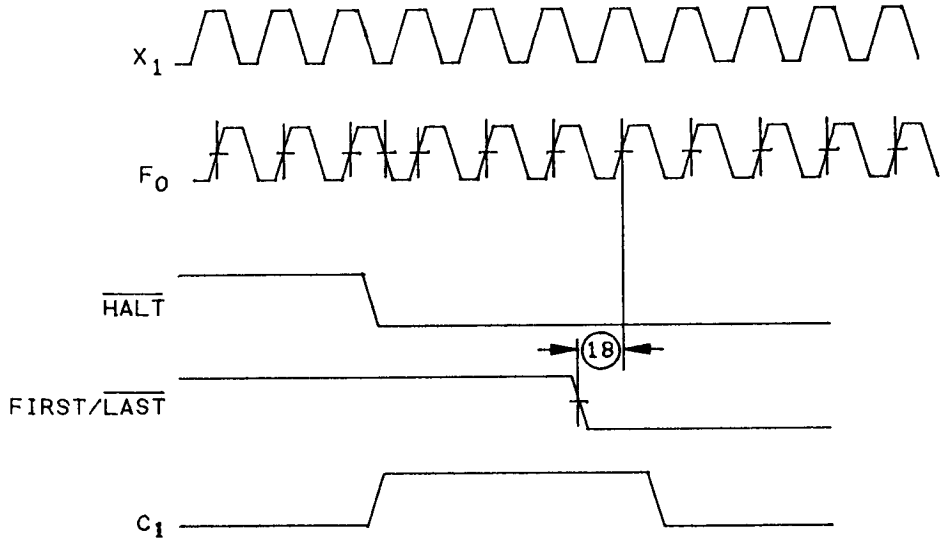


FIGURE 4. Switching waveforms and test circuits - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.6. The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests sufficient to verify the function table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method) 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8, 9,10,11

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8859801LX	34335	AM2925/BLA
5962-88598013X	34335	AM2925/B3A
5962-8859802LX	34335	AM2925A/BLA
5962-88598023X	34335	AM2925A/B3A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088