

REVISIONS																			
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED			
A	Add device type 02. Add package Y. Correct table I, I _{CC} . Editorial changes throughout.										92-01-16					Monica Poelking			
B	Changes in accordance with NOR 5962-R058-94										93-12-02					Tim Noh			
C	Changes in accordance with NOR 5962-R025-95										94-11-15					Thomas M. Hess			
D	Add device 03. Editorial changes throughout.										95-09-26					Monica Poelking			

REV																			
SHEET																			
REV	D	D	D	D	D	D	D	D	D	D	D								
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Todd D. Creek	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444										
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin											MICROCIRCUIT, DIGITAL, CMOS, 32-BIT DMA CONTROLLER WITH INTEGRATED SYSTEM SUPPORT PERIPHERALS, MONOLITHIC SILICON
	APPROVED BY Michael Frye											
	DRAWING APPROVAL DATE 89-06-23											
		REVISION LEVEL D	SIZE A	CAGE CODE 67268	5962-89593							
		SHEET		1	OF		25					

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5962-E258-95

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0013886 11T

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89593	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	82380	32-bit DMA controller with integrated system support peripherals	16 MHz
02	82380	32-bit DMA controller with integrated system support peripherals	20 MHz
03	82380	32-bit DMA controller with integrated system support peripherals	25 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	164	Leaded chip carrier leads
Z	CMGA6-P132	132	Pin grid array package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature range - - - - -	-65°C to +150°C
Voltage on any pin with respect to ground - - - - -	-0.5 V dc to +6.5 V dc
Power dissipation (P_D) - - - - -	2.0 W
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Z - - - - -	See MIL-STD-1835
Case Y - - - - -	+8°C/W
Junction temperature (T_J) - - - - -	+175°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) - - - - -	-55°C to +125°C
Supply voltage range (V_{CC}) - - - - -	+4.75 V dc to +5.25 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89593
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STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE 1. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Devic type	Limits		Unit
					Min	Max	
Input low voltage	V _{IL}		1,2,3	A11	-0.3 1/	0.8	V
Input high voltage	V _{IH}		1,2,3		2.0	V _{CC} 1/ 0.3	V
CLK2 input low voltage	V _{ILC}		1,2,3		-0.3 1/	0.8	V
CLK2 input high voltage	V _{IHC}		1,2,3		V _{CC} 0.8	V _{CC} 1/ 0.3	V
Output low voltage	V _{OL}	I _{OL} = 4 mA: A ₂ -A ₃₁ , D ₀ -D ₃₁ , I _{OL} = 5 mA: all others	1,2,3			0.45	V
Output high voltage	V _{OH}	I _{OH} = -1 mA: A ₂ -A ₃₁ , D ₀ -D ₃₁ , I _{OH} = -0.9 mA: all others	1,2,3		2.4		V
Input leakage current	I _{LI}	All inputs except: <u>TRQ11</u> - <u>TRQ23</u> , EOP, TOUT2/TRQ3 DREQ4, 0 < V _{IN} < V _{CC}	1,2,3		-15	+15	μA
Input leakage current	I _{LI1}	Inputs: <u>TRQ11</u> - <u>TRQ23</u> EOP, TOUT2/TRQ3, DREQ4 0 < V _{IN} < V _{CC} 2/	1,2,3			325	μA
Output leakage current	I _{LO}	0 < V _{OUT} < V _{CC}	1,2,3		-15	+15	μA
Supply current	I _{CC}	CLK2 = 32 Mhz	1,2,3	01		240	mA
		3/ CLK2 = 40 Mhz		02		248	
		3/ CLK2 = 50 Mhz		03		375	
Input capacitance	C _I	f = 1 Mhz See 4.3.1c	4	A11		12	pF
CLK2 input capacitance	C _{CLK}		4	A11		20	pF
Functional tests		4.75 V ≤ V _{CC} ≤ 5.25 V See 4.3.1d	7,8	A11			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating frequency	f _{MAX}	See figure 4	9,10,11	01 02	4 4	16 20	MHz
CLK2 period time	t ₁		9,10,11	01 02 03	31.25 25 20	125 125 125	ns
CLK2 high time	t _{2a}	Measured at 2.0 V See figure 4	9,10,11	01 02 03	9 8 7		ns
CLK2 high time 1/	t _{2b}	Measured at V _{CC} -0.8 V See figure 4	9,10,11	01 02 03	5 5 4		ns
CLK2 low time	t _{3a}	Measured at 2.0 V See figure 4	9,10,11	01 02 03	9 8 7		ns
CLK2 low time 1/	t _{3b}	Measured at 0.8 V See figure 4	9,10,11	01 02 03	7 6 4		ns
CLK2 fall time 1/	t ₄	Measured from V _{CC} -0.8 V to 0.8 V, see figure 4	9,10,11	01 02 03		8 8 7	ns
CLK2 rise time 1/	t ₅	Measured from 0.8 V to V _{CC} -0.8 V, see figure 4	9,10,11	01 02 03		8 8 7	ns
A ₂ -A ₃₁ , $\overline{BE}_0$ - $\overline{BE}_3$, EDACK ₀ -EDACK ₂ valid delay	t ₆	See figure 4	9,10,11	01 02 03	4 4 4	36 30 20	ns
A ₂ -A ₃₁ , $\overline{BE}_0$ - $\overline{BE}_3$, float delay 1/	t ₇		9,10,11	01 02	4 4	40 32	ns
A ₂ -A ₃₁ , $\overline{BE}_0$ - $\overline{BE}_3$, setup times	t ₈		9,10,11	A11	6		ns
A ₂ -A ₃₁ , $\overline{BE}_0$ - $\overline{BE}_3$, hold time	t ₉		9,10,11	A11	4		ns
W/ $\overline{R}$, M/ $\overline{TO}$, D/ $\overline{C}$ valid delay	t ₁₀		9,10,11	01 02 03	6 6 4	33 28 20	ns
W/ $\overline{R}$, M/ $\overline{TO}$, D/ $\overline{C}$ float 1/ delay	t ₁₁		9,10,11	01 02 03	4 4 4	35 30 29	ns
W/ $\overline{R}$, M/ $\overline{TO}$, D/ $\overline{C}$ setup	t ₁₂		9,10,11	A11	6		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
W/ $\overline{R}$, M/ $\overline{IO}$, D/ $\overline{C}$ hold time	t ₁₃	See figure 4	9,10,11	All	4		ns
$\overline{ADS}$ valid delay	t ₁₄		9,10,11	01	6	33	ns
				02	6	28	
				03	4	19	
$\overline{ADS}$ float delay $\frac{1}{f}$	t ₁₅		9,10,11	01	4	35	ns
				02	4	30	
				03	4	29	
ADS setup time	t ₁₆		9,10,11	01	21		ns
				02	15		
				03	12		
$\overline{ADS}$ hold time	t ₁₇		9,10,11	All	4		ns
Slave mode D ₀ -D ₃₁ read	t ₁₈		9,10,11	01	3	46	ns
				02	4	46	
				03	4	31	
Slave mode D ₀ -D ₃₁ read float delay $\frac{1}{f}$	t ₁₉		9,10,11	01	6	35	ns
				02	6	29	
				03	6	21	
Slave mode D ₀ -D ₃₁ write setup time	t ₂₀		9,10,11	01	31		ns
				02	29		
				03	20		
Slave mode D ₀ -D ₃₁ write hold time	t ₂₁		9,10,11	01	26		ns
				02	26		
				03	20		
Master mode D ₀ -D ₃₁ write valid delay	t ₂₂		9,10,11	01	4	48	ns
				02	4	38	
				03	6	27	
Master mode D ₀ -D ₃₁ write float delay $\frac{1}{f}$	t ₂₃		9,10,11	01	4	35	ns
				02	4	27	
				03	4	19	
Master mode D ₀ -D ₃₁ read setup time	t ₂₄		9,10,11	01	11		ns
				02	11		
				03	7		
Master mode D ₀ -D ₃₁ read hold time	t ₂₅		9,10,11	01	6		ns
				02	6		
				03	4		
READY setup time	t ₂₆		9,10,11	01	21		ns
				02	12		
				03	9		
READY hold time	t ₂₇		9,10,11	All	4		ns
WSCO-WSC1 setup time	t ₂₈		9,10,11	All	6		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
WSCO-WSC1 hold time	t ₂₉	See figure 4	9,10,11	01	21		ns
				02	21		
				03	15		
RESET hold time	t ₃₀		9,10,11	01	4		ns
				02	4		
				03	4		
RESET setup time	t ₃₁		9,10,11	01	13		ns
				02	12		
				03	9		
READY0 valid delay	t ₃₂		9,10,11	01	4	31	ns
				02	4	28	
				03	3	21	
CPU reset delay	t ₃₃		9,10,11	01	2	18	ns
				02	2	16	
				03	2	14	
Hold delay	t ₃₄		9,10,11	01	5	33	ns
				02	5	30	
				03	4	22	
HLDA setup time	t ₃₅		9,10,11	01	21		ns
				02	17		
				03	17		
HLDA hold time	t ₃₆		9,10,11	01	6		ns
				02	6		
				03	4		
EOP setup time	t _{37a}		9,10,11	01	21		ns
				02	17		
				03	13		
EOP hold time	t _{38a}		9,10,11	A11	4		ns
EOP setup time	t _{37b}		9,10,11	01	11		ns
				02	11		
				03	10		
EOP hold time	t _{38b}		9,10,11	01	11		ns
				02	11		
				03	10		
EOP valid delay	t ₃₉		9,10,11	01	5	38	ns
				02	5	30	
				03	4	21	
EOP float delay 1/	t ₄₀		9,10,11	01	5	40	ns
				02	5	32	
				03	4	21	

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DREQ setup time	t _{41a}	Synchronous See figure 4	9,10,11	01	21		ns
				02	19		
				03	17		
DREQ hold time	t _{42a}		9,10,11	A11	4		ns
DREQ setup time	t _{41b}		9,10,11	01	11		ns
				02	11		
				03	4		
DREQ hold time	t _{42b}		9,10,11	01	11		ns
				02	11		
				03	10		
INT valid delay	t ₄₃	See figure 4	9,10,11	A11		500	ns
$\overline{NA}$ setup time	t ₄₄	See figure 4	9,10,11	01	11		ns
				02	10		
				03	7		
$\overline{NA}$ hold time	t ₄₅		9,10,11	01	15		ns
				02	15		
				03	8		
CLKIN frequency	t ₄₆		9,10,11	A11	0 ^{1/}	10	MHz
CLKIN high time	t ₄₇	Measured at 2.0 V See figure 4	9,10,11	A11	30		ns
CLKIN low time	t ₄₈	Measured at 0.8 V See figure 4	9,10,11	A11	50		ns
CLKIN rise time ^{1/}	t ₄₉	Measured from 0.8 V to V _{CC} -0.8 V, see figure 4	9,10,11	A11		10	ns
CLKIN fall time ^{1/}	t ₅₀	Measured from V _{CC} -0.8 V to 0.8 V	9,10,11	A11		10	ns
TOUT1/REF valid from CLK2	t ₅₁	See figure 4 ^{4/}	9,10,11	01	4	36	ns
				02	4	30	
				03	4	20	
TOUT1/REF valid from CLKIN	t ₅₂		9,10,11	01	3	93	ns
				02	3	93	
				03	3	90	
TOUT2 valid delay	t ₅₃		9,10,11	01	3	93	ns
				02	3	93	
				03	3	90	
TOUT2 float delay	t ₅₄		9,10,11	01	3	40	ns
				02	3	40	
				03	3	37	
TOUT3 valid delay	t ₅₅		9,10,11	01	3	93	ns
				02	3	93	
				03	3	90	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ Guaranteed to the limit specified herein, if not tested.
- 2/ These pins should not be left floating.
- 3/ I_{CC} is specified with inputs driven to CMOS levels, and outputs driving CMOS loads. I_{CC} may be higher if inputs are driven to TTL levels, or if outputs are driving TTL loads.
- 4/ All outputs loaded to 50 pf.

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Case Y

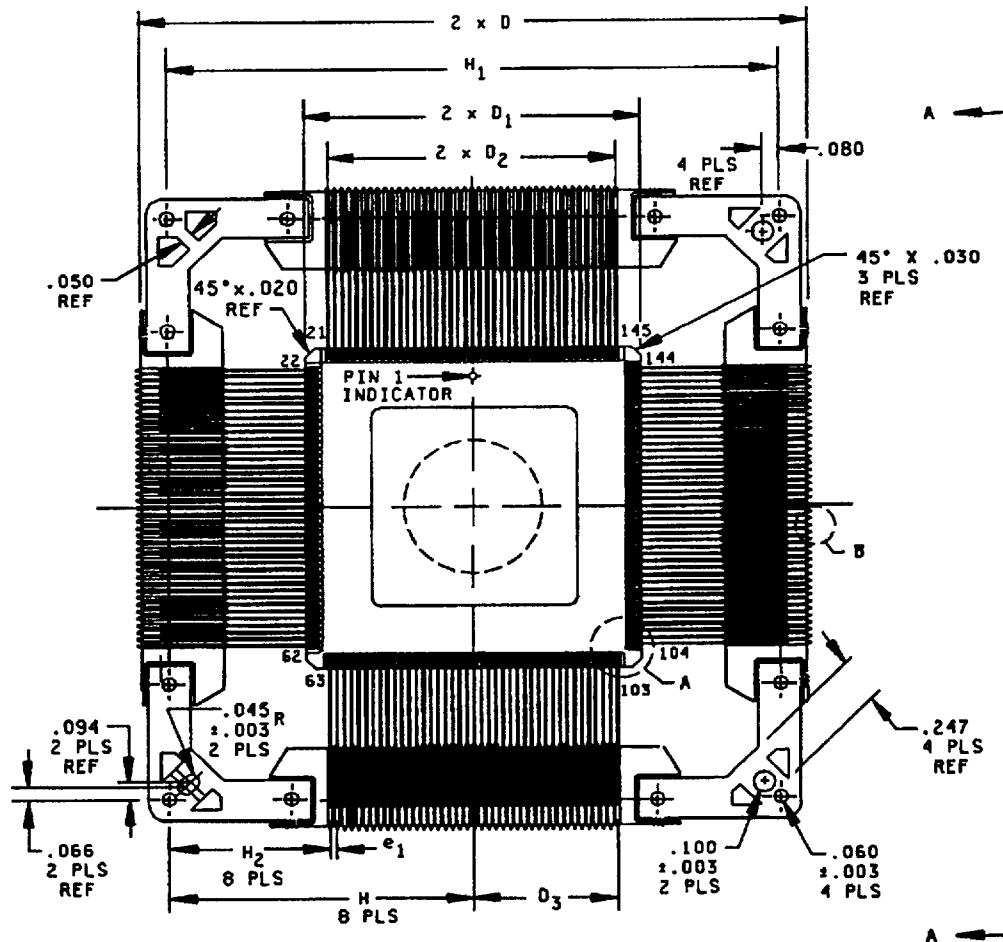


FIGURE 1. Case outline.

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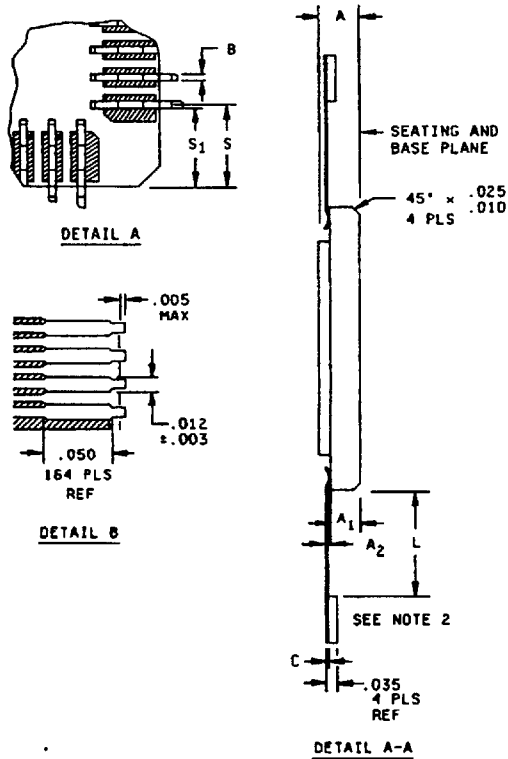
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Case Y



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.088	.115	2.23	2.92
A ₁	.078	.094	1.98	2.39
A ₂	.006	.012	0.15	0.30
B	.007	.010	0.18	0.25
C	.004	.006	0.10	0.15
D	2.480	2.520	63.00	64.01
D ₁	1.120	1.140	28.45	28.96
D ₂	1.00	BASIC	25.40	BASIC
D ₃	.500	BASIC	12.70	BASIC
e ₁	.023	.027	0.58	0.69
H	1.150	BASIC	29.21	BASIC
H ₁	2.30	BASIC	58.42	BASIC
H ₂	.650	BASIC	16.51	BASIC
L	.365	.395	9.27	10.03
N	164 TERMINALS			
S	.060	.080	1.52	2.03
S ₁	.060	.076	1.52	1.93

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbols B and C dimensions shall be increased by .002 inch when solder coat is added.

FIGURE 1. Case outline - Continued.

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Case Y

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	A ₄	28	A ₂₂	55	D ₁₃	82	D ₁
2	V _{CC}	29	V _{SS}	56	D ₅	83	D ₂₄
3	V _{SS}	30	V _{CC}	57	D ₂₈	84	D ₁₆
4	A ₅	31	A ₂₃	58	D ₂₀	85	D ₈
5	A ₆	32	A ₂₄	59	D ₁₂	86	D ₀
6	A ₇	33	A ₂₅	60	V _{CC}	87	V _{SS}
7	A ₈	34	A ₂₆	61	V _{SS}	88	V _{CC}
8	A ₉	35	A ₂₇	62	NC	89	READY ₀
9	V _{CC}	36	A ₂₈	63	NC	90	TOUT1/REF
10	V _{SS}	37	A ₂₉	64	V _{CC}	91	HOLD
11	A ₁₀	38	A ₃₀	65	D ₄	92	M/T ₀
12	A ₁₁	39	A ₃₁	66	D ₂₇	93	V _{SS}
13	A ₁₂	40	NC	67	D ₁₉	94	V _{CC}
14	A ₁₃	41	D ₃₁	68	D ₁₁	95	NC
15	V _{CC}	42	D ₂₃	69	D ₃	96	NC
16	V _{SS}	43	D ₁₅	70	D ₂₆	97	W/R
17	A ₁₄	44	D ₇	71	D ₁₈	98	D/C
18	A ₁₅	45	D ₃₀	72	D ₁₀	99	TOUT3
19	A ₁₆	46	V _{SS}	73	D ₂	100	TOUT2/TRQ3
20	A ₁₇	47	V _{CC}	74	V _{SS}	101	CPURST
21	NC	48	D ₂₂	75	V _{CC}	102	NC
22	NC	49	D ₁₄	76	D ₂₅	103	V _{CC}
23	V _{CC}	50	D ₆	77	D ₁₇	104	V _{SS}
24	A ₁₈	51	V _{SS}	78	D ₉	105	V _{CC}
25	A ₁₉	52	V _{CC}	79	V _{SS}	106	NC
26	A ₂₀	53	D ₂₉	80	CLK2	107	V _{SS}
27	A ₂₁	54	D ₂₁	81	V _{SS}	108	V _{CC}

FIGURE 2. Terminal connections.

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Case Y

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
109	READY	123	TRQ18	137	NA	151	EDACK1
110	RESET	124	TRQ19	138	DREQ6	152	EDACK2
111	WSC1	125	TRQ20	139	DREQ7	153	V _{CC}
112	WSC0	126	TRQ21	140	V _{CC}	154	V _{SS}
113	V _{SS}	127	TRQ22	141	V _{SS}	155	EOP
114	CLKIN	128	TRQ23	142	NC	156	ADS
115	V _{CC}	129	V _{CC}	143	NC	157	BE ₀
116	TRQ11	130	V _{SS}	144	NC	158	BE ₁
117	TRQ12	131	DREQ0	145	NC	159	BE ₂
118	TRQ13	132	DREQ1	146	HLDA	160	BE ₃
119	TRQ14	133	DREQ2	147	INT	161	V _{CC}
120	TRQ15	134	DREQ3	148	NC	162	V _{SS}
121	TRQ16	135	DREQ4/TRQ9	149	NC	163	A ₂
122	TRQ17	136	DREQ5	150	EDACK0	164	A ₃

FIGURE 2. Terminal connections - Continued.

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Pin/signal		Pin/signal		Pin/signal		Pin/signal	
A7	A ₃₁	A8	D ₃₁	P12	V _{CC}	L14	V _{SS}
C7	A ₃₀	B9	D ₃₀	M14	V _{CC}	A1	V _{SS}
B7	A ₂₉	A11	D ₂₉	P1	V _{CC}	P13	V _{SS}
A6	A ₂₈	C11	D ₂₈	P2	V _{CC}	N1	V _{SS}
B6	A ₂₇	D12	D ₂₇	P14	V _{CC}	N2	V _{SS}
C6	A ₂₆	E13	D ₂₆	D1	V _{CC}	C1	V _{SS}
A5	A ₂₅	F14	D ₂₅	C14	V _{CC}	A3	V _{SS}
B5	A ₂₄	J13	D ₂₄	B1	V _{CC}	B14	V _{SS}
C5	A ₂₃	B8	D ₂₃	A2	V _{CC}	A13	V _{SS}
B4	A ₂₂	C9	D ₂₂	A4	V _{CC}	N14	V _{SS}
B3	A ₂₁	B11	D ₂₁	A12	V _{CC}	P6	IRQ23
C4	A ₂₀	B13	D ₂₀	A14	V _{CC}	N6	IRQ22
B2	A ₁₉	D13	D ₁₉	G14	CLK2	M7	IRQ21
C3	A ₁₈	E14	D ₁₈	L12	D/C	N7	IRQ20
C2	A ₁₇	G12	D ₁₇	K12	W/R	P7	IRQ19
D3	A ₁₆	H13	D ₁₆	L13	M/I _O	P8	IRQ18
D2	A ₁₅	C8	D ₁₅	K2	ADS	M8	IRQ17
E3	A ₁₄	A10	D ₁₄	N4	NA	N8	IRQ16
E2	A ₁₃	C10	D ₁₃	J12	HOLD	P9	IRQ15
E1	A ₁₂	C12	D ₁₂	M3	HLDA	N9	IRQ14
F3	A ₁₁	D14	D ₁₁	M6	DREQ0	M9	IRQ13
F2	A ₁₀	F12	D ₁₀	P5	DREQ1	N10	IRQ12
F1	A ₉	G13	D ₉	N5	DREQ2	P10	IRQ11
G1	A ₈	K14	D ₈	P4	DREQ3	M2	INT
G2	A ₇	A9	D ₇	M5	DREQ4/IRQ9	N11	CLKIN
G3	A ₆	B10	D ₆	P3	DREQ5	K13	TOUT1/REF
H1	A ₅	B12	D ₅	M4	DREQ6	N13	TOUT2/IRQ3
H2	A ₄	C13	D ₄	N3	DREQ7	M13	TOUT3
J1	A ₃	E12	D ₃	K3	EOP	M11	READY
H3	A ₂	F13	D ₂	L3	EDACK0	H12	READY0
J2	BE ₃	H14	D ₁	M1	EDACK1	P11	WSCO
J3	BE ₂	J14	D ₀	L2	EDACK2	M10	WSC1
K1	BE ₁	N12	RESET				
L1	BE ₀	M12	CPURST				

FIGURE 2. Terminal connections - Continued.

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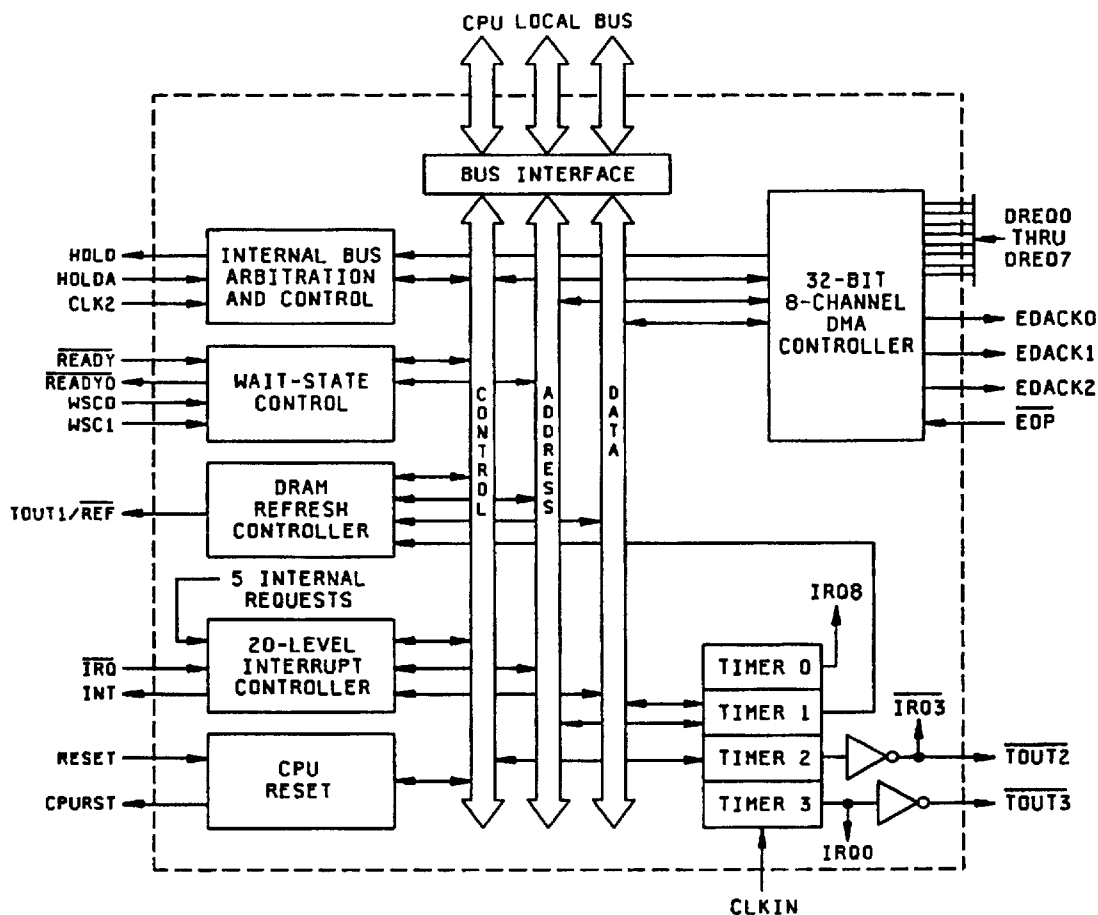


FIGURE 3. Functional block diagram.

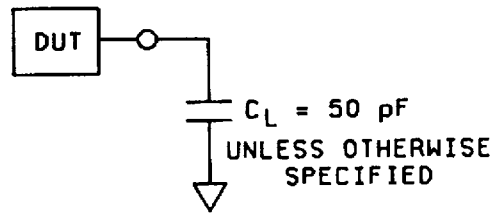
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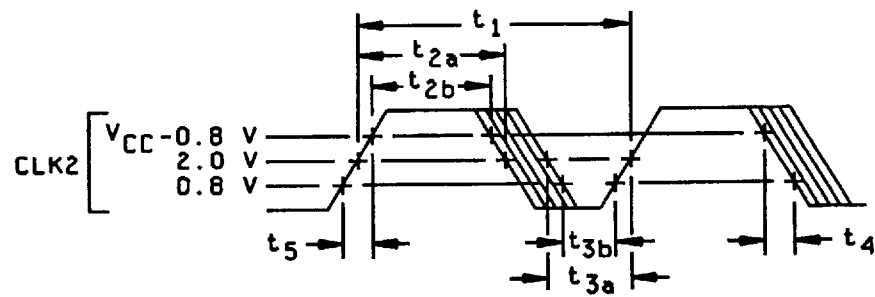
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AC TEST CIRCUIT



CLK2 TIMING

NOTE: All ac timings are tested at 1.5 V threshold, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms.

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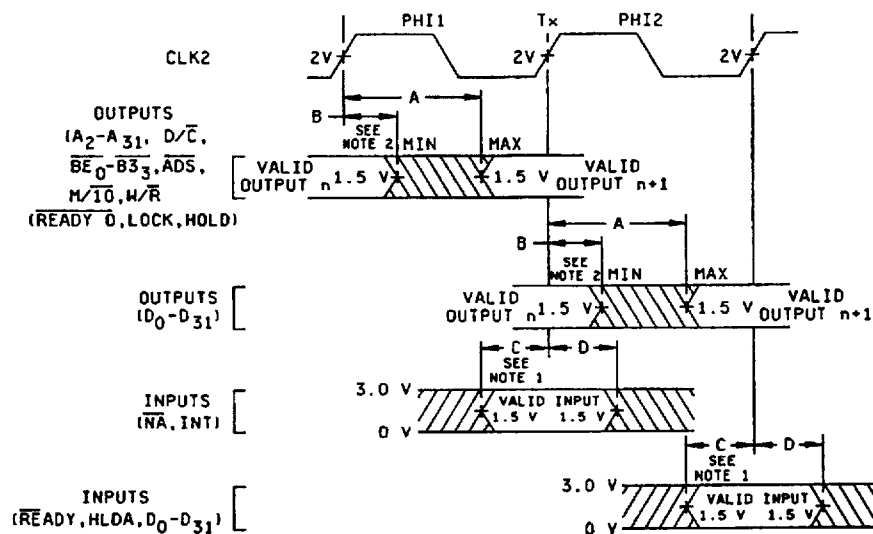
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LEGEND:

- A - Maximum output delay specification.
- B - Minimum output delay specification.
- C - Minimum input setup specification.
- D - Minimum input hold specification.

NOTES:

1. Input waveforms have $t_r \leq 2$ ns from 0.8 V to 2 V.
2. Under rated loading (120 pF): output t_r , t_f is typically ≤ 4 ns from 0.8 V to 2 V.
3. All timing measurements are tested at 1.5 V, unless otherwise specified.

Drive levels and measurements points for ac specification.

FIGURE 4. AC test circuit and timing waveforms - Continued.

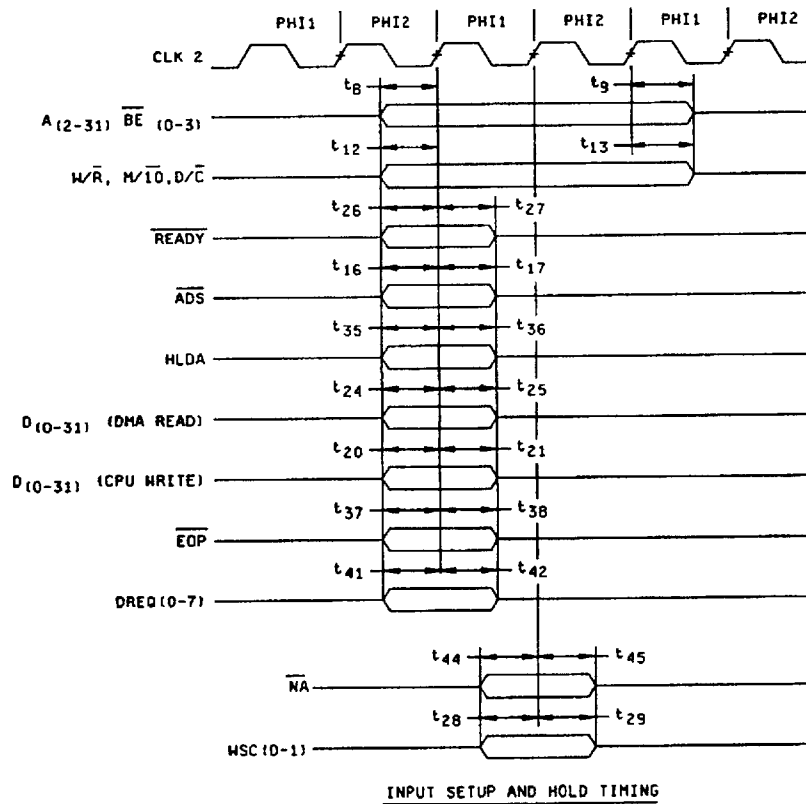
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NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.

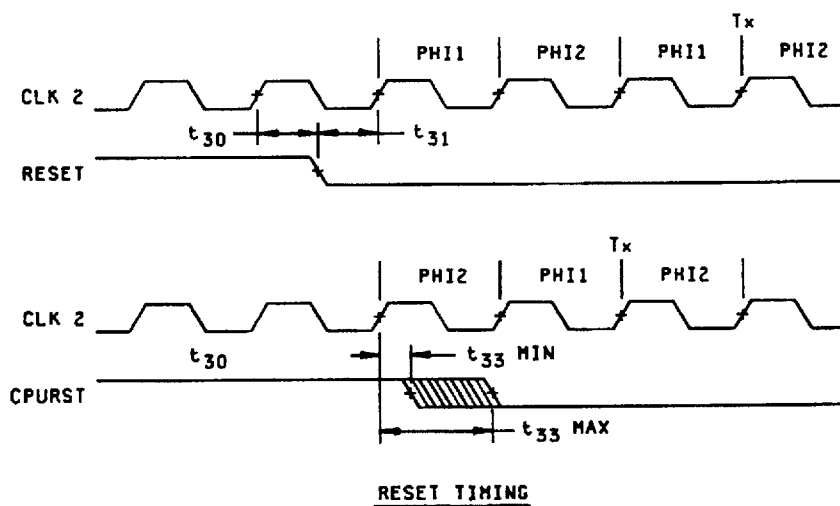
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NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.

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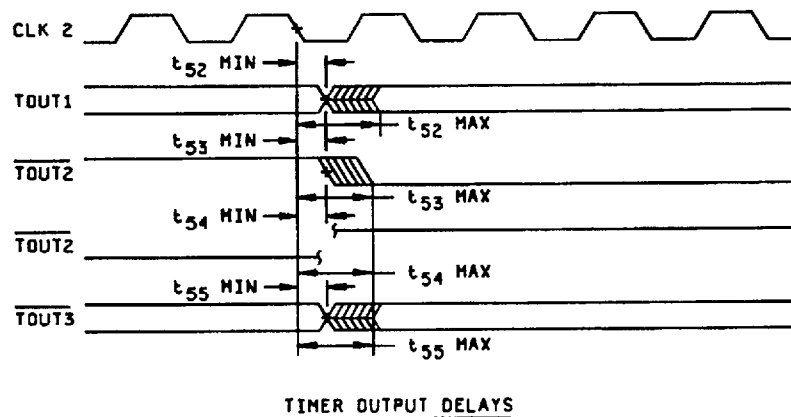
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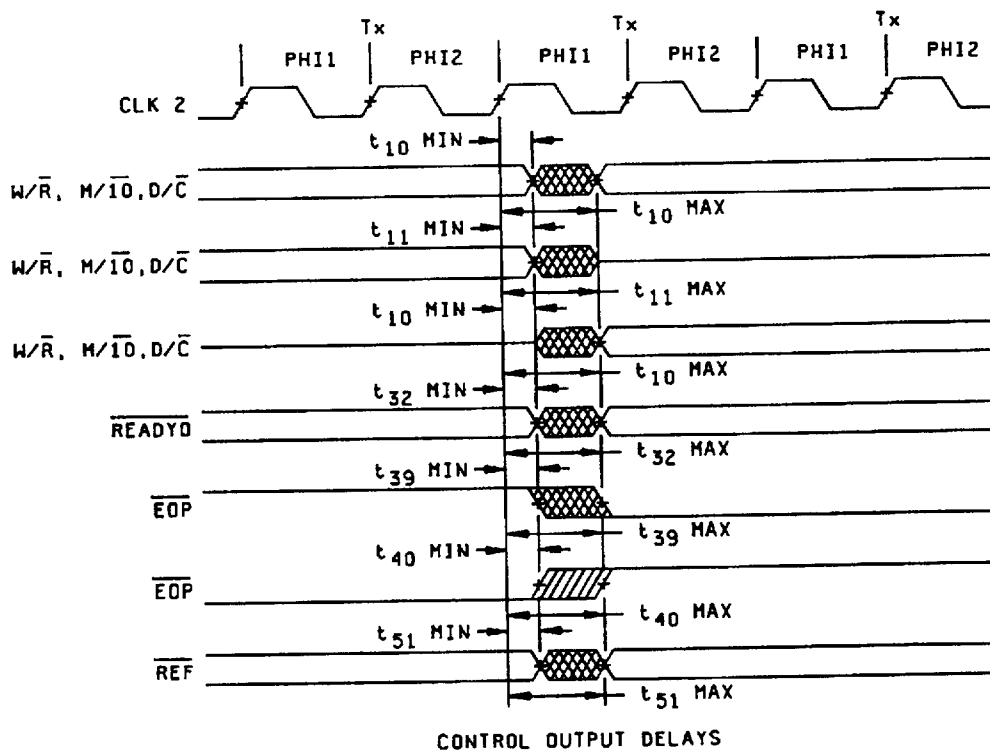
NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.

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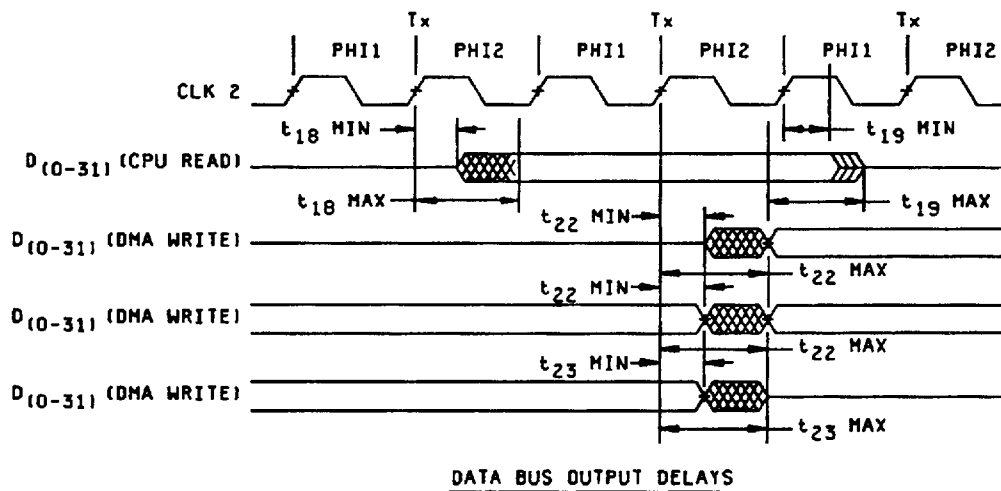
NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.

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NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 7*, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8a, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{CLK} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the functionality of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from the approved source of supply..

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4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.7 Pin descriptions.

Pin name	I/O	Description
A_0-A_{31}	I/O	Address bus. This is the 32-bit address bus. The addresses are doubleword memory and I/O addresses. These are three-state signals which are active active only during master mode. The address lines should be connected directly to the CPU's local bus.
D_0-D_{31}	I/O	Data bus. This is the 32-bit data bus. These pins are active outputs during interrupt acknowledges, during slave accesses, and when the device is in the master mode.
CLK2	I	Processor clock. This pin must be connected to CLK2. The device monitors the phase of this clock in order to remain synchronized with the CPU. This clock drives all of the internal synchronous circuitry.
$D/\bar{C}$	I/O	Data/control. $D/\bar{C}$ is used to distinguish between CPU control cycles and DMA or CPU data access cycles. It is active as an output only in the master mode.

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Pin name	I/O	Description - Continued.
$\overline{BE}_0$	I/O	Byte enable 0. $\overline{BE}_0$ active indicates that data bits D_0-D_7 are being accessed or are valid. It is connected directly to the CPU's $\overline{BE}_0$. The byte enable signals are active outputs when the device is in the master mode.
$\overline{BE}_1$	I/O	Byte enable 1. $\overline{BE}_1$ active indicates that data bits D_8-D_{15} are being accessed or are valid. It is connected directly to the CPU's $\overline{BE}_1$. The byte enable signals are active only when the device is in the master mode.
$\overline{BE}_2$	I/O	Byte enable 2. $\overline{BE}_2$ active indicates that data bits $D_{16}-D_{23}$ are being accessed or are valid. It is connected directly to the CPU's $\overline{BE}_2$. The byte enable signals are active only when the device is in the master mode.
$\overline{BE}_3$	I/O	Byte enable 3. $\overline{BE}_3$ active indicates that data bits $D_{24}-D_{31}$ are being accessed or are valid. The byte enable signals are active only when the device is in the master mode. This pin should be connected directly to the CPU's $\overline{BE}_3$. This pin is used for factory testing and must be low during reset. The CPU drives $\overline{BE}_3$ low during reset.
HOLD	0	Hold request. This is an active-high signal to the CPU to request control of the system bus. When control is granted, the CPU activates the hold acknowledge signal (HLDA).
HLDA	1	Hold acknowledge. This input signals tells the DMA controller that the CPU has relinquished control of the system bus to the DMA controller.

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