REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
SHEET																									
REV																									
SHEET																									

REV STATUS OF SHEETS																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15							

PMIC N/A	PREPARED BY Larry T. Gauder	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, FAST, CMOS, 9-BIT WIDE BUFFERED REGISTERS, MONOLITHIC SILICON
	APPROVED BY	
	DRAWING APPROVAL DATE 30 NOVEMBER 1989	SIZE A | CAGE CODE 67268 | 5962-89665
AMSC N/A	REVISION LEVEL	SHEET 1 OF 15

DESC FORM 193
SEP 87

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1320

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89665	01	K	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT824A	9-bit wide buffered registers, TTL compatible, with inverted three-state outputs
02	54FCT824B	9-bit wide buffered registers, TTL compatible, with inverted three-state outputs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK})	-20 mA
DC output diode current (I_{OK})	-50 mA
DC output current	±100 mA
Maximum power dissipation (P_D) 2/	500 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Case operating temperature (T_C)	-55°C to +125°C

1/ All voltages referenced to GND.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10 percent unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OH} = -300 µA	All	1,2,3	4.3		V
			I_{OH} = -15 mA	All	1,2,3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OL} = 300 µA	All	1,2,3		0.2	V
			I_{OL} = 32 mA	All	1,2,3		0.5	V
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		All	1		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1,2,3		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		All	1,2,3		-5.0	µA
High impedance output current	I_{OZH}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V or GND		All	1,2,3		±10	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/ V_{OUT} = GND		All	1,2,3	-75		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V, V_{CC} = 5.5 V, $f_I = f_{CP}$ = 0 MHz		All	1,2,3		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V 2/		All	1,2,3		2.0	mA
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $\overline{OE}$ = GND, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V, Outputs open, one bit toggling: 50 percent duty cycle		All	3/		0.25	mA/MHz

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ $V_{CC} = 5.0$ V dc ±10 percent unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Total power supply current 4/	I_{CC}	$V_{IN} \geq 5.3$ V or $V_{IN} \leq 0.2$ V, $V_{CC} = 5.5$ V, $f_{CP} = 10$ MHz, Outputs open, one bit toggling at $f_I = 5$ MHz 50 percent duty cycle, $\overline{OE}$ = GND		All	1,2,3		4.0	mA
		$V_{IN} = 3.4$ V or V_{IN} = GND, $V_{CC} = 5.5$ V, $f_{CP} = 10$ MHz, Outputs open, one bit toggling at $f_I = 5$ MHz 50 percent duty cycle, $\overline{OE}$ = GND					6.0	mA
Functional tests		See 4.3.1d		All	7,8			
Input capacitance	C_{IN}	See 4.3.1c		All	4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c		All	4		12	pF
Propagation delay time, CP to Y_i ($\overline{OE}$ = low)	t_{PLH1}, t_{PHL1}	$R_L = 500\Omega$, see figure 3	$C_L = 50$ pF	01	9,10,11		11.5	ns
				02			8.5	
			$C_L = 300$ pF 5/	01	9,10,11		20.0	ns
				02			16.0	
Propagation delay time, $\overline{CLR}$ to Y_i	t_{PHL2}		$C_L = 50$ pF	01	9,10,11		15.0	ns
				02			9.5	
Output enable time, $\overline{OE}$ (low-to-high) to Y_i	t_{PZH}, t_{PZL}		$C_L = 50$ pF	01	9,10,11		13.0	ns
				02			9.0	
			$C_L = 300$ pF 5/	01	9,10,11		25.0	ns
				02			16.0	

See footnotes at end of table.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ\text{C} \le T_C \le +125^\circ\text{C}$ V_{CC} = 5.0 V dc ±10 percent unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Output disable time, $\overline{OE}$ (low-to-high) to Y_i	t_{PHZ}, t_{PLZ}	R_L = 500Ω, see figure 3	C_L = 50 pF	01	9,10,11		9.0	ns
				02			7.0	
			C_L = 5.0 pF 5/	01	9,10,11		8.0	ns
				02			8.0	
Setup time, Dn to CP	t_{S1}	C_L = 50 pF, R_L = 500Ω, see figure 3		01	9,10,11	4.0		ns
				02		3.0		
Setup time, $\overline{EN}$ to CP	t_{S2}			01	9,10,11	4.0		ns
				02		3.0		
$\overline{CLR}$ recovery time	t_{rec}			01	9,10,11	7.0		ns
				02		6.0		
Hold time, Dn to CP	t_{h1}			01	9,10,11	2.0		ns
				02		1.5		
Hold time, $\overline{EN}$ to CP	t_{h2}			01	9,10,11	2.0		ns
				02		0.0		

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ V_{CC} = 5.0 V dc ±10 percent unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Clock pulse width	t_{PWH1}, t_{PWL1}	$R_L = 500\Omega$, C_L = 50 pF, see figure 3	01	9,10,11	7.0		ns
			02		6.0		
$\overline{CLR}$ pulse width	t_{PWL2}		01	9,10,11	7.0		ns
			02		6.0		

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed one second.

2/ TTL driven inputs at V_{IN} = 3.4 V; all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + (I_{CCD}(f_I \times N_I + f_{CP}/2))$

where: D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
f_I = Input frequency in MHz
N_I = Number of inputs at f_I
f_{CP} = Clock frequency in MHz

5/ This parameter is guaranteed if not tested, to the limits specified in table I.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Device types	All	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	$\overline{\text{OE}}$	NC
2	D0	$\overline{\text{OE}}$
3	D1	D0
4	D2	D1
5	D3	D2
6	D4	D3
7	D5	D4
8	D6	NC
9	D7	D5
10	D8	D6
11	$\overline{\text{CLR}}$	D7
12	GND	D8
13	CP	$\overline{\text{CLR}}$
14	$\overline{\text{EN}}$	GND
15	Y8	NC
16	Y7	CP
17	Y6	$\overline{\text{EN}}$
18	Y5	Y8
19	Y4	Y7
20	Y3	Y6
21	Y2	Y5
22	Y1	NC
23	Y0	Y4
24	V_{CC}	Y3
25	---	Y2
26	---	Y1
27	---	Y0
28	---	V_{CC}

FIGURE 1. Terminal connections.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Inputs					Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	Dn	CP	Y_i	
H H	X X	L L	L H	↑ ↑	Z Z	High Z
H L	L L	X X	X X	X X	Z L	Clear
H L	H H	H H	X X	X X	Z NC	Hold
H H L L	H H H H	L L L L	L H L H	↑ ↑ ↑ ↑	Z Z H L	Load

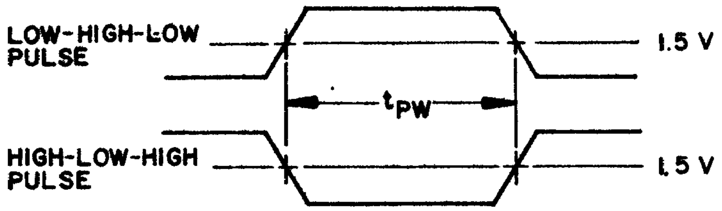
H = High voltage level
L = Low voltage level
X = Irrelevant
NC = No change
Z = High impedance state
↑ = Low to high transition

FIGURE 2. Truth table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Pulse width



Propagation delay

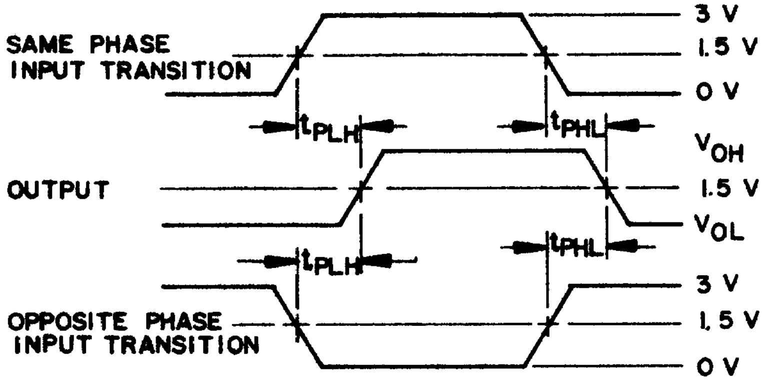
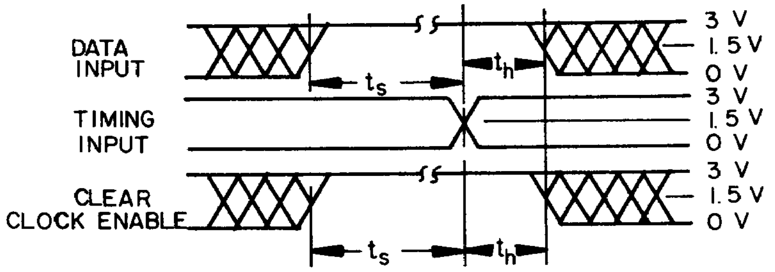


FIGURE 3. Switching times waveforms and test circuit.

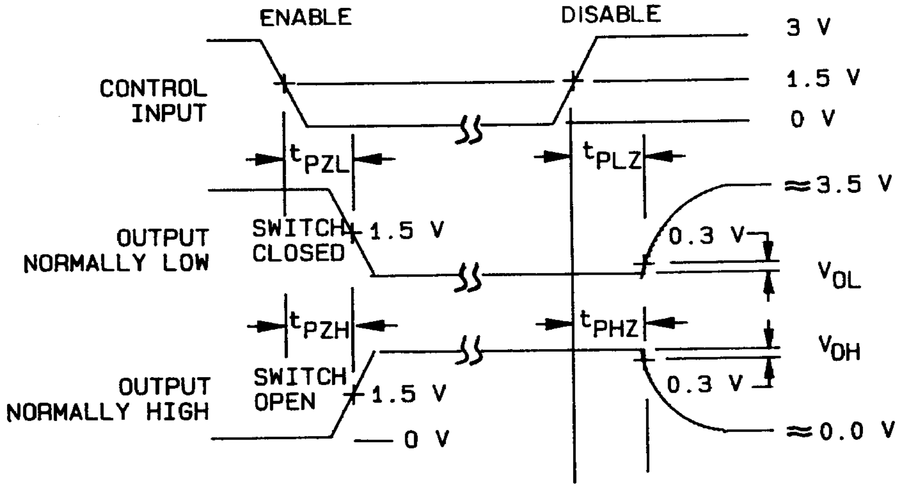
☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Setup and hold times



Enable and disable times



NOTES:

1. Diagram shown for input control enable: Low; input; control disable: High.
2. Pulse generator for all pulses: $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

FIGURE 3. Switching times waveforms and test circuit - Continued.

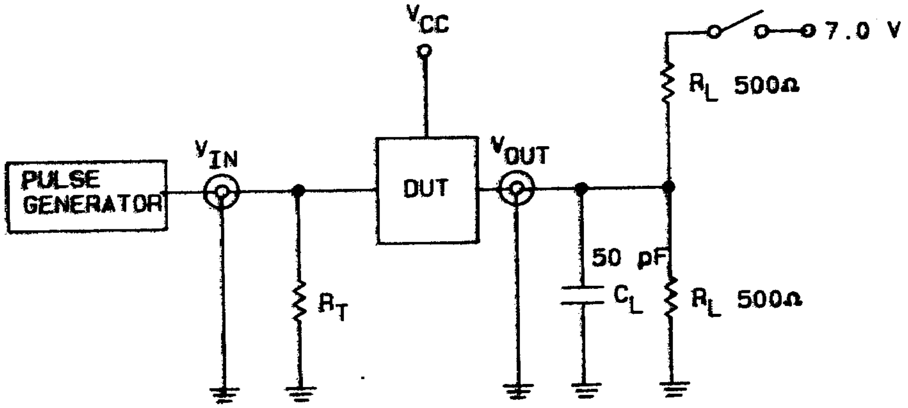
STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE A		5962-89665
	REVISION LEVEL	**SHEET** 11

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Test circuits for three-state outputs



Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
All other	Open

NOTES:

1. C_L includes probe and jig capacitance.
2. R_T should be equal to Z_{OUT} of the pulse generator.
3. Pulse generator for all pulses: PRR $\leq$ 1.0 MHz, $Z_{OUT} \leq 50\Omega$, $t_r = t_f = 2.5$ ns.

FIGURE 3. Switching waveforms and test circuit - Continued.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

  (2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.

d. Subgroup 7 and 8 tests shall verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

  (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

  (2) T_A = +125°C, minimum.

  (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

Powered by ICminer.com Electronic-Library Service CopyRight 2003

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8966501KX	61772	IDT54FCT824AEB
5962-8966501LX	61772	IDT54FCT824ADB
5962-89665013X	61772	IDT54FCT824ALB
5962-8966502KX	61772	IDT54FCT824BEB
5962-8966502LX	61772	IDT54FCT824BDB
5962-89665023X	61772	IDT54FCT824BLB

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology 1566 Moffett Boulevard Salinas, CA 93905 Point of contact: 3236 Scott Boulevard Santa Clara, CA 95054

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

Powered by ICminer.com Electronic-Library Service CopyRight 2003