REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to the small signal response time test as specified in table I.	98-03-13	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A				
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10				

PMIC N/A	PREPARED BY RICK C. OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MIROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY CHARLES E. BESORE	
	APPROVED BY MONICA L. POELKING	MICROCIRCUIT, LINEAR, QUAD, LOW POWER PRECISION COMPARATOR, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 90-04-27	
	REVISION LEVEL A	SIZE A CAGE CODE 67268 **5962-89904** SHEET 1 OF 10

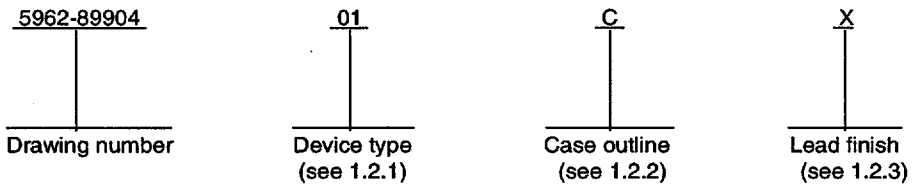
DSC FORM 2233
APR 97

5962-E223-98

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	CMP404A	Quad low-power precision comparator
02	CMP404B	Quad low-power precision comparator
03	CMP04B	Quad low-power precision comparator

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage ..... 36 V or ±18 V
Input voltage ..... -0.3 V to V+
Output voltage ..... -0.3 V to 36 V
Power dissipation ..... 500 mW 1/
Input current ..... 20 mA 2/
Output short-circuit to V+ ..... 50 mA 3/
Lead temperature (soldering, 60 seconds) ..... +300°C
Operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 100°C/W

1.4 Recommended operating conditions.

Supply voltage (V+) ..... 5 V
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1/ Derate at T_A above +100°C by 10 mW/°C.
2/ Limit for input current that flows when input voltage signals exceed V+ or GND biasing internal junctions.
3/ Short circuits to V+ can cause excessive heating and eventual destruction. The maximum output current is 50 mA.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V+ = 5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{OS}	$R_S = 50\ \Omega$, $V_{CM} \le 3.5$ V	1	01,03		1.0	mV
			2,3			2.0	
			1	02		2.0	
			2,3			3.0	
Input offset current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$	1	01		10.0	nA
			2,3			50.0	
			1	02		25.0	
			2,3			100.0	
			1	03		10.0	
			2,3			20.0	
Input bias current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	1	01		50.0	nA
			2,3			100.0	
			1	02,03		100.0	
			2,3			200.0	
Supply current	I+	$R_L = \infty$	1,2,3	01		300.0	µA
		V+ = 36 V, $R_L = \infty$				500.0	
		$R_L = \infty$	1,2,3	02		350.0	
		V+ = 36 V, $R_L = \infty$				550.0	
		V+ = 30 V, $R_L = \infty$	1	03		2.0	mA
			2,3			3.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V+ = 5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Common mode rejection	CMR	R_L = 15 kΩ, V_{CM} = 0 V to 3.5 V	1,2,3	01	75.0		dB
		R_L = 15 kΩ,	1	02	75.0		
		V_{CM} = 0 V to 3.0 V	2,3		65.0		
		V+ = 15 V, R_L = 15 kΩ,	1	03	80.0		
		V_{CM} = 1.5 V to 13.5 V	2,3		60.5		
Common-mode voltage 1/ range	CMVR		1	01,02		3.5	mV
			2,3			3.0	
		V+ = 15 V	1	03		13.5	
			2,3			13.0	
Power supply rejection	PSR	V+ = 5 V to 30 V,	1,2,3	01	75.0		dB
		R_L = 15 kΩ		02	65.0		
		V+ = 5 V to 18 V, R_L = 15 kΩ	1,2,3	03	80.0		
Output sink current	I_{SINK}	V_{IN+} = 0 V, V_{IN-} = 1 V, V_O = 2 V	1,2,3	01,02	10.0		mA
		V_{IN+} = 0 V, V_{IN-} = 1 V,	1	03	6.0		
		V_O = 1.5 V	2,3		5.0		
Saturation voltage	V_{OL}	V_{IN+} = 0 V, V_{IN-} = 1 V,	1	01,02		400.0	mV
		I_{SINK} = 1 mA	2,3			500.0	
		V_{IN+} = 0 V, V_{IN-} = 1 V,	1	03		400.0	
		I_{SINK} = 4 mA	2,3			700.0	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V+ = 5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output leakage current	I_{LEAK}	$V_{IN+} \ge 1$ V, $V_{IN-} = 0$ V,	1	01,02		0.1	µA
		$V_O = 30$ V	2,3			0.4	
			1	03		0.1	
			2,3			0.2	
Voltage gain	A_V	$R_L = 15$ kΩ 2/	1,2,3	01,02	50		V/mV
		$\Delta V_O = 2.4$ V		03	70		
Large-signal response time	t_r	V_{IN} = TTL logic swing,	9	01,02		1.5	µs
		$V_{REF} = 1.4$ V, $R_L = 5.1$ kΩ	10,11			1.8	
		5 V input step, $R_L = 5.1$ kΩ	9	03		0.7	
		$V_{REF} = 1.4$ V, $V_{RL} = 5$ V	10,11			1.4	
Small-signal response time	t_r	Low to high transition $V_{RL} = 5$ V, $R_L = 5.1$ kΩ 100 mV input step, 5 mV overdrive	9,10,11	01,02		1.5	µs
				03		3.0	
		High to low transition $V_{RL} = 5$ V, $R_L = 5.1$ kΩ 100 mV input step, 5 mV overdrive	9,10,11	01,02		3.5	
				03		3.0	

1/ CMVR is guaranteed by CMR test conditions. For device type 03, the input common mode voltage, or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is supply voltage -1.5 V, but either or both inputs can go to 30 V without damage.

2/ If not tested, shall be guaranteed to the limits specified in table I herein for device type 03 only.

Devcie types	01, 02, and 03
Case outline	C
Terminal number	Terminal symbol
1	OUT2
2	OUT1
3	V+
4	IN1-
5	IN1+
6	IN2-
7	IN2+
8	IN3-
9	IN3+
10	IN4-
11	IN4+
12	GND
13	OUT4
14	OUT3

FIGURE 1. Terminal connections.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1,2,3
Group A test requirements (method 5005)	1,2,3,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125° C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-03-13

Approved sources of supply for SMD 5962-89904 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8990401CA	24335	CMP404AY
5962-8990402CA	24355	CMP404BY
5962-8990403CA	24355	CMP04BY

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices RT 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 1500 Space Park Drive P.O. Box 58020 Santa Clara, CA 95050-8020

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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