

DESCRIPTION:

The DPS256S8N is a Military 256K X 8 high-density, low-power static RAM module comprised of two ceramic 128K X 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

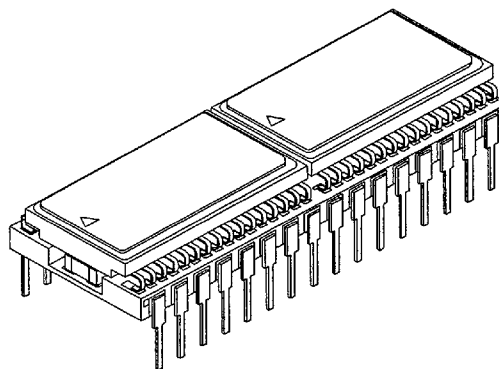
The DPS256S8N is available in a 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The DPS256S8N operates from a single +5V supply and all input and output pins are completely TTL-compatible. The low standby power of the DPS256S8N make it ideal for battery-backed applications.

FEATURES:

- 262,144 by 8 bit configuration
- Access Times: 85*, 100, 120, 150ns
- Faster Speeds Upon Request
- Low Power Dissipation:
40 μ W (typ.) standby
375 mW (typ.) operating
- 2-Volt data retention
- Fully Static Operation - No clock or refresh required
- All inputs and outputs are TTL-compatible
- 600 mil, 32-pin JEDEC standard DIP pinout

* Commercial Only.



PIN NAMES

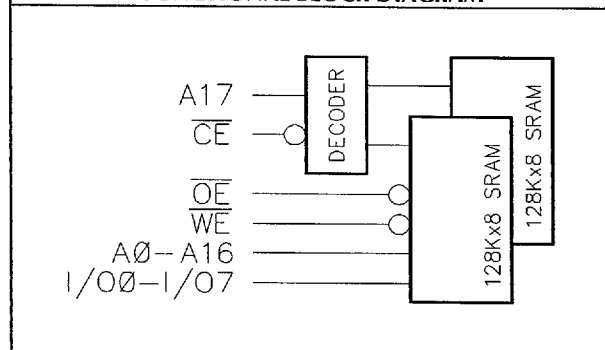
A0 - A18	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VDD	Power (+5V)
VSS	Ground

PIN-OUT DIAGRAM

* 1	32	VDD
A16 2	31	A15
A14 3	30	A17
A12 4	29	$\overline{WE}$
A7 5	28	A13
A6 6	27	A8
A5 7	26	A9
A4 8	25	A11
A3 9	24	$\overline{OE}$
A2 10	23	A10
A1 11	22	$\overline{CE}$
A0 12	21	I/O7
I/O0 13	20	I/O6
I/O1 14	19	I/O5
I/O2 15	18	I/O4
VSS 16	17	I/O3

* This pin must be tied to a Logic LOW for proper operation (see Truth Table).

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V
T _A	Operating Temperature	C	0	+25	+70
		I	-40	+25	+85
		M/B	-55	+25	+125

TRUTH TABLE						
Mode	Pin 1	CE	WE	OE	I/O Pin	Supply Current
Not Selected	X	H	X	X	HIGH-Z	Standby
Not Selected	H	X	X	X	HIGH-Z	Standby
D _{OUT} Disable	L	L	H	H	HIGH-Z	Active
Read	L	L	H	L	D _{OUT}	Active
Write	L	L	L	X	D _{IN}	Active

H = HIGH

L = LOW

X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -1.0mA	2.4	-	V
V _{OL}	LOW Voltage	I _{OL} = 2.1mA		0.4	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Max.	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} + 0.5	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	35	pF	V _{IN} = 0V
C _{CE}	Chip Enable	20		
C _{WE}	Write Enable	30		
C _{OE}	Output Enable	30		
C _{I/O}	Data Input/Output	35		

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	TYP.	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-	-10	+10	-10	+10	-10	+10	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-	-10	+10	-10	+10	-10	+10	μA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	30		50		50		60	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100%, I _{OUT} = 0mA	75		110		110		120	mA
I _{SB1}	Full Standby Supply Current	V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V, CE ≥ V _{DD} -0.2V	8		200		400		1000	μA
I _{SB2}	Standby Current	CE = V _{IH} , V _{IN} = V _{IH} or V _{IN}	3		6		6		6	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA	-		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	-	2.4		2.4		2.4		V

* Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

DATA RETENTION CHARACTERISTICS										
Symbol	Parameter	Test Conditions	Typ. (†)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V _{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DR} - 0.2V$	-	2.0	5.5	2.0	5.5	2.0	5.5	V
I _{CCDR2}	Data Retention Supply Current	V _{DR} = 2.0V	4		90		170		700	μA
I _{CCDR3}	Data Retention Supply Current	V _{DR} = 3.0V	4		100		200		800	μA
t _{CDR}	Chip Disable to Data Retention Time		-	0		0		0		ns
t _R	Recovery Time	t _{RC} = Read Cycle Timing		5		5		5		ms

† Typical measurement made at +25°C, Cycle = min., V_{DD} = 5.0V.

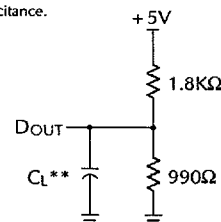
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C _L	Parameters Measured
1	100pF	except t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WHZ} , and t _{WLZ}
2	5pF	t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WHZ} , and t _{WLZ}

Figure 1. Output Load

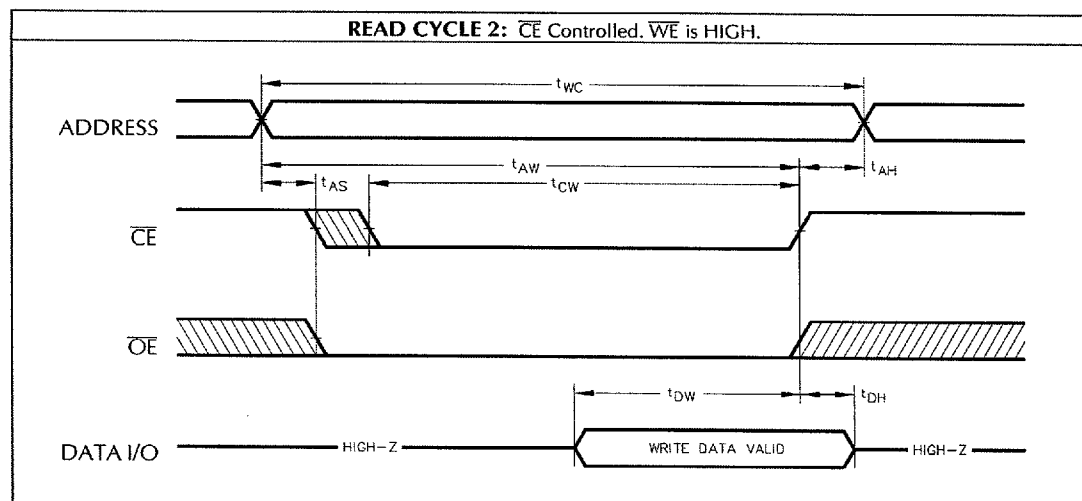
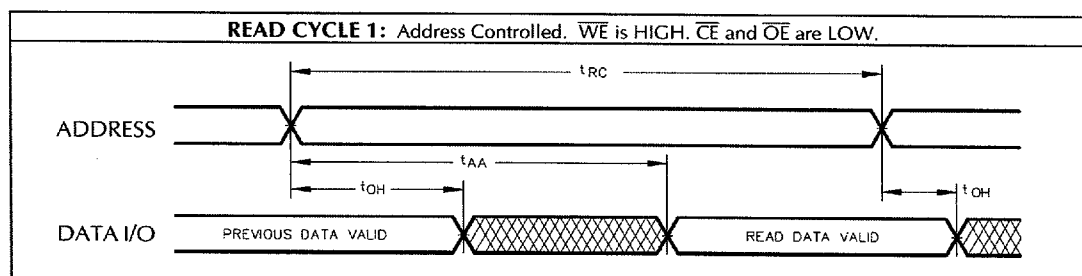
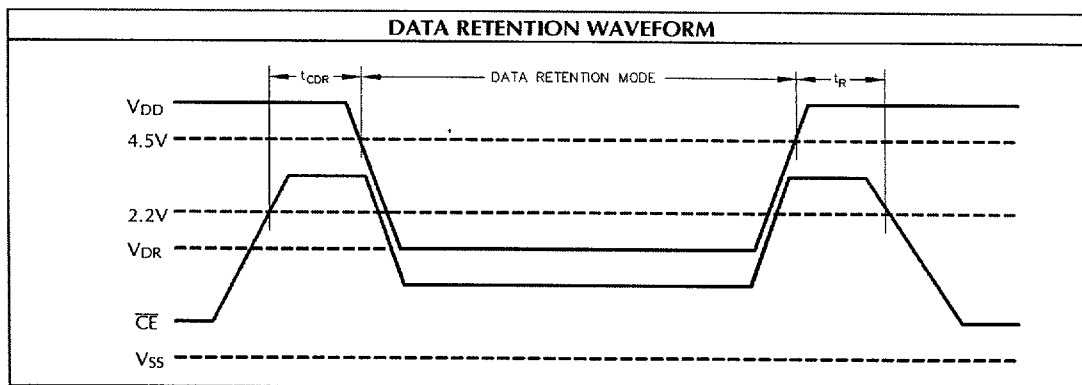
** Including Probe and Jig Capacitance.

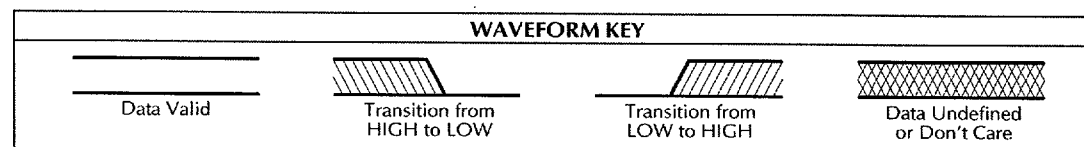
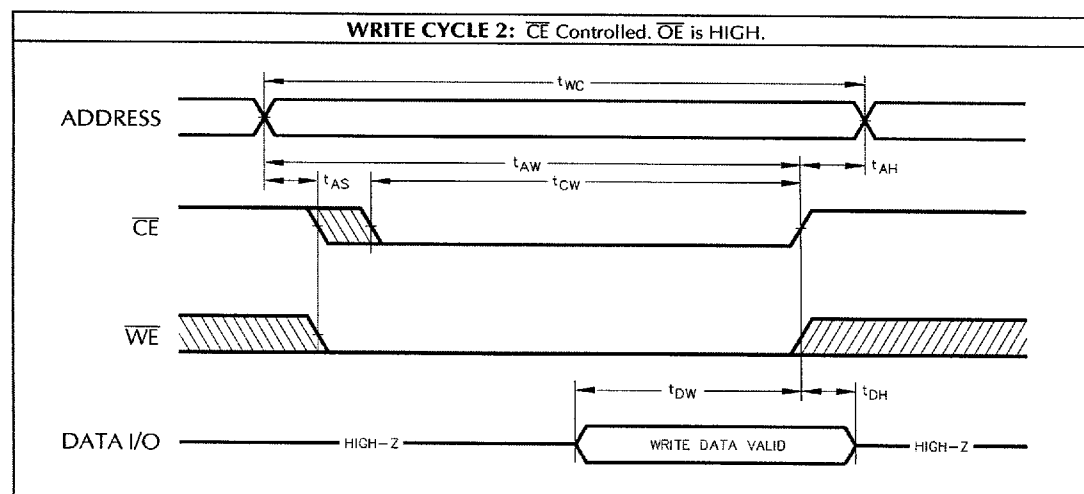
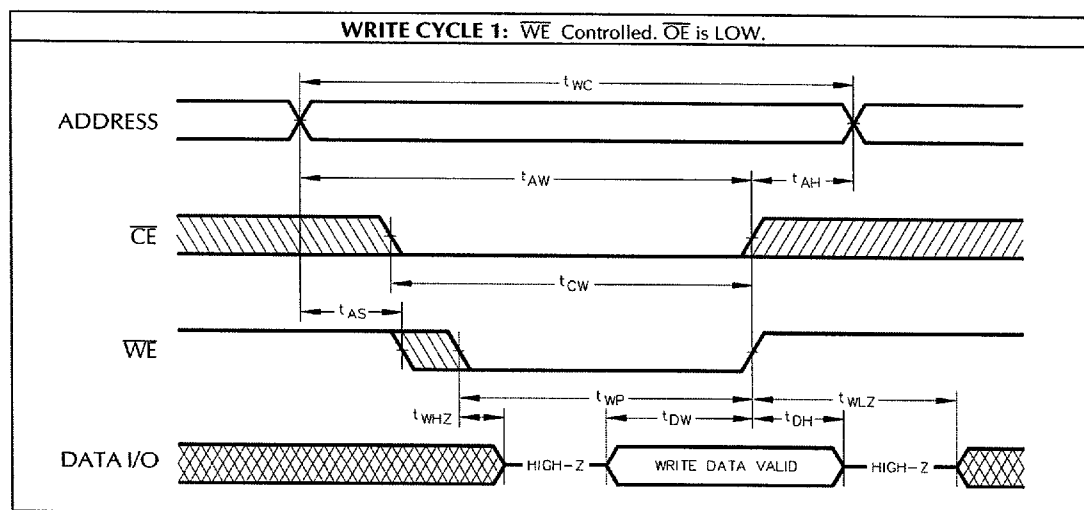


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	85		100		120		150		ns
2	t _{AA}	Address Access Time		85		100		120		150	ns
3	t _{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t _{OV}	Output Enable to Output Valid		40		45		50		60	ns
5	t _{OH}	Output Hold from Address Change	10		10		10		10		ns
6	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	5		5		10		10		ns
7	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 6}	0		0		0		0		ns
8	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		45		45		50		60	ns
9	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 6}		30		30		35		45	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷											
No.	Symbol	Parameter	85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	85		100		120		150		ns
11	t _{AW}	Address Valid to End of Write	80		90		105		115		ns
12	t _{CW}	Chip Enable to End of Write	80		90		105		115		ns
13	t _{DW}	Data to Write Time Overlap	35		35		40		50		ns
14	t _{DH}	Data Hold Time from Write Time	0		0		0		0		ns
15	t _{WP}	Write Pulse Width	55		65		75		85		ns
16	t _{AS}	Address Set-up Time ***	0		0		0		0		ns
17	t _{AH}	Address Hold Time	5		5		5		5		ns
18	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		30		30		35		40	ns
19	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		ns

*** Valid for both Read and Write Cycles.

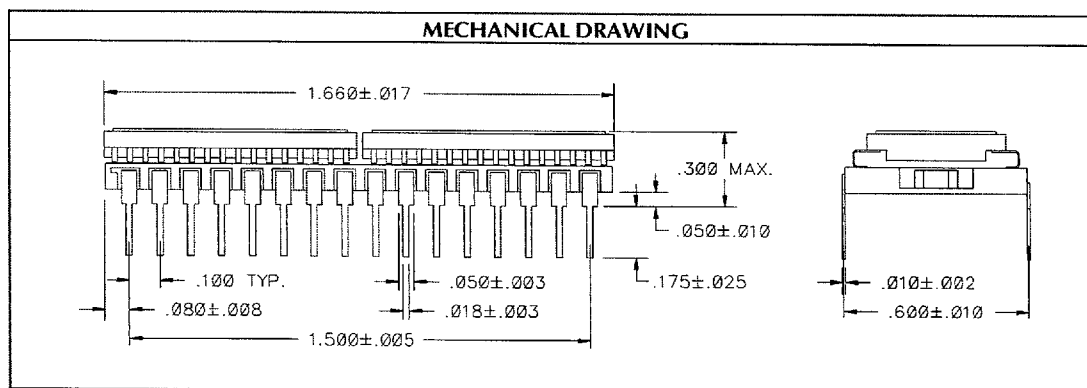




ORDERING INFORMATION						
DP	S	256	S	8	N	-XX X
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	PACKAGE	SPEED GRADE
						C COMMERCIAL 0°-+70°C
						I INDUSTRIAL -40°-+85°C
						M MILITARY -55°-+125°C
						B MIL-PROCESSED -55°-+125°C
						85 85ns (COMMERCIAL ONLY)
						10 100ns
						12 120ns
						15 150ns
						CERAMIC SIDE BRAZED PACKAGE
						MEMORY MODULE WITH SUPPORT LOGIC
						CMOS SRAM

NOTES:

1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500 mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.



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