Am95C71

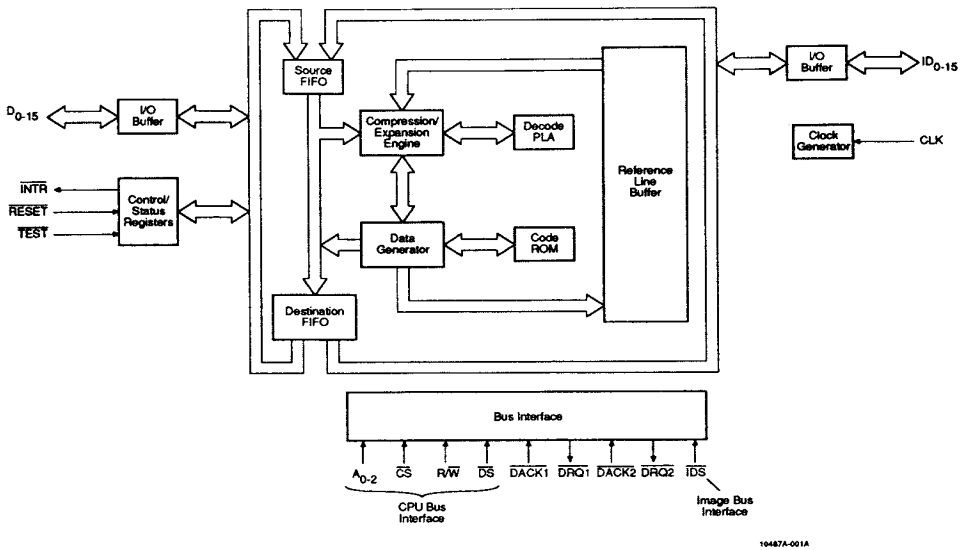
Video Compression/Expansion Processor (VCEP)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Throughput exceeding an average rate of 50 Mb/s when compressing or expanding
- Full CCITT Group 3 and Group 4 compression/expansion: allows MH, MR and MMR coding and transparent mode
- Dual-bus architecture with single-bus mode option
- Supports bit-boundary image width up to 8191 pixels in one-dimensional (1D) mode and 6911 pixels in two-dimensional (2D) mode
- Has on-chip 6911-pixel reference-line buffer allowing high-performance 2D coding
- Provides error detection and recovery capability
- Supports programmable k-Parameter for 2D coding
- 16-word FIFOs on input and output
- Half-duplex operation

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am95C71 Video Compression/Expansion Processor (VCEP) is a high-performance CMOS processor which compresses and expands binary image data using the internationally standardized CCITT Group 3 and Group 4 algorithms.

The VCEP supports the Modified Huffman (MH), Modified Read (MR), and Modified-Modified Read (MMR) coding schemes used by the CCITT Groups 3 and 4 standards. MH coding is a one-dimensional technique which identifies and then codes run-lengths of black or white pixels. MR coding compresses a single scan line using MH coding, followed by k-1 scan lines coded in such a way as to reflect differences from the pixel patterns of the previous scan line (two-dimensional or 2D coding); the value of the k-Parameter is defined by the user and will generally be set to a larger number on communication links with lower bit-error rates.

MMR coding is a full 2D-coding scheme which uses an all-white imaginary reference line when coding the first scan line. All lines on the page are coded two-dimensionally. For a typical binary image, MMR coding offers the best compression, followed by MR and then MH. Compressed data may be corrupted during transmission or storage. Error-free (or error-protected) transmission media are used with Group 4 coding, since error recovery is not possible. The CCITT standard refers to MH and MR coding as Group 3 techniques and MMR coding as a Group 4 technique. Group 3 error recovery facility is provided on the VCEP.

The extent of data compression provided by Group 3 and Group 4 compression techniques depends on the specific data patterns contained in the image. Typically, an originally black-or-white (binary) image will yield compression ratios between 5:1 and 50:1, whereas a binary image produced from a grey-scale or color original may compress poorly, even resulting in a compressed file larger than the raw image. Alternatively, the user may program the VCEP into transparent mode where data is simply passed from source FIFO to destination FIFO without compressing or modifying the data.

When 2D (MR or MMR) coding is performed, the previous scan line is used as a reference to code the current line. To significantly increase performance the VCEP stores the reference line in an on-chip buffer.

The VCEP is a slave-mode device with two 16-bit bus interfaces. The user may select either bus to be source or destination and the VCEP to compress, expand or pass through (transparent mode) data. Data is buffered on input and output by 16-word FIFOs. The VCEP, therefore, may be used as a single-bus or dual-bus device, with FIFO buffers on input and output.

The VCEP may either compress, expand, or pass through data; it cannot do these functions simultaneously or in a multiplexed fashion and is therefore termed a half-duplex device.

However, it is possible for the VCEP to multiplex data compression from several sources if a full scan line is processed from each source, and MH coding is selected. Multiplexed expansion is not supported.

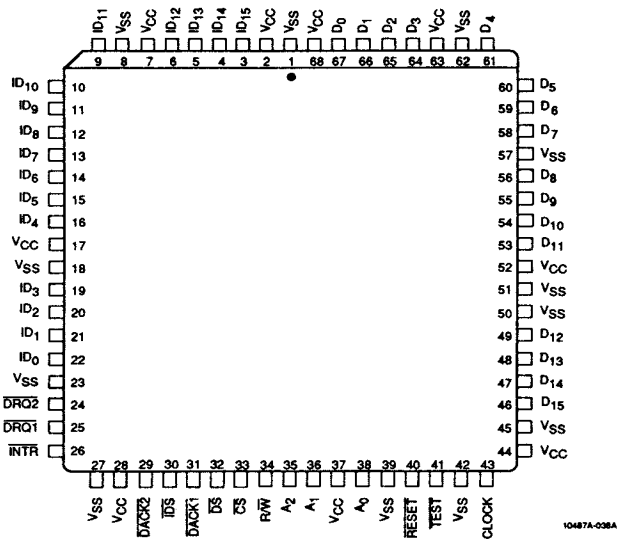
The VCEP has several mechanisms to detect data errors on expansion. For MH and MR modes, if the expanded scan line is longer or shorter than the user-programmed length, the VCEP sets a flag and halts. Illegal codes, negative run lengths in 2D coding, and other illegal fields are detected as errors. Since the VCEP has no on-chip DMA, the host CPU is responsible for error recovery; for example, by replicating the previous scan line when an error is found in the current scan line.

The VCEP has programmable bus burst and dwell counters to allow the user control over the length of the VCEP's data requests and the time between requests.

All registers on the VCEP are set up by the CPU via the VCEP's CPU bus, selecting specific registers with three address lines. In the dual-bus configuration, data is accessed on the Image bus by a slave-mode access which does not require an address.

CONNECTION DIAGRAMS
Top View

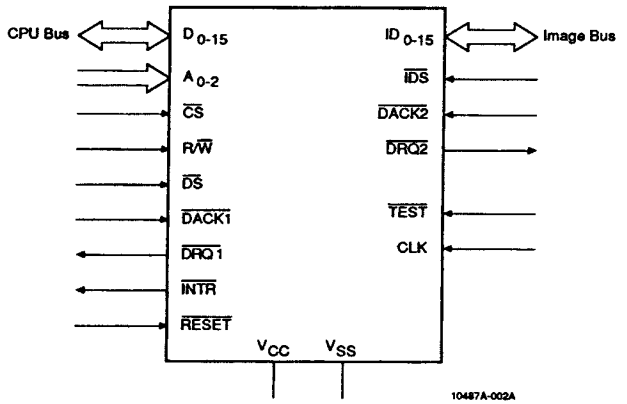
PLCC



CD011640

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS003291

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM95C71 -20 J C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
J = 68-Pin Plastic Leaded Chip Carrier (PL 068)

b. SPEED OPTION
-20 = 20 MHz
-16 = 16 MHz

a. DEVICE NUMBER/DESCRIPTION
Am95C71
Video Compression/Expansion Processor (VCEP)

Valid Combinations	
AM95C71-20	JC
AM95C71-16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A_{0-2} Address Bus (Input)
A 3-bit address used to select one of seven internal registers. These pins are ignored when performing a fly-by transfer on the CPU bus.

CLK Clock (Input)
Master timing of the VCEP is provided by an external source connected to CLK.

$\overline{CS}$ Chip Select (Input; Active LOW)
Qualifies $\overline{DS}$ when performing a flow-through register access via the CPU bus. Chip Select must be inactive when performing a fly-by transfer on the CPU bus.

D_{0-15} CPU Data Bus (Input/Output; Three-state)
A 16-bit bidirectional data bus used to transfer data, commands and status to or from the VCEP.

$\overline{DACK1}$ Data Transfer Acknowledgement 1 (Input; Active LOW)
Controls data transfers to or from the FIFO Data Port.

$\overline{DACK2}$ Data Transfer Acknowledgement 2 (Input; Active LOW)
Controls data transfers to or from the FIFO Data Port.

$\overline{DRQ1}$ Data Transfer Request 1 (Output; Active LOW)
Controls data transfers to or from the FIFO Data Port.

$\overline{DRQ2}$ Data Transfer Request 2 (Output; Active LOW)
Controls data transfers to or from the FIFO Data Port.

$\overline{DS}$ Data Strobe (Input; Active LOW)
Controls data transfers on the CPU data bus.

ID_{0-15} Image Data Bus (Input/Output; Three-state)
A 16-bit bidirectional data bus used to transfer data to or from the VCEP.

$\overline{IDS}$ Image Data Strobe (Input; Active LOW)
Controls data transfers on the Image Data Bus.

$\overline{INTR}$ Interrupt Request (Output; Active LOW)
$\overline{INTR}$ is asserted when an exception or termination condition occurs and the user has previously set the Interrupt Enable bit in the Command/Status Register. $\overline{INTR}$ is made inactive when the Command/Status Register is read or when the VCEP is reset.

R/$\overline{W}$ Read/Write (Input)
Controls the direction of transfer on the CPU bus when accessing one of the internal registers. This signal is ignored when performing a fly-by transfer on the CPU bus.

$\overline{RESET}$ Reset (Input; Active LOW)
$\overline{RESET}$ is an asynchronous, active-LOW input which initializes VCEP to an idle state. $\overline{RESET}$ must be driven LOW for at least four clock cycles to ensure proper operation.

$\overline{TEST}$ Test (Input; Active LOW)
When $\overline{TEST}$ is held LOW, all VCEP outputs are three-stated. In normal use this pin should be tied to V_{CC} or held at a TTL-HIGH level.

FUNCTIONAL DESCRIPTION

Register Description

The VCEP has seven user registers: the FIFO Data Port, Command/Status Register, Parameter Register, Burst Count Register, Dwell/Offset Register, Line Length Register and Line Count Register. These registers are shown in Figure 1-1.

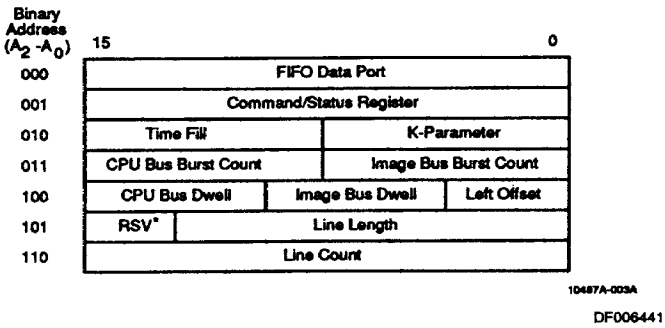


Figure 1-1. VCEP Register Set

OVERVIEW OF REGISTERS

The Command/Status Register (CSR) contains 11 Command bits and 4 Status bits (see Figure 1-2).

GO: The GO bit is used to start VCEP operation in the mode indicated by the OM field compression, expansion or transparent.

Operational Mode (OM): The OM field defines whether VCEP should be in compress or expand (MH, MR or MMR), transparent or reset mode.

Line Mode (LM): When LM = 0 the VCEP will process one scan line before stopping. When LM = 1 the VCEP processes a full image before stopping.

Boundary Mode (BM): This bit defines whether the first code data word of a page is on a word boundary, BM = 0, or on an odd-byte boundary, BM = 1.

Interrupt Enable (IE): When IE = 1, the $\overline{INTR}$ output is asserted whenever the VCEP encounters an exception or termination condition.

Compressor Word-boundary Control (CW): In MH or MR mode, if CW = 1 the VCEP pads the end of the code line to ensure it ends on a word boundary. In MMR mode this bit is ignored.

Source Control (SC): If SC = 0, the CPU bus is selected as the data source. If SC = 1, the Image bus is selected as data source.

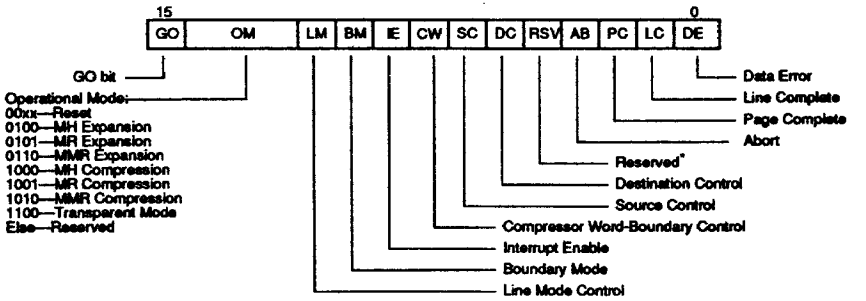


Figure 1-2. Command/Status Register

Destination Control (DC): If DC = 0, the CPU bus is selected as the data destination. IF DC = 1, the Image bus is selected as data destination.

The remaining bits indicate status information:

Abort (AB): If the Command/Status Register is written while the VCEP is busy, the VCEP stops processing and sets AB = 1.

Page Complete (PC): When the VCEP detects the RTC/EOP code in expansion mode it sets this bit. In compression or transparent mode this bit is set when the Line Count Register has been decremented to zero.

Line Complete (LC): When the VCEP is in single-line mode it sets the Line Complete bit each time VCEP has processed a line of data. This bit may also be set when a data error occurs.

Data Error (DE): When the VCEP detects a data error on expansion this bit is set.

The Parameter Register contains an 8-bit Time-Fill value and an 8-bit k-Parameter. Time-Fill is used in MH and MR Compression modes and its value specifies the minimum length of a coded line in words, which may vary from 0 to 255 words. The k-Parameter specifies for MR compression mode how many lines (k-1) will be compressed using two-dimensional coding after a one-dimensionally coded reference line. "k" may vary from 1 to 255 and infinity, indicated by k = 0.

The Burst Count Register contains an 8-bit CPU bus burst count and an 8-bit Image bus burst count.

The Dwell/Offset Register contains a 6-bit CPU bus dwell count, a 6-bit Image bus dwell count, and a 4-bit Left Offset Register (LOR).

The Line Length Register (LLR) specifies the number of pixel elements contained in one line. For one-dimensional coding the total of LLR + LOR must not exceed 8191 pixels. For two-dimensional coding LLR + LOR must not exceed 6911 pixels, due to the internal reference line buffer size. The minimum value of LLR + LOR in either case is 17 pixels.

The Line Count Register (LCR) should be set to the number of scan lines of an image when data compression is used and will be decremented each time the VCEP processes one line in compression or transparent mode. The LCR value is incremented each time the VCEP expands a line. The user may read this value from the LCR Register at any time, while the last value written to the LCR Register is stored elsewhere internally and will be reloaded at the start of a new page.

The FIFO Data Port is a 16-bit I/O port through which image and compressed data is accessed.

All Reserved bits ahould be set to "0" by the user.

Operational Overview

The VCEP has two 16-bit data buses. The control signals associated with each bus depend on whether the VCEP is programmed for single-or dual-bus operation and the type of transfer performed. The CPU bus supports two methods of transferring data into or out of the VCEP. Flow-through operations on the CPU bus use $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$, and A_{0-2} to determine whether a read or write is to be performed o n one of seven internal registers. Fly-by operations on the CPU bus use $\overline{DS}$ and $\overline{DACK1}$ or $\overline{DACK2}$, depending on bus configuration selected, to perform a transfer to or from the FIFO Data Port. The Image bus supports only fly-by operations to or from the FIFO Data Port and uses $\overline{IDS}$ and $\overline{DACK1}$ or $\overline{DACK2}$, depending on bus configuration selected, to perform a transfer.

The VCEP requires data to be both written to and read from the FIFO Data Port. The SC field in the Command/Status Register (CSR) is used to select whether the CPU or Image bus will be used for supplying data to the source buffer via the FIFO Data Port. The DC field of the CSR selects whether the CPU or Image bus will be used for reading data from the destination buffer via the FIFO Data Port. The SC and DC fields are independent and may be programmed to any of four possible configurations. Of these possibilities, two assign a single bus for reading and writing source and destination buffers. The remaining two possibilities have source and destination assigned to different buses.

Table 1 defines the settings of SC and DC, together with use of $\overline{DRQ1}$, $\overline{DACK1}$, $\overline{DRQ2}$ and $\overline{DACK2}$. The data acknowledge signals associated with the CPU bus, $\overline{DACK1}$ and/or $\overline{DACK2}$, are used in fly-by operations only and must both be inactive whenever $\overline{CS}$ is active.

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TABLE 1. VCEP BUS ASSIGNMENT

SC	DC	Source Bus	Input Pins	Control Pins	Destination Bus	Output Pins	Control Pins
0	0	CPU	D_{0-15}	$\overline{DRQ1}/\overline{DACK1}$	CPU	D_{0-15}	$\overline{DRQ2}/\overline{DACK2}$
0	1	CPU	D_{0-15}	$\overline{DRQ1}/\overline{DACK1}$	Image	ID_{0-15}	$\overline{DRQ2}/\overline{DACK2}$
1	0	Image	ID_{0-15}	$\overline{DRQ2}/\overline{DACK2}$	CPU	D_{0-15}	$\overline{DRQ1}/\overline{DACK1}$
1	1	Image	ID_{0-15}	$\overline{DRQ1}/\overline{DACK1}$	Image	ID_{0-15}	$\overline{DRQ2}/\overline{DACK2}$

Detailed Functional Description

The VCEP is a streamlined, high-speed compression/expansion engine. The inclusion on-chip of a 6911-pixel reference line buffer allows very efficient two-dimensional coding while a minimal set of user registers combines ease of programming with operational flexibility. By using FIFOs at input and output the VCEP presents a simple, buffered slave-mode interface to CPU and Image buses.

The VCEP may be clocked asynchronously from the system CPU. In addition, the CPU and VCEP clock rates may differ significantly within the following limitations.

When the VCEP clock is slower than the CPU clock, a lower limit is reached if more than one complete data transfer cycle occurs in each VCEP clock cycle. One data transfer may occur on each bus of a dual-bus system since the buses are fully independent.

When the VCEP clock is faster than the CPU clock, the upper limit is defined by the maximum low pulse width of $\overline{DS}$, which is 15 VCEP clock cycles.

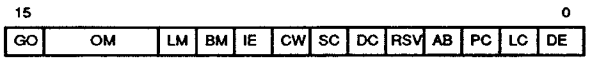
To start VCEP operation after a hardware Reset, the CPU must initialize VCEP registers, specify Operational Mode (OM), select source and destination buses, and choose whether to process single scan lines or full pages. Other parameters may need to be selected depending on choice of operational

mode. Additionally, a software Reset should be asserted prior to processing each page.

The typical pattern of operations after a hardware Reset would be: wait at least eight clock cycles after asserting reset; set up parameters and select mode; assert GO = 1; wait until line processing (if LM = 1) or page processing terminates and LC = 1 or PC = 1; read Status bits; select Reset mode; wait at least eight clock cycles; change parameters if needed and repeat.

COMMAND/STATUS REGISTER (CSR) ADDRESS = 001

The CSR contains 11 Command bits and 4 Status bits, described below. Note that after writing a register, the system should wait a minimum of eight clocks before accessing that register again.



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DF006460

Figure 2. Command/Status Register

Bit 15 — GO: The GO bit is used to start VCEP operation in the mode indicated by the OM field. The user must set up all parameters and operational mode before setting GO = 1. If GO is set and the VCEP is not busy, the VCEP will clear Status bits and start the selected operation. When the operation is complete, the VCEP resets GO and halts. If the user attempts to write the CSR while GO is set and the VCEP is busy, the VCEP will halt the current operation and interrupt the CPU if the Interrupt Enable (IE) bit is set. This condition requires the user to provide the VCEP with a software reset.

When GO = 0, the VCEP is idle and the user may access all registers except the FIFO Data Port, which may yield unpredictable results and if accessed, requires the CPU to reset the VCEP. If the user has programmed the VCEP to compress, expand or pass-through (transparent mode) a complete page of data, Status bits are set and GO is reset when the page has been processed and all data read from the destination buffer by the user, or when an error condition is detected. In single-line mode (LM = 0) Status bits are set and GO is reset when the VCEP has processed a single line of data and the user has emptied the destination buffer. The system may begin processing in single-line mode and then switch to multi-line mode at the end of any scan line.

The user should never assert the GO bit when selecting a software Reset.

When the VCEP finishes an operation and resets GO it will also generate an interrupt if IE = 1.

GO = 0 after a hardware or software Reset.

Bits 14 – 11 — Operational Mode (OM): The OM field defines whether VCEP should compress, expand, pass-through data (transparent mode) or do a software Reset. When compression or expansion is selected, the OM field also defines whether MH, MR or MMR coding is to be used. Table 2 defines the OM bits.

TABLE 2. OPERATIONAL MODE BIT DEFINITIONS

Bit 14	Bit 13	Bit 12	Bit 11	Operational Mode
0	0	0	0	Software Reset
0	0	0	1	Software Reset
0	0	1	0	Software Reset
0	0	1	1	Software Reset
0	1	0	0	MH Expansion
0	1	0	1	MR Expansion
0	1	1	0	MMR Expansion
0	1	1	1	Reserved
1	0	0	0	MH Compression
1	0	0	1	MR Compression
1	0	1	0	MMR Compression
1	0	1	1	Reserved
1	1	0	0	Transparent Mode
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Each Operational Mode is explained in considerable detail in the section on Operating Modes.

Bit 10 — Line Mode (LM): When LM = 0 the VCEP is in single-line mode and when set to LM = 1 the VCEP is in multi-line mode. In single-line mode, when the user selects an operational mode besides Reset, the VCEP will process a single line, waiting until the destination buffer has been emptied, before it clears GO, sets Line Complete (LC = 1), and halts. When in multi-line mode and when compressing or in transparent mode, the VCEP will process data until the Line Count Register is zero. When it detects LCR = 0 it waits until all data has been read from the destination buffer, clears GO, sets Page Complete (PC = 1), and halts.

Bit 9 — Boundary Mode (BM): This bit defines whether the first code data word of a page is on a word boundary, BM = 0, or on an odd-byte boundary, BM = 1. When BM = 1 and VCEP is compressing, it inserts eight zeros before the code data so that the code begins the page on an odd-byte boundary. If BM = 0 no zeros are inserted. When BM = 1 and VCEP is expanding, it ignores the first eight bits of the first code word of the page and begins expanding from the second code byte of the page (bit 8). When BM = 0 and the VCEP is expanding, it begins from bit 0 of the first code word.

Bit 8 — Interrupt Enable (IE): When IE = 1, the $\overline{INTR}$ output is asserted whenever VCEP encounters an exception or termination condition. When IE = 0, $\overline{INTR}$ is never asserted.

Bit 7 — Compressor Word-boundary Control (CW): In MH or MR Compression mode, if CW = 1 the VCEP will insert 0 to 15 pad bits (zeros) at the end of each line of code data to ensure that the line ends on a word boundary. In MMR Compression mode this bit is ignored.

Bit 6 — Source Control (SC): If SC = 0, the CPU bus is selected as the data source. If SC = 1, the Image bus is selected as data source.

Bit 5 — Destination Control (DC): If DC = 0, the CPU bus is selected as the data destination. IF DC = 1, the Image bus is selected as data destination.

Bit 4: Reserved.

The remaining bits indicate status information. Status bits are reset when GO = 1 or when the system performs a software Reset of the VCEP.

Bit 3 — Abort (AB): If the Command/Status Register is written while the VCEP is busy, the VCEP will abort processing and set this bit. To restart the VCEP, the user must perform a software or hardware Reset and wait at least eight clocks before setting an active operational mode and writing GO = 1. If an Abort occurs, this is a non-recoverable condition and all data currently in process will be lost.

Bit 2 — Page Complete (PC): When VCEP detects the RTC/EOP code in expansion mode it sets this bit. In compression or transparent mode this bit is set when the Line Count Register has been decremented to zero. Either way this Status bit indicates that the VCEP has processed a page of data.

Bit 1 — Line Complete (LC): When the Line Mode bit is reset (LM = 0) the VCEP is in single-line mode and the Line Complete bit is set when the VCEP has processed a line of data.

Bit 0 — Data Error (DE): When VCEP detects a data error during expansion, this bit is set. Data error conditions are described in the section on Error Detection and Recovery.

A summary of status information is given in Table 3.

TABLE 3. SUMMARY OF STATUS INFORMATION

AB	PC	LC	DE	Explanation
1	X	X	X	VCEP Aborted the Current Operation
0	1	0	0	Page Complete without Error in Multi-line Mode
0	0	1	0	Line Complete without Error in Single-line Mode
0	0	0	1	Data Error (see above)
0	0	1	1	Data Error Detected in EOL Code
0	1	0	1	RTC/EOP Detected with Data Error

OPERATING MODES

The system must specify LLR, LCR, LOR, Time-Fill, and k-Parameter before setting the GO bit in any mode, except where specified.

Compression

When compressing data, the VCEP reads image data from the source buffer, converts it to code, and writes it to the destination buffer.

If BM = 1 in the CSR, the VCEP puts the first EOL code on an odd-byte boundary by inserting eight zeros into the first word. If CW = 1, the VCEP compresses each scan line and adds from one to fifteen zeros to ensure each line ends on a word boundary. The VCEP also inserts bits before the next line's EOL code if the current line is shorter than the minimum length specified by the Time-Fill Parameter Register.

The user specifies scan line length in the Line Length Register (LLR) and as the VCEP reads image data from the source buffer, it will ignore the first LOR bits of each scan line, where the user defines LOR, the Left Offset Register, which may vary from 0 to 15 bits. The user must also program the VCEP's Line Count Register (LCR), specifying the number of scan lines in a page. Once the VCEP has compressed LCR scan lines this is the end of a page.

In all compression modes once the VCEP has finished compressing a page it will wait until the destination FIFO has been emptied before it sets PC = 1 in the CSR and halts. In addition, if LM = 0 in the CSR (single-line mode), the VCEP waits until its destination FIFO is emptied after compressing each scan line, sets LC = 1, and halts. If LM = 0 and the code data does not end on a word boundary, the VCEP retains the last partial word if no padding or Time-Fill bits are added.

MH Compression

When the CPU sets OM = 1000, the VCEP is in MH Compression mode, where each scan line is 1D-compressed and prefixed with an EOL (End-of-Line) code; the k-Parameter is ignored. Once it has compressed a scan line and added pad bits as needed, it decrements the Line Count Register. When this count reaches zero, the VCEP adds six EOL codes, indicating the RTC (Return-to-Control) code to indicate end-of-page. MH Compression mode data format is shown in the Data Formats section.

MR Compression

When OM = 1001 in the CSR, the VCEP is in MR Compression mode, where it 1D-compresses the first scan line and 2D-compresses the following (k-1) lines. The code for each scan line is preceded by an EOL code with Tag bit. Tag = 1 for 1D-compressed lines; Tag = 0 for 2D-compressed lines. If k = 0, all but the first scan line are 2D-compressed. The value of k is stored internally and so does not need to be loaded each time the user sets GO = 1, although k may be changed while compressing a page in single-line mode.

When beginning page compression, the VCEP outputs an EOL code with Tag bit set, followed by the 1D code for the first scan line. The VCEP then decrements the Line Count Register and adds the RTC code (six EOL codes with Tag = 1) if the count is zero, to indicate end-of-page. MR compression mode data format is shown in the section on Data Formats.

Using the k-Parameter: The k-Parameter specifies how many lines (k-1) will be compressed using two-dimensional coding after a one-dimensionally coded reference line. "k" may vary from 1 to 255 and infinity. This register is valid only in MR Compression mode and is ignored in all other modes. The most-significant bit of the k-Parameter is bit 7. To set k at infinity, write k = 0. When k = 0, the first scan line of a page is 1D-coded and all remaining scan lines are 2D-coded.

When LM = 0, and single-line mode is used with MR Compression, the user may change the value of k while compressing a document. The effect of k-Parameter on whether a line is 1D- or 2D-coded is shown in Figure 3.

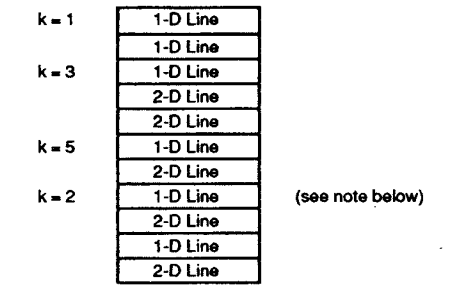

Figure 3. Effect of k-Parameter on Coding

MMR Compression

When OM = 1010 in the CSR, the VCEP is in MMR Compression mode and will 2D-compress all scan lines. The k-Parameter and Time-Fill parameter are ignored.

When the VCEP begins page compression it 2D-compresses the first scan line with respect to an imaginary white reference line (all zeros). For subsequent lines, the VCEP uses as reference the data in its internal line buffer. At the beginning of page, VCEP will pad the first code with eight zeros if BM = 1. In MMR Compression mode, no EOL code precedes each coded line.

Once the VCEP has compressed a scan line, it decrements the Line Count Register. When this count reaches zero, the VCEP adds two EOL codes, indicating the EOP (End-of-Page) code. MMR Compression mode data format is shown in the section on Data Formats.

Expansion

In all expansion modes, the VCEP reads code data that the user has written to the source buffer, expands it, and places it in the destination buffer. The k-Parameter and Time-Fill parameter are ignored.

Prior to beginning page expansion, the user defines scan line length in the Line Length Register (LLR), and as the VCEP expands code data and writes it to the destination buffer, it compares current line length to LLR, allowing error detection. The VCEP will also write the first expanded word of each scan line offset by LOR bits, where the user defines LOR (Left Offset Register), which may vary from 0 to 15 bits. The VCEP increments the Line Count Register (LCR) after expanding a scan line. At the end of the page, the user may read LCR to determine the number of scan lines in a page. When the user sets GO = 1 to begin processing an image, LCR is loaded with the last count programmed (since this is retained internally between pages). The VCEP then begins expanding a new page. If BM = 0 the VCEP will search from bit 0 of the first code word; if BM = 1, the VCEP searches from bit 8.

MH Expansion

When OM = 0100 in the CSR, the VCEP is in MH Expansion mode, where it 1D-expands all code data.

MR Expansion

When OM = 0101 in the CSR, VCEP is in MR Expansion mode, where it 1D- or 2D-expands code data, depending on the detected value of the Tag bit following EOL codes. If Tag = 1, data is 1D-expanded, while Tag = 0 will cause 2D expansion.

MMR Expansion

When OM = 0110, the VCEP is in MMR Expansion mode, where it will 2D-expand all code data.

Transparent Mode

When OM = 1100, the VCEP is in Transparent mode, where it transfers data from source to destination buffers without modification. Transparent mode is a simple mechanism to allow data flow between CPU and Image buses. The Time-Fill and k-Parameters are ignored and LOR should be set to zero. The VCEP still uses LLR and LCR values. When the VCEP

reaches the end of the page (LCR = 0), it waits until the destination buffer has been emptied, sets PC = 1 in the Status Register, and halts. In single-line mode (where LM = 0), when the VCEP detects the end of the scan line (LLR reaches the programmed value), it waits until the destination buffer has been emptied, sets LC = 1, and halts.

Reset

When OM = 00xx, the VCEP is reset. This software Reset has the same effect on the VCEP as a hardware Reset, clearing source and destination buffers, all Status bits, and the GO bit. Other register contents are unchanged. The GO bit should not be set when performing a software Reset. Once the user has performed a software Reset, the CSR should not be accessed for at least eight clock (CLK) cycles.

DATA FORMATS

Image Data Format

The VCEP processes (compresses or expands) images digitized as described below:

1. A single image is represented by an array of black and white pixels.
2. Each row of pixels is represented by ones and zeros:
   White pixel = 0
   Black pixel = 1
3. The image bit stream is assumed to be generated by a scanner which moves from left to right across the page while scanning each line.
4. Bit 0 of each word of the resulting bit stream is considered to be the least-significant bit.
5. Bit 0 of a code word is the least-significant bit.

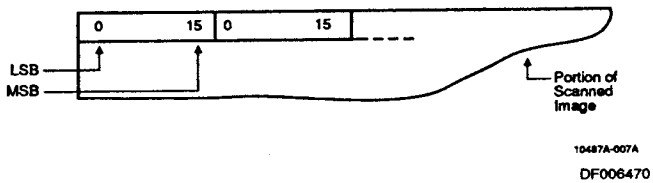

Figure 4. Scanned Data Stream to/from VCEP

Compressed Data Format

The compressed data formats for MH, MR and MMR modes are shown below.

MH Code Compressed Data Format without Time-Fill Bits

If BM = 1 in the CSR, the prefixed EOL starts from bit 8 of the first word, which is the odd-byte boundary (Figure 6).

If CW = 1 in the CSR, the VCEP's compressor adds pad bits (0 to 15 zeros) to the end of the coded line, to make the coded line end on a word boundary (Figure 7).

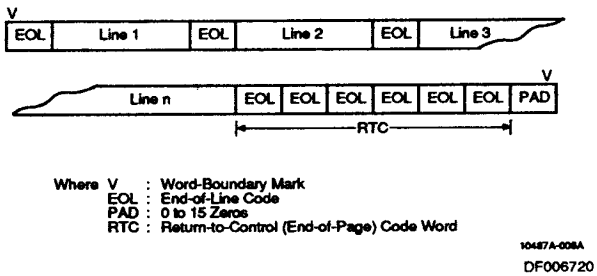

Figure 5. MH Coded Data without Time-Fill

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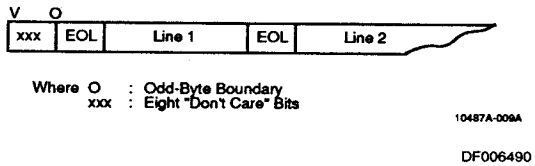

Figure 6. MH Coded Data with BM = 1

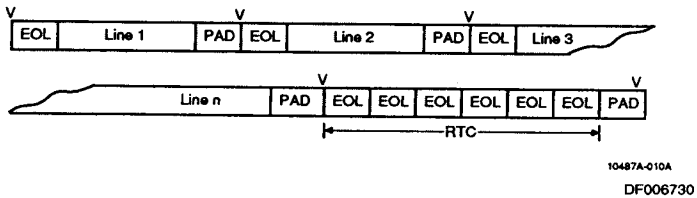

Figure 7. Padded MH Coded Data

MH Mode Compressed Data Format with Time-Fill Bits

If BM = 1 in the CSR, the prefixed EOL of the first line starts from bit 8 of the first word, on the odd-byte boundary (Figure 9).

If CW = 1 in the CSR, the VCEP's compressor will insert pad bits (0 to 15 zeros) to the last code of the line, such that the coded line ends on a word boundary. Since the Time-Fill bits will always end on a word boundary, no pad bits will be added when Time-Fill occurs (Figure 10).

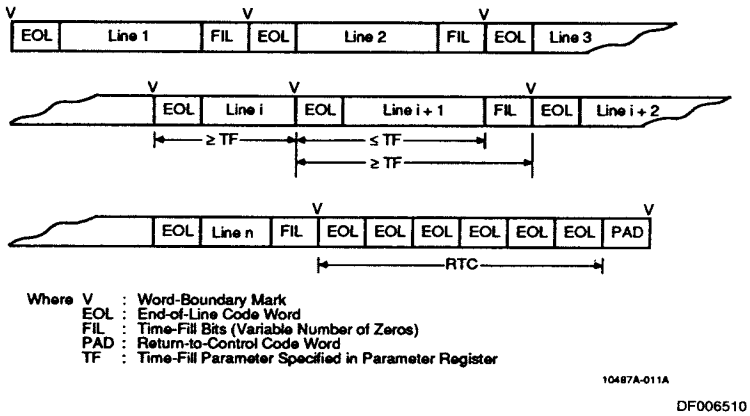

Figure 8. MH Coded Data with Time-Fill

Where O : Odd-Byte Boundary
xxx : Eight "Don't Care" Bits

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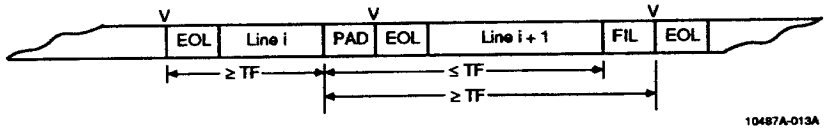
Figure 9. MH Coded Data with Time-Fill and BM = 1



10487A-013A

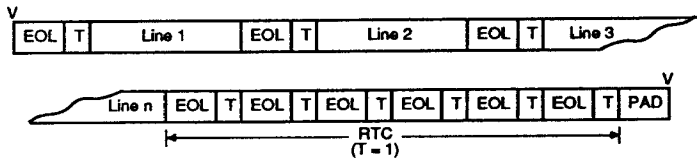
DF006530

Figure 10. Padded MH Coded Data with Time-Fill

MR Mode Compressed Data Format without Time-Fill Bits

If BM = 1 in the CSR, the prefixed EOL of the first coded line will be at the odd-byte boundary of the first word (Figure 12).

If CW = 1 in the CSR, the VCEP's compressor will insert pad bits (0 to 15 zeros) at the end of the coded line to ensure it ends on a word boundary (Figure 13).



Where V : Word-Boundary Mark
EOL : End-of-Line Code
T : Tag Bit
PAD : 0 to 15 Zeros
RTC : Return-to-Control Code Word

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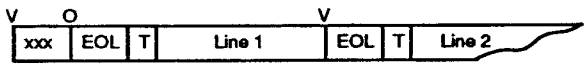
DF006540

Figure 11. MR Coded Data without Time-Fill



Where O : Odd-Byte Boundary
xxx : Eight "Don't Care" Bits

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DF006550

Figure 12. MR Coded Data with BM = 1

5

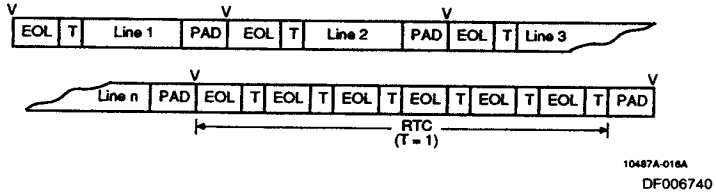
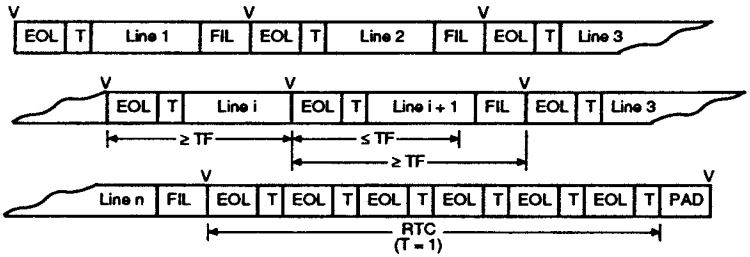


Figure 13. Padded MR Coded Data without Time-Fill

MR Mode Compressed Data Format with Time-Fill Bits

If BM = 1 in the CSR, the prefixed EOL of the first coded line will begin on an odd-byte boundary (Figure 15).

If CW = 1 in the CSR, the VCEP's compressor inserts pad bits (0 to 15 zeros) to the end of the coded scan line, such that it ends on a word boundary. Since Time-Fill bits will always end on a word boundary, no pad bits are necessary when Time-Fill occurs (Figure 16).



Where V : Word-Boundary Mark
EOL : End-of-Line Code
FIL : Time-Fill Bits (Variable Number of Zeros)
T : Tag Bit
PAD : 0 to 15 Zeros
RTC : Return-to-Control Code Word
TF : Time-Fill Value

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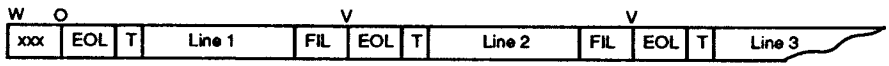
Figure 14. MR Coded Data with Time-Fill



Where O : Odd-Byte Boundary
xxx : Eight "Don't Care" Bits

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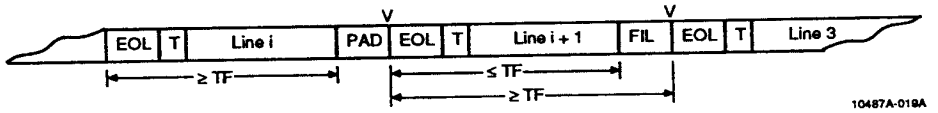
Figure 15. MR Coded Data with Time-Fill and BM = 1

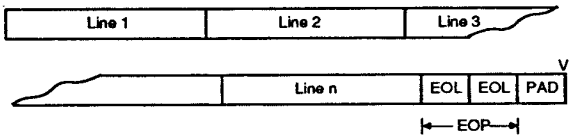


DF006590

Figure 16. Padded MR Coded Data with Time-Fill

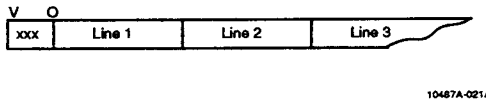
MMR Mode Compressed Data Format

If BM = 1 in the CSR, the first code word of the first scan line will begin on an odd-byte boundary (Figure 18).



DF006600

Figure 17. MMR Coded Data



DF006750

Figure 18. MMR Coded Data with BM = 1

5

End-of-Line and End-of-Page Codes

Note: Serial data streams are shown here from least- to most-significant bits in all cases.

When Modified Huffman (MH) coding is expanded, the VCEP recognizes the end of a page (known as Return-to-Control or RTC), when it detects three consecutive EOL code words:

(MH code RTC) = 0000 0000 0001
0000 0000 0001
0000 0000 0001

When the VCEP is in MH Compression mode it will append six EOL codes to the end of each page.

When Modified Read (MR) coding is expanded, the VCEP recognizes the end of a page (RTC) when it detects three EOL codes, as in MH coding, but each EOL code has a single Tag bit (set to one) added:

(MR code RTC) = 0000 0000 0001 1
0000 0000 0001 1
0000 0000 0001 1

When the VCEP is in MR Compression mode it will append six EOL codes with Tag bits set, to the end of each page.

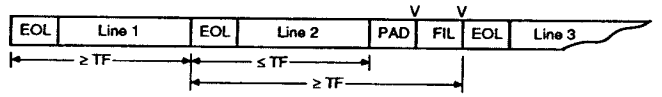
When MMR coding is used, the end of a page (now called EOP) is indicated by two EOL code words:

(MMR code EOP) = 0000 0000 0001
0000 0000 0001

When the VCEP is in MMR Compression mode it will append two EOL codes to the end of each page.

Time-Fill Parameter

Parameter Register (PMR), Bits 15 – 8 Time-Fill (TF): This value specifies the minimum length of a coded line in words, which may vary from 0 to 255 words or from 0 to 4080 bits. VCEP will pad all coded lines less than the value specified here by inserting zeros after the end of the coded data and before the EOL code, with the Time-Fill bits always ending on a word boundary. Time-Fill is performed only when MH and MR coding are used. Minimum line length is calculated as the sum of lengths of the coded scan line, pad bits (to ensure the last code word ends on a word boundary) and the EOL code. An example of Time-Fill in the coded data stream is given in Figure 19.



Where V : Word-Boundary Mark
EOL : End-of-Line Code
FIL : Time-Fill Bits
PAD : 0 to 15 Zeros
TF : Time-Fill Value

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Figure 19. Example of Time-Fill

The Time-Fill parameter may specify a minimum line length of 0 to 255 words, where bit 15 in the Parameter Register is the most-significant bit and bit 8 is the least-significant bit.

ERROR DETECTION AND RECOVERY

Detected error conditions are as follows. In MH/MR Expansion modes:

1. The expanded scan line length is longer than the Line Length Register before EOL is detected.
2. The expanded scan line length is shorter than the Line Length Register when the EOL is detected.
3. The expanded scan line length is shorter than the Line Length Register when the RTC/EOP is detected.
4. The codes indicate at any time that a negative run length has occurred.
5. An illegal code word is detected. These codes are:

   0000 0000 1,
   0000 0000 01,
   and 0000 0000 001.

   Also, if an error occurs in the last code word in a line such that it ends in one or more zeros, this may cause false EOL recognition and status will be LC = 1 and DE = 1.
6. In 2D-coding, the following illegal codes are detected:

   0000 001,
   and 0000 0001.
7. Two consecutive EOL codes are detected followed by a non-EOL code word. In the event of this error LC is also set.

In MMR Expansion mode:

1. The expanded scan line length is longer than the Line Length Register.
2. The codes indicate at any time that the run length is negative.
3. An illegal code word is detected. These codes are:

   0000 001,
   0000 0001,
   0000 0000 1,
   0000 0000 01,
   and 0000 0000 001.
4. An EOL code is detected except as part of a pair indicating EOP.
5. Fill bits are present in the code data.
6. The expanded scan line length is shorter than the Line Length Register when an EOP code is detected.

If an error is detected within a line and the Interrupt Enable bit is set (IE = 1 in CSR), the system will be interrupted; otherwise the system must poll the Status bits in the CSR. Either way, Table 4 shows the possible status code combinations when an error is detected.

TABLE 4. ERROR STATUS CODES

AB	PC	LC	DE	Explanation
0	0	0	1	Data Error
0	0	1	1	Data Error Detected in EOL Code
0	1	0	1	RTC/EOP Detected with Data Error

The DE bit is reset after the user issues a command with GO = 1, or when the user issues a software Reset.

When the VCEP detects an error, it stops expanding data, waits until the destination buffer has been emptied, and then sets Status bits and goes idle. When the user executes the error recovery routine for MH or MR modes, the VCEP could be programmed to be in single-line mode to facilitate the user's administration of error recovery. Once the error recovery is complete, the user may switch the VCEP into multi-line mode to process the remainder of the page.

When an error is detected during MMR mode expansion, no recovery is possible; since the page has been encoded two-dimensionally, it is not possible to "pass over" the error without its having a cumulative effect on subsequent data. For this reason (inherent in MMR coding rather than the VCEP) the CCITT has specified that systems using MMR coding should implement error protection apart from the compression code, allowing an effectively error-free transmission environment for the MMR code.

When MH- or MR-coded images are expanded, the three combinations of codes in Table 4 describe four possible error conditions, which together with recovery procedures will be defined below:

Error Condition 1

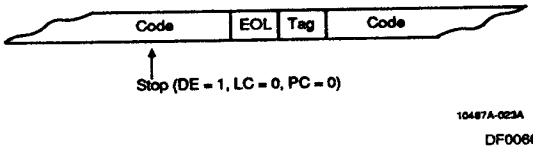


Figure 20. Error Condition 1

Status: DE = 1, LC = 0, PC = 0

1. The expanded line length is longer than the Line Length Register before the EOL code is detected.
2. A code indicating negative run length is detected.
3. An illegal code (but not a false EOL code) is detected. These are:

   0000 0000 1,
   0000 0000 01,
   and 0000 0000 001.

4. An illegal code is detected in horizontal mode where 1D-codes are expected.
5. In 2D-coding, the following illegal codes are detected:

   0000 001,
   and 0000 0001.

Recovery routine:

1. System must replace current scan line containing error with the last correctly expanded scan line.
2. System sets GO = 1.
3. VCEP will search for the next EOL to determine where to restart expansion.

Note that for MR coding, errors will rapidly compound in 2D-coded sections of the image; each time a 2D line is detected in error, it is flagged with a DE = 1 status. Therefore, even for MR coding, the user is only required to administer error recovery on a line-by-line basis.

Error Condition 2

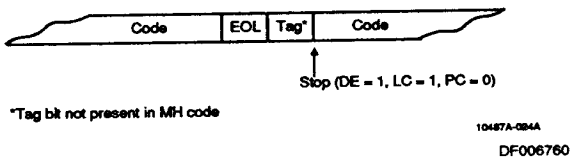


Figure 21. Error Condition 2

Status: DE = 1, LC = 1, PC = 0

1. The expanded line length is shorter than the Line Length Register when the EOL is detected.
2. False EOL codes are detected.
3. Two consecutive EOLs are detected (see Figure 22).

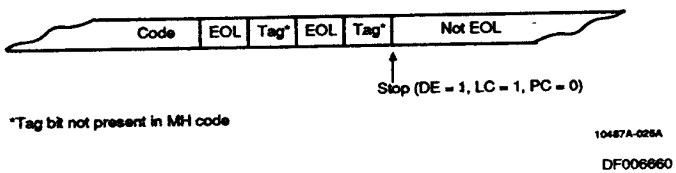
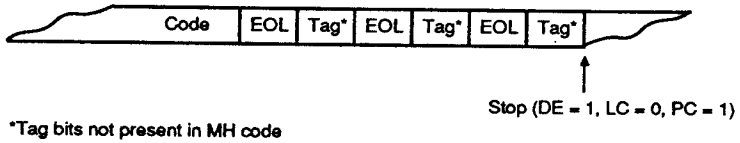


Figure 22. Error Condition 2 with Two EOLs

Recovery routine:

1. System must replace current scan line containing error with the last correctly expanded scan line.
2. System sets GO = 1.
3. The VCEP will start expanding the next line immediately, as it has already detected the EOL code. The DE bit is cleared when the system sets GO = 1.

Error Condition 3



*Tag bits not present in MH code

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Figure 23. Error Condition 3

Status: DE = 1, LC = 0, PC = 1

The VCEP detects a short line (less than LLR) when the end of page (RTC) has been detected. Note that although the VCEP detects the Tag bits within EOL codes, it will not indicate an error based on the value of these Tag bits.

MH and MR recovery routine:

1. System must replace current scan line containing error with the last correctly expanded scan line.
2. System must issue a software Reset to the VCEP.
3. After allowing a minimum of eight clock cycles from issuing the reset, the system may set up parameters for a new page.

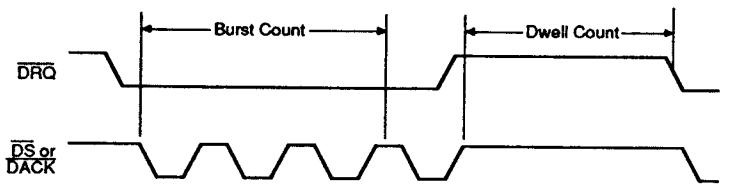
BUS BURST AND DWELL CONTROL

The VCEP is capable of processing up to 16 bits of data every three clock cycles. This may require a bus master to be able to regulate the amount of time for which the VCEP may request data transfer. The VCEP, therefore, has two identical and independent Burst-Dwell counters (one for each bus) that can be used to help regulate bus activity. The burst count specifies the maximum time the VCEP will hold a request active, while the dwell count specifies the minimum time the VCEP will wait, after taking request lines inactive and before requesting service again.

The Burst Count Register contains two 8-bit burst count values, one for the CPU bus and one for the Image bus. The burst count specifies the maximum number of clock cycles the VCEP will hold the request lines active and is given by:

(Burst Count Value 1) x 4

The counter starts decrementing at the beginning of the first access, to or from the FIFO Data Port, in either fly-by or flow-through mode. Once the burst counter expires all active requests associated with a particular bus will remain active until the beginning of the next transfer on that bus. At that time they will be taken inactive (see Figure 24).



Note: $\overline{DRQ}$ may be either $\overline{DRQ1}$ or $\overline{DRQ2}$; $\overline{DACK}$ then refers to $\overline{DACK1}$ or $\overline{DACK2}$, respectively.

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Figure 24. Bus Burst and Dwell Timing

A burst count of one will ensure that the VCEP only does a single transfer each time it accesses the bus. If the burst counter is set to zero it is disabled, effectively allowing an unlimited burst time.

When all requests associated with a particular bus are taken inactive before the burst counter expires (because the source or destination buffers have been filled or emptied), the VCEP will take its request line inactive and give up the bus. In the case where the burst counter expires while a source buffer request is active, the system may have given the complete (coded or uncoded) image to the VCEP, but since the burst counter has expired, the VCEP is waiting for one more transfer before removing its data transfer request. In this case a software Reset is necessary, making all request lines inactive.

If the burst count is not set to zero, the burst counter may expire before all requests have been completely serviced. The source buffer requests service when there are at least eight empty locations in the source buffer. The destination buffer requests service when at least eight words are in the destination buffer or the buffer is being emptied at the end of a line (single-line mode) or page. When the burst counter expires prior to completely servicing these requests, active requests are removed for the duration of the dwell count and are then reactivated.

The Dwell-Offset Register contains two 6-bit count values, one for each bus, and a 4-bit left-offset value applied to the first word of each scan line. The dwell count specifies the minimum number of clock cycles to wait (from the end of a burst cycle), before the VCEP will reactivate service requests ($\overline{DREQ1}$ and/or $\overline{DREQ2}$). The minimum dwell time is given by:

(Dwell Count Value) x 8

The dwell counter starts at the end of the last bus access of a burst, to or from the FIFO Data Port (see Figure 24). Setting the dwell count to zero will result in a minimum dwell time. For both burst and dwell counts, the actual times the VCEP requests data transfer may vary due to synchronization of the data strobe ($\overline{DS}$ or $\overline{IDS}$) and data acknowledge ($\overline{DACK1}$ or $\overline{DACK2}$) signals to the VCEP's input clock.

GUIDE TO VCEP THROUGHPUT CALCULATIONS

VCEP throughput in compression or expansion is dependent on the specific data input. The stated throughput of 50 Mb/s is based on the average throughput achieved over the CCITT standard documents numbers 4 and 7, when scanned at 200 dpi; these are the most complex of the eight standard documents, with the lowest compression ratio and therefore the lowest throughput on the VCEP. The other six CCITT documents should achieve higher throughput, as would documents scanned at higher resolutions, since they will compress better.

The most specific information on throughput may be obtained by analysis of a given image file. The VCEP, whether compressing or expanding, processes one run length of up to 16 bits in three clock cycles. If the maximum clock rate of 20 MHz is used, one run length up to 16 bits will be processed every 150 ns. This means that if an image consisting of alternating black and white pixels is compressed by the VCEP, it will be processed at one bit per 150 ns, or 6.67 Mb/s. At the other extreme, an all-white image will be processed at 16 bits per 150 ns, or 106.7 Mb/s. Typical documents rarely contain alternating run lengths of unit length. While each document is unique, our analysis shows that the worst sections of the CCITT documents contain five run lengths per 16 bits. In this practical worst-case condition the VCEP would still throughput data in excess of 20 Mb/s.

The above discussion centers on the VCEP's engine speed, but other factors must be taken into account, including the smoothing effect of the source and destination buffers which each hold sixteen words.

The most important issue affecting throughput will often be the handling of raw image data. Assuming a dual-bus VCEP system in expansion mode (for optimum throughput), image data must be removed by the system from the VCEP's destination buffer at a rate at least equal to the engine speed to provide maximum system throughput. This area will be addressed below.

To ensure maximum throughput, a dual-bus system is required with the code buffer on the CPU bus and the image buffer on the Image bus. Also, certain settings of VCEP programmable parameters are necessary. The bus burst value should be maximum especially on the Image bus, and dwell values should be minimum.

The above throughput numbers apply to compression and expansion when in MMR mode. Since MMR coding is the most complex, MR and MH code compression or expansion will yield higher throughput. Also, throughput in Transparent mode will be 16 bits per three clocks.

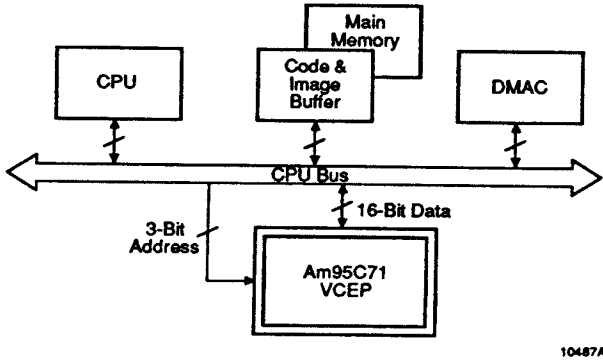

Figure 25. Single-Bus Configuration

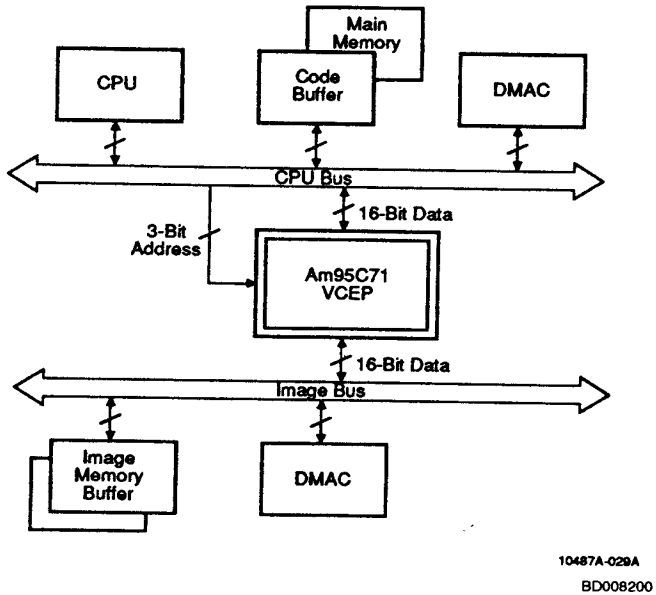

Figure 26. Dual-Bus Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Maximum V_{CC} Relative to V_{SS} ..... −0.3 to +7.0 V
DC Voltage Applied to Any Pin
Relative to V_{SS} ..... −0.5 to V_{CC} + 0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		−0.5	+ 0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA		+ 0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = 250 µA	2.4		V
I_{LI}	Input Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0.45 < V_{OUT} < V_{CC}		±10	µA
I_{CC}	Power Supply Current			250	mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Pin Capacitance	f_C = 1 MHz		10	pF
C_{OUT}	Output Pin Capacitance			15	pF
$C_{I/O}$	I/O Buffer Capacitance			20	pF

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SWITCHING CHARACTERISTICS over operating range (T_A = 0 to +70°C, V_{CC} = 5 V ± 5%)

No.	Parameter Symbol	Parameter Description	95C71-20		95C71-16		Unit
			Min.	Max.	Min.	Max.	
1	t_{PD}	Clock Period	50	500	62	500	ns
2	t_{PWH}	Clock HIGH Time	23		28		ns
3	t_{PWL}	Clock LOW Time	23		28		ns
4	t_R	Clock Rising Time		5		5	ns
5	t_F	Clock Falling Time		5		5	ns
6	t_S	Address Valid to $\overline{DS}$ FE Setup Time	10		12		ns
7	t_S	$\overline{CS}$ Valid to $\overline{DS}$ FE Setup Time	0		0		ns
8	t_S	R/$\overline{W}$ Valid to $\overline{DS}$ FE Setup Time	10		12		ns
9	t_{SKEW}	$\overline{DS}$ FE to Data Output Valid Delay				85	ns
10	t_{SKEW}	$\overline{DS}$ FE to $\overline{DRQ}$ RE Delay		60		70	ns
11	t_H	$\overline{DS}$ RE to Data Output Hold Time			0		ns
12	t_{SKEW}	$\overline{DS}$ RE to Data Out Float Delay		50		55	ns
13	t_H	$\overline{DS}$ RE to R/$\overline{W}$ Valid Hold Time	0		0		ns
14	t_H	$\overline{DS}$ RE to $\overline{CS}$ Valid Hold Time	0		0		ns
15	t_H	$\overline{DS}$ RE to Address Valid Hold Time	0		0		ns
16	t_{PWL}	$\overline{DS}$ LOW Width (Note 2)	70		90		ns
17	t_S	Data In Valid to $\overline{DS}$ FE Setup Time	50		60		ns
18	t_H	$\overline{DS}$ RE to Data Valid Hold Time	0		0		ns
19	t_{PWH}	$\overline{CS}$ HIGH Width	65		70		ns
20	t_S	$\overline{DACK}$ FE to $\overline{DS}$ FE Setup Time	0		0		ns
21	t_{PWH}	$\overline{DS}$/$\overline{DACK}$ HIGH Width	65		70		ns
22	t_{SKEW}	$\overline{DS}$ RE to $\overline{INTR}$ RE Delay Time		100		100	ns
23	t_{PWL}	$\overline{RESET}$ LOW Width	(Note 1)		(Note 1)		ns

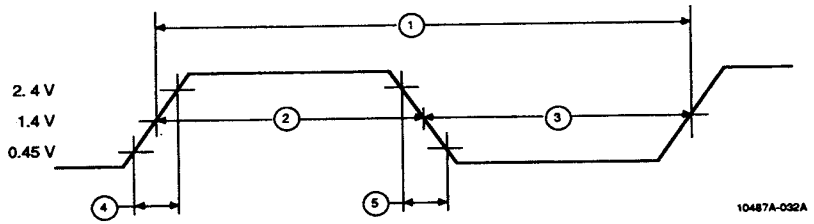
Notes: 1. Minimum $\overline{RESET}$ LOW Width is four clock periods (see parameter 1).
2. No more than one complete data transfer cycle can occur in each VCEP clock cycle. One data transfer may occur on each bus of a dual-bus system since the buses are fully independent. In addition, the maximum low pulse of $\overline{DS}$ cannot exceed 15 VCEP clock cycles.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



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Clock Timing

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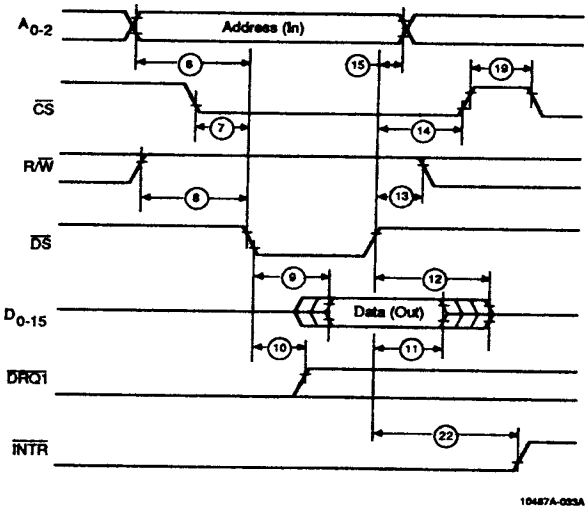
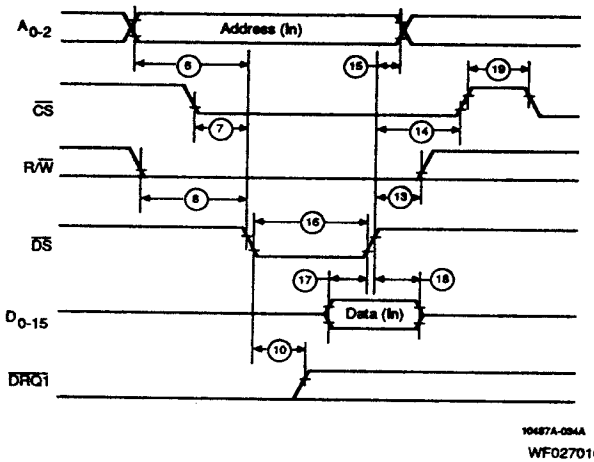


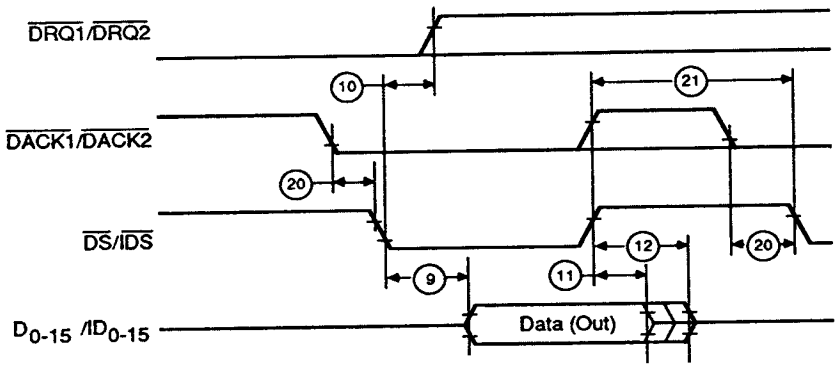
WF026570

CPU Program/DMA Flow-Through Mode Read Timing



WF027010

CPU Program/DMA Flow-Through Mode Write Timing

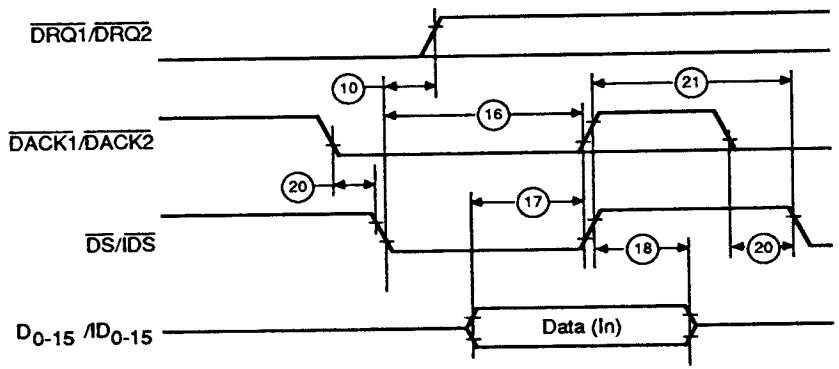


Note: Parameters 11, 12, and 21 are with respect to DS/IDS or DACK1/DACK2 inactive, whichever is sooner.

10487A-035A

WF026590

DMA Fly-by Mode Read Timing



Note: Parameters 17, 18, and 21 are with respect to DS/IDS or DACK1/DACK2 inactive, whichever is sooner.

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DMA Fly-by Mode Write Timing

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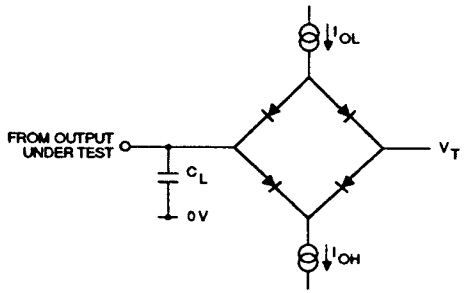
SWITCHING TEST CIRCUIT

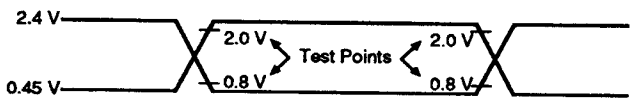


AF004810

Notes: 1. C_L = 100 pF (includes text fixture capacitance).

SWITCHING TEST WAVEFORM

(Input)



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