Pixel
Semiconductor
A Cirrus Logic Company

CL-PX2080

Preliminary Data Sheet

MediaDAC™

FEATURES

- **Direct ISA/MCA bus interface**
- **Interlaced or non-interlaced output**
- **Pixel clock rates up to 85 MHz**
- **Video inputs**
  - — 8:8:8 RGB at 40 MHz
  - — (1)5:5:5 (T)RGB at 85 MHz
  - — 5:6:5 RGB
  - — 4:2:2 YUV at 85 MHz
  - — Tagged or untagged 4:2:2 YUV at 85 MHz
- **Zoom controls**
- **Hardware cursor controls**
- **Three overlay combination controls**
  - — Tagged chroma color key
  - — Graphics overlay color key
  - — X/Y window
- **Graphics input**
  - — 4-bit or 8-bit pseudocolor at 85 MHz
  - — 5:6:5 RGB at 85 MHz
  - — 5:5:5 RGB at 85 MHz
  - — 8:8:8 RGB at 40 MHz

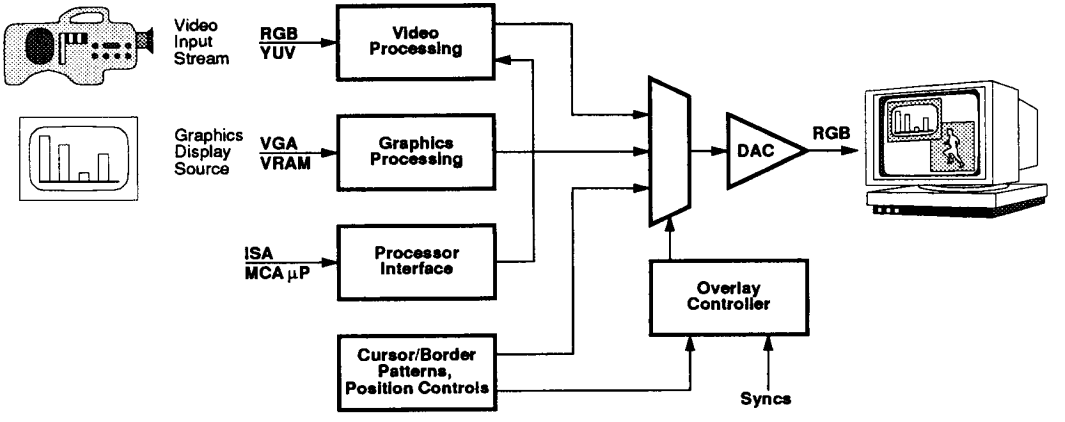
APPLICATIONS

- **Presentations**
- **Video Editing**
- **Video Authoring**
- **Video Teleconferencing**
- **Interactive Education**
- **Games**

OVERVIEW

The CL-PX2080 MediaDAC™ is a multiple-source, digital-to-analog video converter. It manages and mixes two different input video data streams while converting the input data into the format of the display subsystem. It also changes color space and resolution from the input format to the output format in real time. A simplified block diagram of the CL-PX2080 is shown below.

Simplified Functional Block Diagram



December 1992

ARCHTECTURAL OVERVIEW

This section describes the architecture and functionality of the CL-PX2080 MediaDAC.

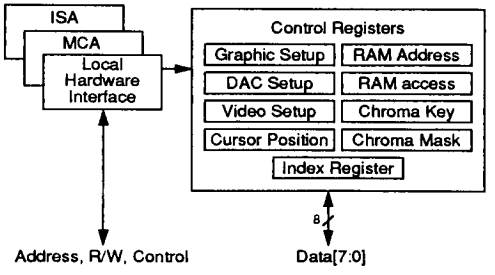
The CL-PX2080 has a video port for YCbCr or RGB data and a graphics port with both 8-bit VGA and 32-bit high-resolution ports. Its interfaces are described below. Its display functions include:

- pseudocolor,
- display of true-color RGB data,
- X zooming,
- hardware cursor controls, and
- a combination of three graphics overlay controls.

Host System Interface

The CL-PX2080 connects directly to ISA and MCA buses, internally decoding a 16-bit address and responding as an 8-bit peripheral. Its internal ISA/MCA bus interface eliminates most of the costly 'glue' circuitry common to many personal-computer-system expansion boards.

HIU Functions



As illustrated, the Host Interface Unit contains the bus interface and the configuration, control, and status registers.

In response to customer demands for increased performance, industry has encouraged migration of the display subsystem onto the host processor bus. The CL-PX2080 is designed to accommodate this trend with its Local Hardware Interface Mode.

Video Input Interface

The Video Input Interface accepts digitized video in a wide range of formats. The CL-PX2080 converts the video data stream to its final output format and then mixes and/or overlays it with processed graphics data and cursor data. The video processing functions are illustrated in the figure below.

Features:

- 36-bit input data path
- internal 256 x 36 bit input FIFO that supports:
  - — 24-bit RGB data (up to 40 mega-pixels)
  - — 16-bit RGB or YCbCr data (up to 85 mega-pixels)
- chrominance format alignment
- color-space interpolation
- zoom control.

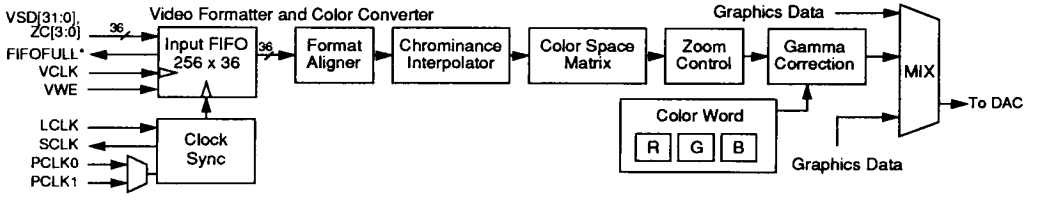
Graphics Frame Buffer Interface

The CL-PX2080 accepts data from the graphics display source through either of two paths:

- an 8-bit VGA serial data path, or
- a 32-bit VRAM serial data path.

As a result, PC graphics subsystems based on the CL-PX2080 chip can maintain compatibility with both the VGA systems and the VRAM systems. The VGA path supports a large, existing installed base of systems and VGA-specific software. The VRAM path supports the next generation of higher-performance and higher-resolution products.

Video Processing Functions



Features:

- VRAM Interface:
  - — 32-bit data bus
  - — efficient pixel mapping within graphics-data word
  - — accepts data from VRAM serial ports; can be used with a variety of architectures
- VGA Interface
- true-color (CLUT bypass) option.

The figure below shows the functional block diagram for graphics processing.

Graphics Overlay Control

The graphics overlay controls allow a video image and a graphics image to be combined using a variety of operations (see the figure below).

Every graphics pixel is either transparent or opaque. The color information for an opaque pixel is displayed on the screen. The color information for a transparent pixel is not displayed; instead, the color information of the video pixel behind it is displayed on the screen. The graphics overlay controls determine which graphics pixels are transparent. The CL-PX2080 has 256 possible overlay combinations based on the video-pixel tag bit, the graphics-pixel overlay color, and the XY window of the video data.

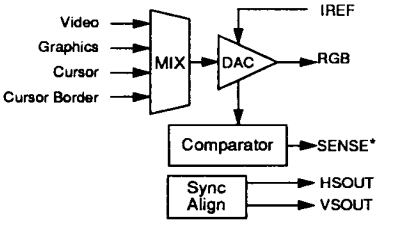
Cursor

The CL-PX2080 implements an on-chip, three-color, user-definable hardware cursor in a 32 x 32 x 2 bit memory. This cursor works in both interlaced and non-interlaced systems.

Output DACs

The CL-PX2080 has three video-speed, 8-bit digital-to-analog converters, internal comparators to provide the sense function, and sync alignment logic. These form a complete RGB monitor interface, as illustrated below.

RGB Monitor Interface



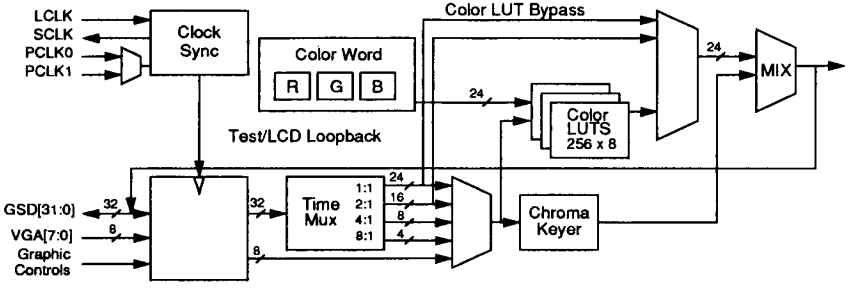
Power Down Mode

During the CL-PX2080's power-down condition, the DACs are turned off and the RAM enters a low-power, data-retaining standby mode. The processor can read from or write to the RAM as long as the pixel clock is running. The RAM automatically powers-up during processor read/write cycles and shuts-down when processor access is completed.

SOFTWARE SUPPORT

Pixel Semiconductor provides a complete solution for computer-based video. Our multilevel software support assures a quick product-development cycle that meets today's time-to-market requirements.

Graphics Processing Functions



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CONVENTIONS

Conventions used in this document are described in the following table:

GCKc	Register names that contain lower-case variables represent groups of registers with similar functions. For example, GCKc represents *all* of the Graphics Chroma Key registers — GCKR (Graphics Chroma Key Red), GCKG (Graphics Chroma Key Green), and GCKB (Graphics Chroma Key Blue). Table 4–1 on page 53 defines all variables used in this manner.

ABBREVIATIONS, ACRONYMS, and MNEMONICS

Abbreviations, acronyms, and mnemonics used in this documents are described in the following table:

CPU	Central Processing Unit
CRT	Cathode Ray Tube
DMA	Direct Memory Access
FIFO	First In First Out
ISA	Industry Standard Architecture
LSB	Least Significant Byte
LSb	Least Significant bit
LUT	Look-Up Table
MCA	Micro Channel Architecture
MSB	Most Significant Byte
MSb	Most Significant bit
PQFP	Plastic Quad Flat Pack
RGB	Red, Green, Blue
RAM	Random Access Memory
VRAM	Video Dynamic Random Access Memory

TRADEMARKS

Trademarks used in this document are described in the following table:

MediaDAC	is a trademark of Pixel Semiconductor, Inc.
HiCOLOR	is a trademark of Sierra Semiconductor.

1. PIN INFORMATION

The CL-PX2080 MediaDAC is available in a 160-pin Plastic Quad Flat Pack (PQFP) device that can be configured for ISA, MCA, or local hardware interface bus implementation.

1.1 Pin Diagrams

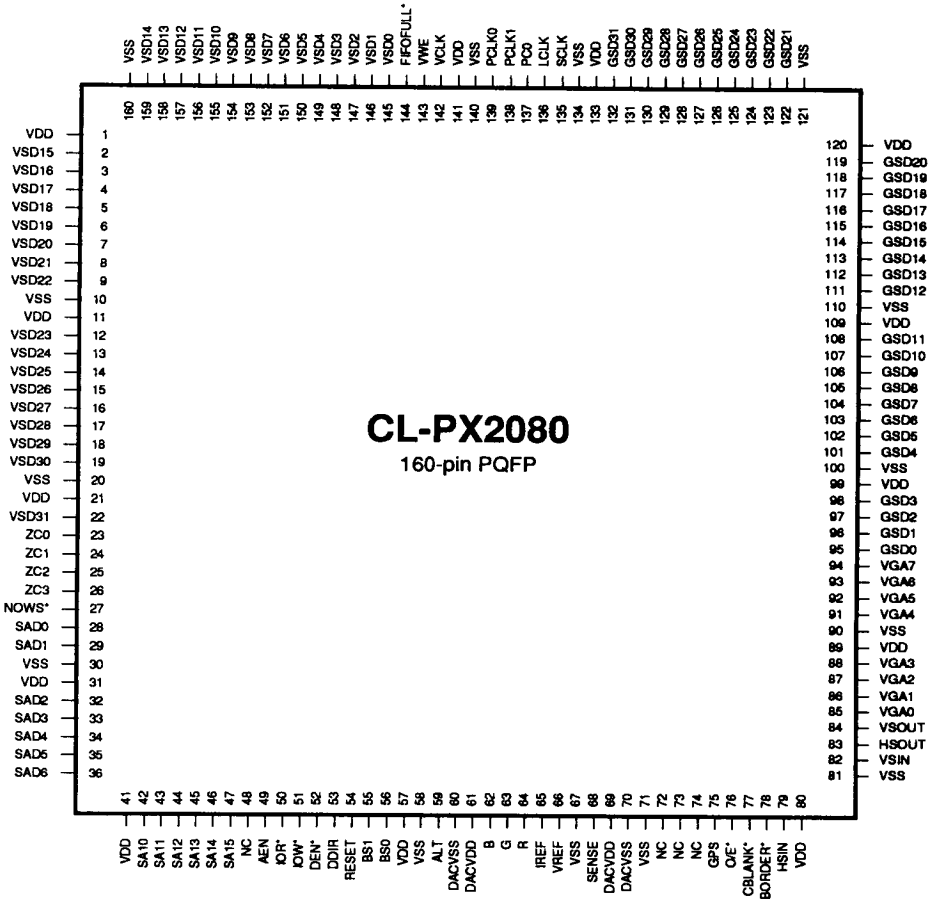


Figure 1–1. Pin Diagram — ISA Bus Configuration

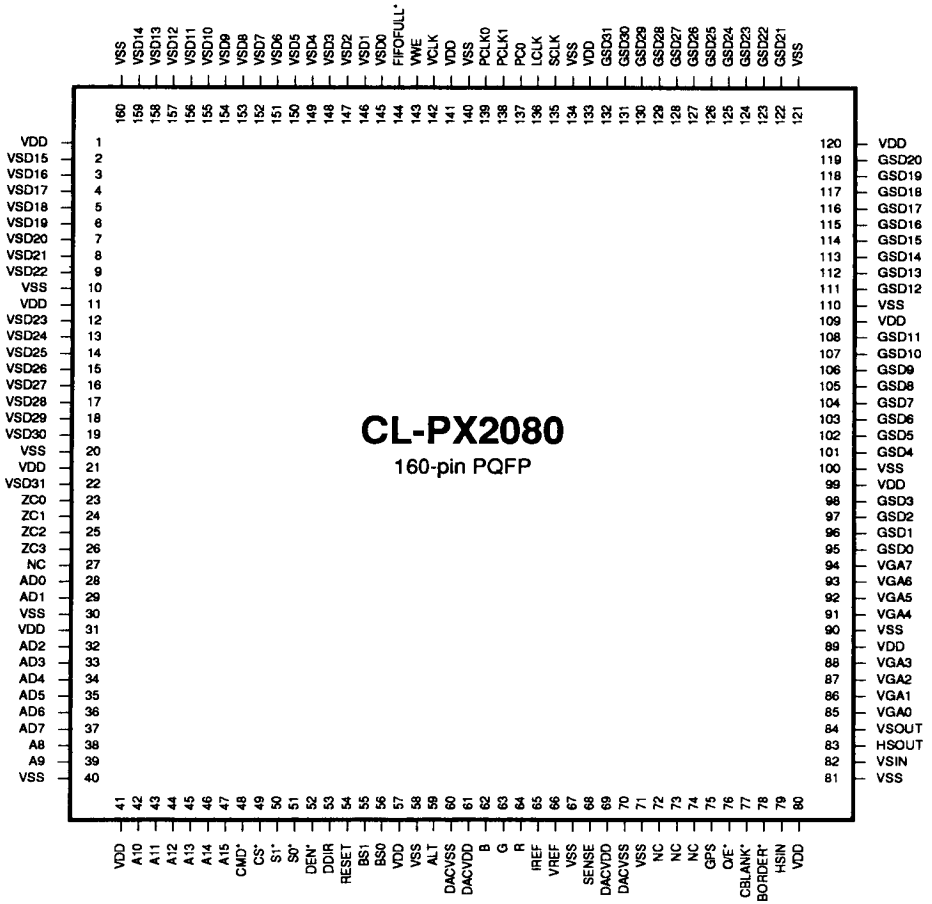


Figure 1–2. Pin Diagram — MCA Bus Configuration

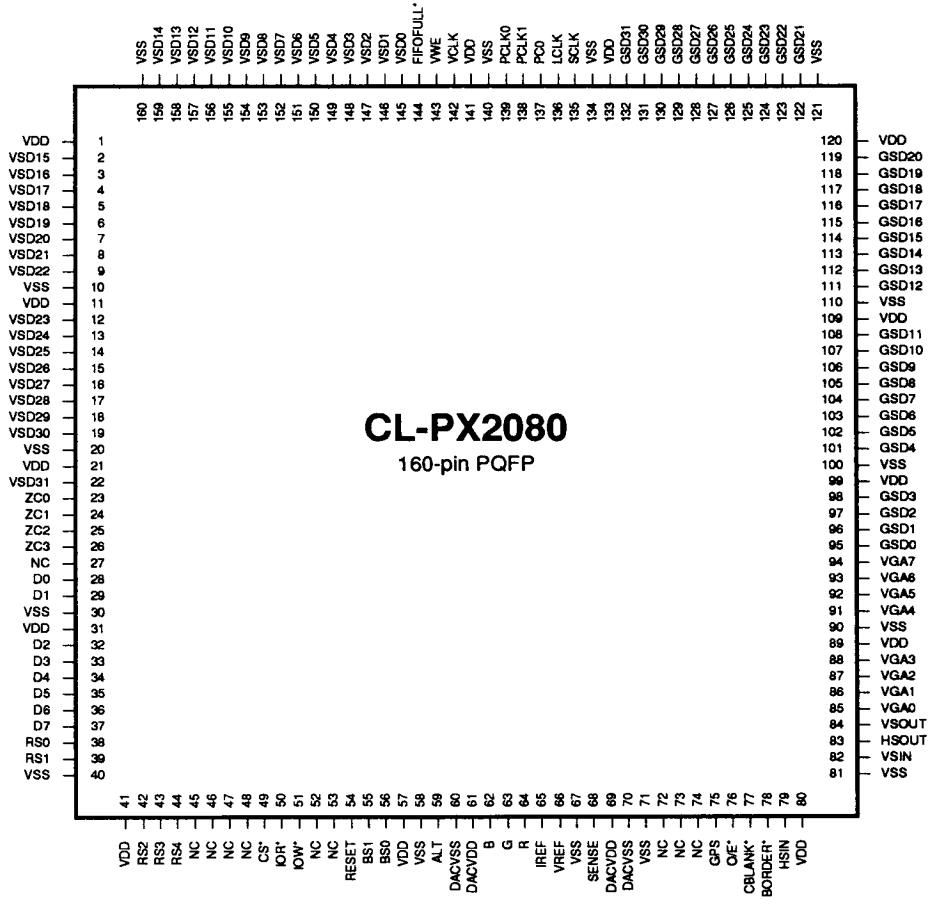


Figure 1–3. Pin Diagram — Local Hardware Interface Configuration

1.2 Pin Assignment Table

The following conventions are used in the pin assignment table:

*	= negative-true (active-low) signal
I	= input
O	= output
AN	= analog signal
PU	= internal pull-up
PD	= internal pull-down
PWR	= power
TTL	= the pad has standard TTL input threshold and TTL output levels
CMOS	= the pad has standard CMOS input threshold and CMOS output levels
3S	= three-state TTL drive capability
OD	= open drain, TTL inputs
4	= 4-mA sink and 2-mA source drive capability
12	= 12-mA sink and 4-mA source drive capability
24	= 24-mA sink and 8-mA source drive capability

NAME	PIN	TYPE	CELL	FUNCTION
PROCESSOR INTERFACE — ISA BUS MODE SUMMARY				
SA[15:8]	47:42, 39:38	I	TTL	CPU Address High Byte
SAD[7:0]	37:32, 29:28	I/O	3S, 8	CPU Address and Data Low Byte
IOR*	50	I	TTL	I/O Read
IOW*	51	I	TTL	I/O Write
AEN	49	I	TTL	Address Enable
RESET	54	I	TTL	Reset
NOWS*	27	O	OD, TTL, 24	No Wait State
DEN*	52	O	OD, TTL, 8	Data Buffer Enable
DDIR	53	O	OD, TTL, 8	Data Buffer Direction
BS[1:0]	55:56	I	TTL	Bus Select
ALT	59	I	TTL	BIR alternate address select
NC	48	N/A	N/A	No Connect (must be left floating)
PROCESSOR INTERFACE — MCA BUS MODE SUMMARY				
A[15:8]	47:42, 39:38	I	TTL	CPU Address High Byte
AD[7:0]	37:32, 29:28	I/O	3S, 8	CPU Address and Data Low Byte
NC	27	N/A	N/A	No Connect (must be left floating)
CMD*	48	I	TTL	Command
M/IO*	49	I	TTL	Memory or I/O Cycle
S1*	50	I	TTL	Status 1
S0*	51	I	TTL	Status 0
CDRESET	54	I	TTL	Reset
DEN*	52	O	OD, TTL, 8	Data Buffer Enable
DDIR	53	O	OD, TTL, 8	Data Buffer Direction
BS[1:0]	55:56	I	TTL	Bus Select
ALT	59	I	TTL	BIR alternate address select

NAME	PIN	TYPE	CELL	FUNCTION *(cont.)*
PROCESSOR INTERFACE — LOCAL HARDWARE INTERFACE MODE SUMMARY				
RS[4:0]	44:42, 39:38	I	PD, TTL	Register Select
D[7:0]	37:32, 29:28	I/O	3S, 8	Data
IOR*	50	I	TTL	I/O Read Cycle
IOW*	51	I	TTL	I/O Write Cycle
RESET	54	I	TTL	Reset
CS*	49	I	TTL	Chip Select
BS[1:0]	55:56	I	TTL	Bus Select
NC	53:52	N/A	N/A	No Connect (must be left floating)
NC	48	N/A	N/A	No Connect (must be left floating)
NC	47:45	N/A	N/A	No Connect (must be left floating)
NC	27	N/A	N/A	No Connect (must be left floating)
NC	59	N/A	N/A	No Connect (must be left floating)
GRAPHICS PORT INTERFACE				
GSD[31:0]	132:122, 119:111, 108:101, 98:95	I/O	PU, 3S, 8	Graphics Source Data
VGA[7:0]	94:91, 88:85	I	PU, TTL	VGA Graphics Source Data
PCLK0	139	I	TTL	Pixel Input Clock 0
PCLK1	138	I	TTL	Pixel Input Clock 1
LCLK	136	I	TTL	Latch Clock Input
SCLK	135	O	TTL, 12	VRAM Shift Clock Output
O/E*	76	I	TTL	Odd/Even Field Input
GPS	75	I	TTL	Graphics Port Select
BORDER*	78	I	TTL	Active Display Border
CBLANK*	77	I	TTL	Composite Blank Input
VSIN	82	I	TTL	Vertical Sync Input
HSIN	79	I	TTL	Horizontal Sync Input
VSOUT	84	O	TTL, 8	Vertical Sync Output
HSOUT	83	O	TTL, 8	Horizontal Sync Output
PC0	137	O	TTL, 12	Pixel Clock Output
VIDEO PORT INTERFACE				
VSD[31:0]	22, 19:12, 9:2, 159:145	I	PU, TTL, 8	Video Source Data
ZC[3:0]	26:23	I	TTL	Zoom Control Code
FIFOFULL*	144	O	TTL, 8	FIFO Full Indication
VCLK	142	I	TTL	Video Clock Input
VWE	143	I	TTL	Video FIFO Write Enable

NAME	PIN	TYPE	CELL	FUNCTION *(cont.)*
MONITOR INTERFACE				
R	64	O	AN	Analog Red
G	63	O	AN	Analog Green
B	62	O	AN	Analog Blue
IREF	65	I	AN	Current Reference
SENSE	68	O	TTL, 8	Monitor Sense
VREF	66	I	AN	Voltage Reference Input
POWER INTERFACE				
VDD	1, 11, 21, 31, 41, 57, 80, 89, 99, 109, 120, 133, 141	PWR		+5 Volts DC for Digital Logic and Interface Buffers
VSS	10, 20, 30, 40, 58, 67, 71, 81, 90, 100, 110, 121, 134, 140, 160	PWR		Ground for Digital Logic and Interface Buffers
DACVDD	61, 69	PWR		+5 Volts DC for DAC
DACVSS	60, 70	PWR		Ground for DAC
NO CONNECTS				
NC	72	N/A	N/A	No Connect (must be left floating)
NC	73	N/A	N/A	No Connect (must be left floating)
NC	74	N/A	N/A	No Connect (must be left floating)

2. DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface — ISA Bus Mode

Signal	Pin	Type	Cell	Function
SA[15:8]	47:42, 39:38	I	TTL	**CPU Address High Byte:** Specifies the resource to be accessed during an I/O or memory cycle.
SAD[7:0]	37:32, 29:28	I/O	3S, 12	**CPU Address and Data Low Byte:** The lower byte of address is externally multiplexed with the low byte of data to transfer data to and from the CL-PX2080 during an I/O cycle.
IOR*	50	I	TTL	**I/O Read:** Specifies an I/O read cycle.
IOW*	51	I	TTL	**I/O Write:** Specifies an I/O write cycle.
AEN	49	I	TTL	**Address Enable:** Specifies that a DMA cycle is in progress. The CL-PX2080 responds to I/O cycles when AEN is asserted low.
RESET	54	I	TTL	**Reset:** Causes the CL-PX2080 to cease all activity and perform a hardware reset.
NOWS*	27	O	OD, TTL, 24	**No Wait State:** Specifies that the host should run a zero-wait-state cycle. The default ISA bus cycle is one wait state.
DEN*	52	O	OD, TTL, 8	**Data Buffer Enable:** When pulled low, enables the host data bus buffer.
DDIR	53	O	OD, TTL, 8	**Data Buffer Direction:** Specifies the direction of data flow on bus SAD[7:0]. A high level specifies that the host system is driving data to SAD[7:0] (write cycle); a low level specifies that the CL-PX2080 is driving SAD[7:0] (read cycle) to the host system.
BS[1:0]	55:56	I	TTL	**Bus Select:** Specifies the bus mode for the operation of the CL-PX2080: 0 0 ISA Bus Mode 0 1 MCA Bus Mode 1 0 Local Hardware Interface Mode 1 1 Reserved
ALT	59	I	TTL	**BIR alternate address select:** Enables secondary ISA address range for BIR access. 0 Primary ISA address range 1 Secondary ISA address range
NC	48	N/A	N/A	**No Connect:** (must be left floating).

2.2 Processor Interface — MCA Bus Mode

Signal	Pin	Type	Cell	Function
A[15:8]	47:42, 39:38	I	TTL	**CPU Address High Byte:** Specifies the resource to be accessed during an I/O or memory cycle.
AD[7:0]	37:32, 29:28	I/O	3S, 12	**CPU Address and Data Low Byte:** Multiplexed with data externally to transfer data to and from the CL-PX2080 during an I/O cycle.
NC	27	N/A	N/A	**No Connect:** (must be left floating).
CMD*	48	I	TTL	**Command:** Specifies that valid data is on bus AD[7:0] during a write cycle, and specifies that the CL-PX2080 should place valid data on the bus during a read cycle.
M/IO*	49	I	TTL	**Memory or I/O Cycle:** Used with S1* and S0* to specify the current bus cycle: **M/IO* S0* S1*** 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Inactive
S1*	50	I	TTL	**Status 1:** This active-low signal works with M/IO* and S0* to specify the current bus cycle (see table under M/IO* above).
S0*	51	I	TTL	**Status 0:** Used with M/IO* and S1* to specify the current bus cycle (see table under M/IO* above).
CDRESET	54	I	TTL	**Reset:** Causes the CL-PX2080 to cease all activity and perform a hardware reset.
DEN*	52	O	OD, TTL, 8	**Data Buffer Enable:** When pulled low, enables the host data bus buffer.
DDIR	53	O	OD, TTL, 8	**Data Buffer Direction:** Specifies the direction of data flow on bus AD[7:0]. A high level indicates that the host system is driving data to AD[7:0] (write cycle); a low level indicates that the CL-PX2080 is driving AD[7:0] (read cycle) to the host system.
BS[1:0]	55:56	I	TTL	**Bus Select:** Specifies the bus mode selected for the operation of the CL-PX2080: 0 0 ISA Bus Mode 0 1 MCA Bus Mode 1 0 Local Hardware Interface Mode 1 1 Reserved

Signal	Pin	Type	Cell	Function *(cont.)*
ALT	59	I	TTL	**BIR alternate address select:** Enables secondary MCA address range for BIR access. 0 Primary MCA address range 1 Secondary MCA address range

2.3 Processor Interface — Local Hardware Interface Mode

Signal	Pin	Type	Cell	Function
RS[4:0]	44:42, 39:38	I	PD, TTL	**Register Select:** Specifies the internal register to be accessed during a CL-PX2080 I/O cycle.
D[7:0]	37:32, 29:28	I/O	3S, 12	**Data:** Bidirectional data bus that accesses the internal control registers.
IOR*	50	I	TTL	**I/O Read Cycle**: Specifies an I/O read cycle.
IOW*	51	I	TTL	**I/O Write Cycle**: Specifies an I/O write cycle.
RESET	54	I	TTL	**Reset:** Causes the CL-PX2080 to cease all activity and perform a hardware reset.
CS*	49	I	TTL	**Chip Select:** Specifies that the CL-PX2080 is being accessed by the host system.
BS[1:0]	55:56	I	TTL	**Bus Select:** Specifies the bus mode for the operation of the CL-PX2080: 0 0 ISA Bus Mode 0 1 MCA Bus Mode 1 0 Local Hardware Interface Mode 1 1 Reserved
NC	53:52	N/A	N/A	**No Connect:** (must be left floating).
NC	48	N/A	N/A	**No Connect:** (must be left floating).
NC	47:45	N/A	N/A	**No Connect:** (must be left floating).
NC	27	N/A	N/A	**No Connect:** (must be left floating).
NC	59	N/A	N/A	**No Connect:** (must be left floating).

2.4 Graphics Port Interface

Signal	Pin	Type	Cell	Function
GSD[31:0]	132:122, 119:111, 108:101, 98:95	I/O	PU, 3S, 8	**Graphics Source Data:** GSD[31:0] is selected when GPS is '1'. GSD[31:0] is a 32-bit VRAM serial data path that accepts data at 4, 8, and 16 bits per pixel. GPS selects either the VGA source or the GSD source into the graphical data path. GSD[31:0] is latched on the rising edge of LCLK. All unused bits must be connected to VSS. When CSC Register Bits (6,5) are both '1', the GSD Signals become graphics data outputs as follows: GSD[23:16] to R[7:0] GSD[26] to WINACT GSD[15:8] to G[7:0] GSD[25] to VSOUT GSD[7:0] to B[7:0] GSD[24] to HSOUT (This is primarily a test mode feature but may interface to LCD controller. This output mode will not run at maximum frequency.)
VGA[7:0]	94:91, 88:85	I	PU, TTL	**VGA Graphics Source Data:** VGA[7:0] is selected when GPS is '0'. VGA[7:0] is latched on the rising edge of LCLK. All unused bits must be connected to VSS.
PCLK0	139	I	TTL	**Pixel Input Clock 0:** PCLK0 is the VGA input clock; it is selected when Bit 4 of the CSC Register is '0'.
PCLK1	138	I	TTL	**Pixel Input Clock 1:** PCLK1 is the high-speed GSD[31:0] input clock used during multiplexed operation of the 32-bit VRAM serial pixel port; it is selected when Bit 4 of the CSC Register is '1'.
LCLK	136	I	TTL	**Latch Clock Input:** The rising edge of LCLK latches GSD[31:0] or VGA[7:0], and BLANK*, HSIN, VSIN, GPS, and BORDER*, which are then synchronized internally with SCLK. To avoid metastability, LCLK must maintain setup and hold requirements to SCLK. Data is synchronized with PCLKn after being internally latched with SCLK. When the input data multiplexing rate is 8:1, 4:1, 2:1, or 1:1, LCLK must equal PCLKn divided by 8, 4, 2, or 1, respectively.
SCLK	135	O	TTL, 12	**VRAM Shift Clock Output:** SCLK equals PCLKn divided by 8, 4, 2, or 1, depending on the operating mode specified.
O/E*	76	I	TTL	**Odd/Even Field Input:** The cursor controller uses O/E* to ensure proper operation in Interlaced Mode, and ignores it in Non-interlaced Mode. O/E* should be changed only during vertical blanking.
GPS	75	I	TTL	**Graphics Port Select:** When GPS is asserted high and Bits (6,5) of the CSC Register are both '1', GSD[31:0] becomes the graphic port. When GPS is asserted low and Bits (6,5) of the CSC Register are both '1', VGA[7:0] becomes the graphics port. GPS is disabled when Bits (6,5) of the CSC Register are both '0'.

Signal	Pin	Type	Cell	Function *(cont.)*
BORDER*	78	I	TTL	**Active Display Border:** Used with CBLANK* and GPS to specify whether the DAC outputs are blanked or contain cursor, pixel, or border color, as shown below. BORDER* is '1' when a display border is not used. **CBLANK* BORDER* GPS** 0 X X Video blanking 1 0 X Border color 1 1 0 VGA or cursor color 1 1 1 GSD or cursor color
CBLANK*	77	I	TTL	**Composite Blank Input:** Applies a color value of '0' to the DAC inputs to produce black at the DAC outputs. The cursor position counters are referenced to CBLANK*.
VSIN	82	I	TTL	**Vertical Sync Input:** Generates a vertical sync pulse once every frame in Non-interlaced Mode and once every field in Interlaced Mode. VSIN is polarity programmable.
HSIN	79	I	TTL	**Horizontal Sync Input:** Generates a horizontal sync pulse every line. HSIN is polarity programmable.
VSOUT	84	O	TTL, 8	**Vertical Sync Output:** A polarity-programmable delay of HSIN.
HSOUT	83	O	TTL, 8	**Horizontal Sync Output:** A polarity-programmable delay of HSIN or a composite SYNC generated from HSIN and VSIN, as determined by the SAR Register.
PCO	137	O	TTL, 12	**Pixel Clock Output:** Buffered output of pixel clock selected by the CSC Register. See Section 4.4.3 on page 64 for additional information.

2.5 Video Port Interface

Signal	Pin	Type	Cell	Function
VSD[31:0]	22, 19:12, 9:2, 159:145	I	PU, TTL, 8	**Video Source Data:** Port through which video data enters the CL-PX2080. The CL-PX2080 supports the following formats in both Tagged and Untagged Modes: 16-bit YUV (4:2:2), 16-bit RGB (5:6:5), 24-bit RGB (8:8:8). VCLK transfers 16-bit modes as two pixels per pixel word.
ZC[3:0]	26:23	I	TTL	**Zoom Control Code:** Specifies several options for interpolation and alignment of the input video stream on VSD[31:0] (when used with CL-PX2070).
FIFOFULL*	144	O	TTL, 8	**FIFO Full Indication:** Asserted low when a full-8 condition occurs in the 256-deep, double-pixel FIFO; indicates to the external video source that the FIFO is nearly full.
VCLK	142	I	TTL	**Video Clock Input:** On its rising edge, VCLK clocks VSD[31:0] and ZC[3:0] data into the CL-PX2080 input video FIFO. If VWE is high, VCLK is generated by the source video processor.
VWE	143	I	TTL	**Video FIFO Write Enable:** When VWE is asserted high, data is written on the rising edge of VCLK. When VWE is negated low, writes are disabled.

2.6 Monitor Interface

Signal	Pin	Type	Cell	Function
R	64	O	AN	**Analog Red:** The analog red channel from the 8-bit digital-to-analog converter.
G	63	O	AN	**Analog Green:** The analog green channel from the 8-bit digital-to-analog converter.
B	62	O	AN	**Analog Blue:** The analog blue channel from the 8-bit digital-to-analog converter.
IREF	65	I	AN	**Current Reference:** The required 8.8-mA reference current for the DAC.
SENSE	68	O	TTL, 8	**Monitor Sense:** A logical OR of the comparator outputs. Three level-detecting comparators individually monitor the red, green, and blue DAC outputs. A maximum analog DAC output level generates a high-level comparator output. A minimum analog level produces a low-level comparator output.
VREF	66	I	AN	**Voltage Reference:** The required 1.23V reference voltage for the DAC.

2.7 Power

Signal	Pin	Type	Cell	Function
VDD	1,11,21, 31, 41, 57, 80, 89, 99, 109, 120, 133, 141	PWR		**+5 Volts DC for Digital Logic and Interface Buffers:** Each VDD pin must be connected directly to the VDD plane.
VSS	10, 20, 30, 40, 58, 67, 71, 81, 90,100, 110, 121, 134, 140, 160	PWR		**Ground for Digital Logic and Interface Buffers:** Each VSS pin must be connected directly to the ground plane.
DACVDD	61, 69	PWR		**+5 Volts DC for DAC:** DACVDD must be decoupled from digital VDD with a ferrite bead or inductor.
DACVSS	60, 70	PWR		**Ground for DAC:** DACVSS must be connected to the analog ground plane.

2.8 No Connects

Signal	Pin	Type	Cell	Function
NC	72	N/A	N/A	**No Connect:** (must be left floating).
NC	73	N/A	N/A	**No Connect:** (must be left floating).
NC	74	N/A	N/A	**No Connect:** (must be left floating).

3. FUNCTIONAL DESCRIPTION

The CL-PX2080 MediaDAC is a multi-source, digital-to-analog video converter that can manage and mix two separate raster streams that have different color spaces and resolutions. As shown in the functional block diagram in Figure 3–1, the CL-PX2080 has three input ports:

- a video input port for YUV or RGB data, and
- two graphics input ports for 8-bit VGA or 32-bit high resolution graphics.

The output to the monitor can be pseudocolor or true-color RGB.

The CL-PX2080 MediaDAC also includes a hardware cursor and a combination of three graphics overlay controls. The video-processing functions of the CL-PX2080 MediaDAC include:

- format alignment,
- chrominance interpolation,
- color-space conversion,
- zoom, and
- gamma correction.

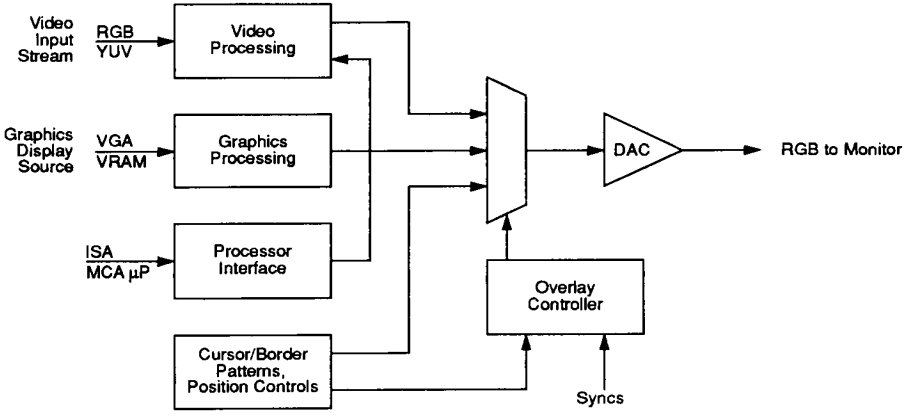


Figure 3–1. CL-PX2080 MediaDAC™ Simplified Functional Block Diagram

Figure 3–2 shows a more detailed CL-PX2080 MediaDAC block diagram.

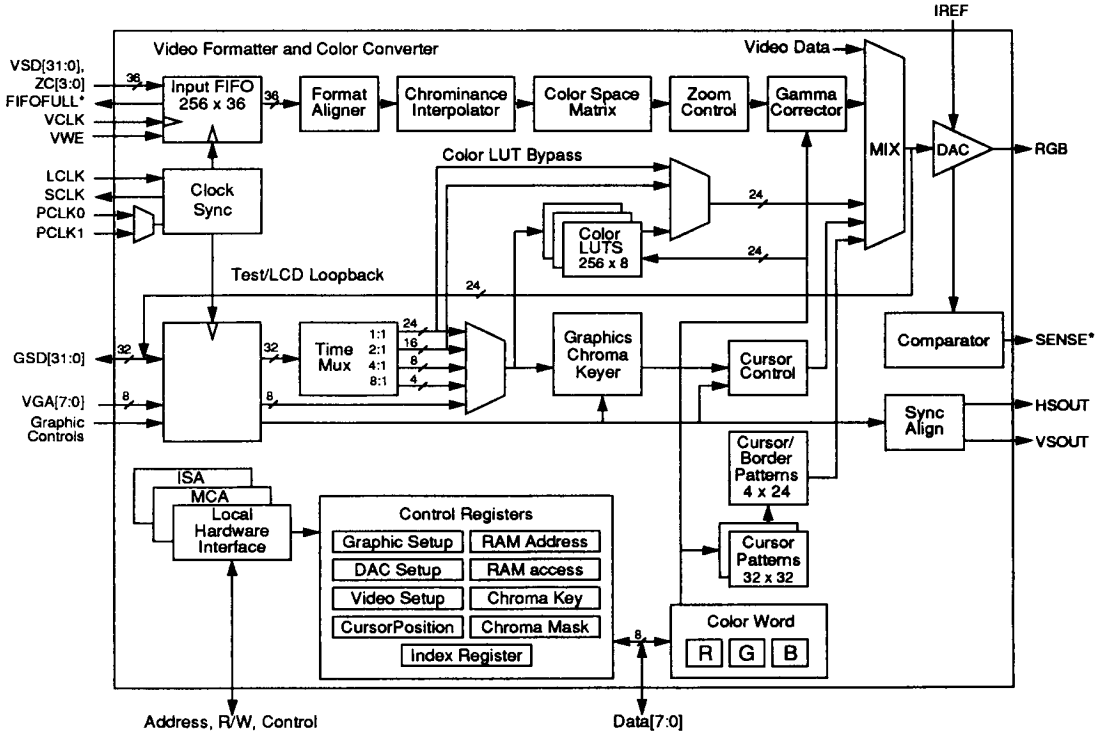


Figure 3–2. CL-PX2080 MediaDAC™ Detailed Block Diagram

As described in the following sections, the primary functions of the MediaDAC include:

- Host Bus Interface,
- Video Input Processing, and
- Graphics Frame Buffer Interface and Processing.

For additional detail concerning specific CL-PX2080 registers, refer to Section 4.

3.1 Host Bus Interface

The CL-PX2080 interfaces with three bus protocols:

- Industry Standard Architecture (ISA) bus,
- Micro Channel Architecture (MCA) bus, and
- Local hardware interface.

As shown in Table 3–1, the bus interface signals share a common set of I/O pins. For a complete pin assignment table, refer to Section 1.2 on page 13.

Table 3–1. Host System Bus I/O Pins

Pin	ISA Interface		MCA Interface		Local Hardware Interface	
27	NOWS*	O	NC	N/A	NC	N/A
[37:32,29:28]	SAD[7:0]	I/O	AD[7:0]	I/O	D[7:0]	I/O
[47:45]	SA[15:13]	I	A[15:13]	I	NC	N/A
[44:42,39:38]	SA[12:8]	I	A[12:8]	I	RS[4:0]	I
48	NC	N/A	CMD*	I	NC	N/A
49	AEN	I	M/IO*	I	CS*	I
50	IOR*	I	S1*	I	IOR*	I
51	IOW*	I	S0*	I	IOW*	I
52	DEN*	O	DEN*	O	NC	N/A
53	DDIR	O	DDIR	O	NC	N/A
54	RESET	I	CDRESET	I	RESET	I
[55:56]	BS[1:0]	I	BS[1:0]	I	BS[1:0]	I
59	ALT	I	ALT	I	NC	N/A

The CL-PX2080 connects directly to the ISA and MCA Buses, internally decoding a 16-bit address and responding as an 8-bit peripheral. An index and data register pair provide access to the internal registers. In Local Hardware Interface Mode, the address range is externally decoded to drive CS*, with RS[4:0] selecting individual CL-PX2080 registers. Bus-selection Pins BS[1:0] specify the host bus interface, as shown in Table 3–2.

Table 3–2. Bus Selection Pins

BS[1:0]	Bus Selected
00	ISA Bus
01	MCA Bus
10	Coprocessor Bus
11	Reserved

The following sections describe the configuration method for each bus.

3.1.1 ISA Bus Interface

The CL-PX2080 interfaces with the ISA Bus using the pins listed in the Pin Assignment Table on page 13 to support I/O read and write cycles. Since the LSB of the address and the data pins are multiplexed, a circuit similar to that shown in Figure 3–3 is required to prevent contention between address and data buffers.

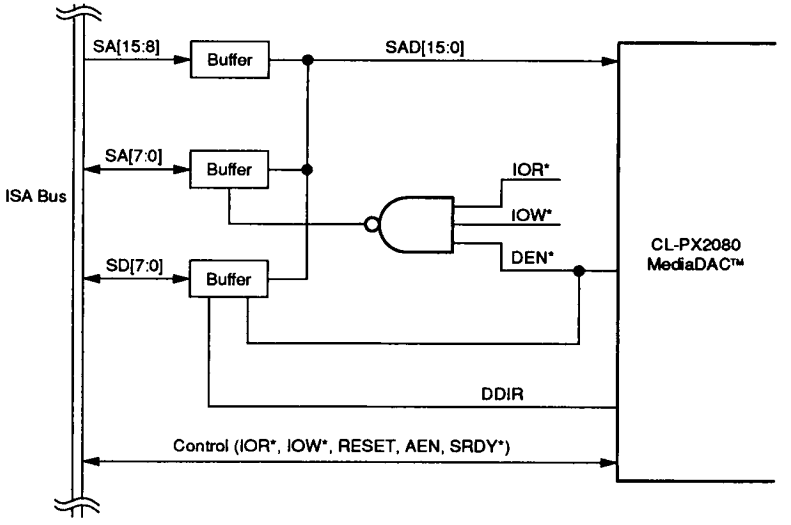


Figure 3–3. Example ISA Interface Circuit

The CL-PX2080 responds to I/O cycles on the ISA Bus. Figure 3–4 shows a typical ISA 8-bit I/O cycle and illustrates both the similarities and differences in the read and write cycles.

Following is the sequence of events for a read cycle:

1. A valid address within the address range of the CL-PX2080 stabilizes on the address bus. The CL-PX2080 decodes the address and asserts NOWS*.
2. The system asserts IOR*. Asserting IOR* causes the following:
   a. The CL-PX2080 latches the address on SA[15:8] and AD[7:0] on the falling edge of IOR*;
   b. The I/O buffers of AD[7:0] change from Input to Output Mode[1];
   c. DDIR goes low, using the external buffers to output to the SD bus;
   d. DEN* is asserted, disabling the address buffers and enabling the data buffers.
3. After the appropriate time interval, the system negates IOR* and latches the data from the SD Bus.
4. DDIR goes high.
5. DEN* is negated.
6. The I/O buffers of AD[7:0] change from Output to Input Mode.

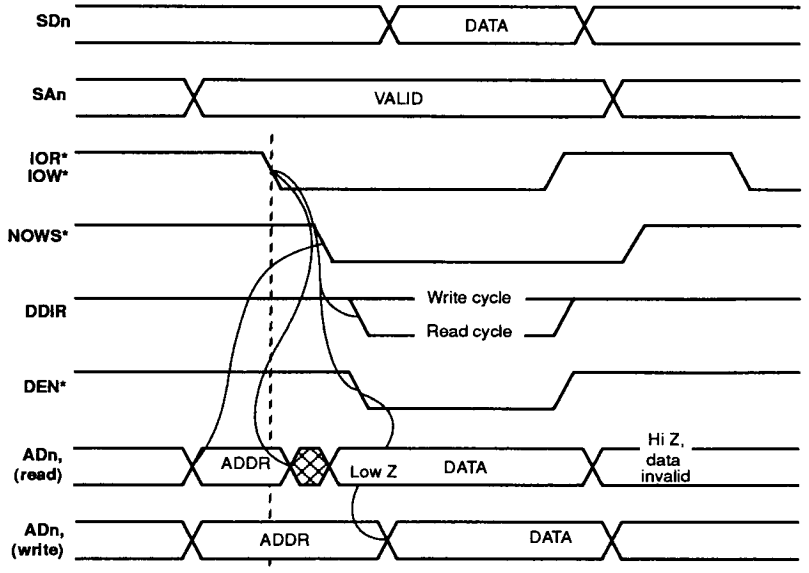


Figure 3–4. ISA 8-Bit I/O Cycle

1. The circuit should be designed to disable the low-byte address buffer on IOR* assertion.

3.1.2 MCA BUS Interface

The CL-PX2080 supports I/O read and I/O write cycles for the MCA environment. The connection of the multiplexed address and data pins to the MCA Bus is similar to the ISA Bus connection shown in Figure 3–3 on page 26. Refer to the detailed signal description in Section 2.1 on page 16 for the MCA Bus cycle decoding performed for Signals M/IO*, S0*, and S1* and for information about the ISA Bus interface.

3.1.2.1 MCA I/O Read

Figure 3–5 shows a typical MCA 8-bit I/O cycle. The CL-PX2080 latches the address present on A[15:8] and AD[7:0] on the falling edge of CMD*. During read operations, the CL-PX2080 provides valid data on the AD[7:0] bus before the rising edge of CMD*. The CL-PX2080 outputs the data fast enough so that no wait states are required. CD-CHRDY is normally pulled high in the MCA environment and does not need to be driven by the CL-PX2080. Since the CL-PX2080 is an 8-bit device, the MCA environment does not require it to drive the CDDS16* Signal.

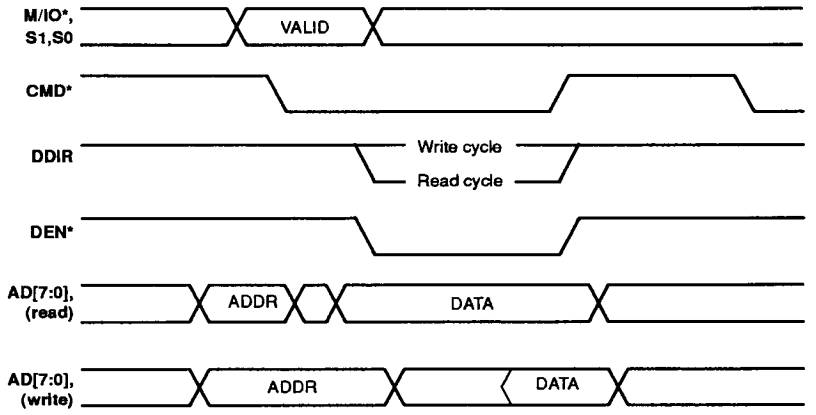


Figure 3–5. MCA 8-Bit I/O Cycle

3.1.3 Local Hardware Interface

The local hardware interface is used in a manner similar to a static RAM. The interface has four components that determine the read and write operations of the local hardware interface:

- an 8-bit, bidirectional data bus;
- chip-select input signal CS*, which is driven by an external address decoder;
- Signals RS[4:0], which select the register to be accessed and are typically connected to the lower five bits of the processor address bus;
- control pins RD* and WR*, which define read and write cycles.

These four components are described in the following sections.

3.1.3.1 Local Access Cycles

Figure 3–6 shows the timing of a local hardware access.

A read from the CL-PX2080 occurs when CS* and RD* are low. Data from the addressed control register is placed on D[7:0] where it may be sampled by the host between the minimum specified access time (see Section 5.5 on page 79) and the rising edge of RD*.

A write occurs when CS* and WR* are low. The host system asserts CS* after RS[4:0] are stable and then asserts WR*. Data must be valid for the specified setup and hold times relative to the rising edge of WR*.

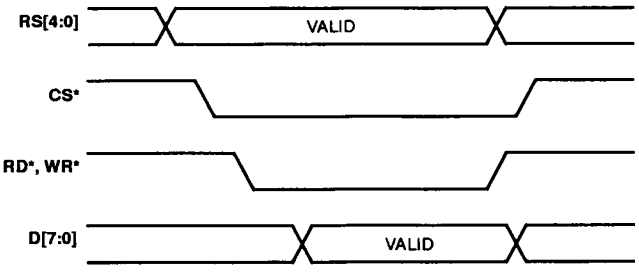


Figure 3–6. Local Hardware Interface Cycle Timing

3.2 Video Input Processing

The video frame buffer interface has a 36-bit data bus referred to as the video port. The four most-significant bits, ZC[3:0], are called the *beta field*, which is used internally by the CL-PX2080 for X-zoom operations. The remaining 32 bits of the video port, VSD[31:0], can contain up to two pixels, depending on the input format control register. The CL-PX2080 supports both tagged and untagged versions of 4:2:2 YUV, 5:5:5 RGB, and 8:8:8 RGB. The bitmapping of these formats onto VSD[31:0] is shown in Table 3–3. The processing of the incoming video stream is shown in Figure 3–8 and is detailed in the sections that follow.

3.2.1 Video Input FIFO

Video port data is clocked into the CL-PX2080 independent of the graphics data. The CL-PX2080 latches video port data on the rising edge of VCLK. When the video input FIFO (full-8) flag goes active, the fifofull is asserted internally before the next VCLK rising edge. A fifofull is asserted internally. FIFOFULL* is asserted two pclks later due to synchronizing circuitry. The video port data must be stable before and after the rising edge of VCLK. The video input FIFO is 256 double-pixels deep.

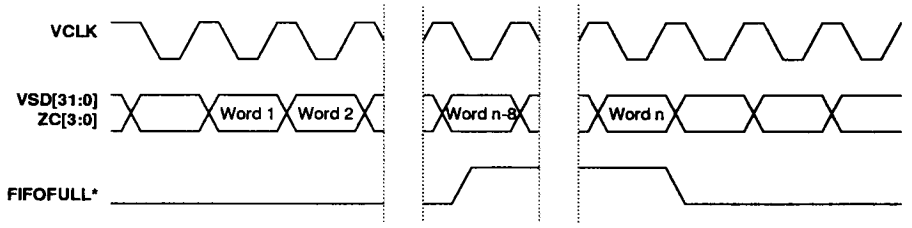


Figure 3–7. Video Input Timing

The Video Input FIFO supports:

- 24-bit RGB color data (≤ 1:1 mux) at up to 40-MHz pixel rates,
- 16-bit RGB (≤ 2:1 mux) at up to 80-MHz pixel rates, and
- 16-bit YUV (≤ 2:1 mux) at up to 80-MHz pixel rates.

The remaining video processing elements described in this section convert a variety of input formats into linear RGB:

- Format Aligner
- Chrominance Interpolator
- Zoom Control
- Color Space Converter
- Gamma Corrector.

These processing elements operate in sequence as shown in Figure 3–8. Any stage not needed for a specific application can be bypassed using internal control registers.

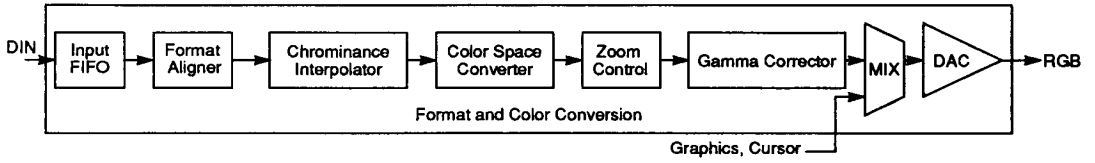


Figure 3–8. Video Input Processing Elements

All elements in the Video Pipeline are adjusted (bypassed, if necessary) automatically, depending on VFC. The exception to this is the Gamma Corrector, which can be bypassed using VFC[4].

3.2.2 Format Aligner

The Format Aligner accepts pixel input (VSD[31:0]) for various pixel input formats described in Table 3–3 and converts it to 4:4:4 format, 1 YUV, or RGB component per pixel clock. For formats requiring less than or equal to 16 bits per pixel, two pixels are packed in the 32-bit pixel word VSD[31:0]. Pipeline registers are used to reformat data before it is passed into the color conversion circuitry. The notation is based on alignment to resultant 8-bit pixel values, where Bit 7 is the MSb. For example, if Y-7, Y-6, Y-5, and Y-4 are specified, then data is left justified out of the pipeline with the 4 LSbs padded with '0's. Also, when Y0 and Y1 are specified in the same input frame, Y0 is the first luminance component in time.

Table 3–3. Supported Pixel Word Input Formats

Pixel Word VSD[31:0]	YUV 16-bit Non-Tagged	YUV 16-bit Tagged	RGB 16-bit Non-Tagged	RGB 16-bit Tagged	RGB 24-bit Non-Tagged	RGB 24-bit Tagged
VSD[31]	Y1-7	Y1-7	R1-7	TAG 1	X	TAG 0
VSD[30]	Y1-6	Y1-6	R1-6	R1-7	X	X
VSD[29]	Y1-5	Y1-5	R1-5	R1-6	X	X
VSD[28]	Y1-4	Y1-4	R1-4	R1-5	X	X
VSD[27]	Y1-3	Y1-3	R1-3	R1-4	X	X
VSD[26]	Y1-2	Y1-2	G1-7	R1-3	X	X
VSD[25]	Y1-1	Y1-1	G1-6	G1-7	X	X
VSD[24]	Y1-0	Y1-0	G1-5	G1-6	X	X
VSD[23]	V0-7	V0-7	G1-4	G1-5	R0-7	R0-7
VSD[22]	V0-6	V0-6	G1-3	G1-4	R0-6	R0-6
VSD[21]	V0-5	V0-5	G1-2	G1-3	R0-5	R0-5
VSD[20]	V0-4	V0-4	B1-7	B1-7	R0-4	R0-4
VSD[19]	V0-3	V0-3	B1-6	B1-6	R0-3	R0-3
VSD[18]	V0-2	V0-2	B1-5	B1-5	R0-2	R0-2
VSD[17]	V0-1	V0-1	B1-4	B1-4	R0-1	R0-1
VSD[16]	V0-0	TAG 1	B1-3	B1-3	R0-0	R0-0
VSD[15]	Y0-7	Y0-7	R0-7	TAG 0	G0-7	G0-7
VSD[14]	Y0-6	Y0-6	R0-6	R0-7	G0-6	G0-6
VSD[13]	Y0-5	Y0-5	R0-5	R0-6	G0-5	G0-5
VSD[12]	Y0-4	Y0-4	R0-4	R0-5	G0-4	G0-4
VSD[11]	Y0-3	Y0-3	R0-3	R0-4	G0-3	G0-3
VSD[10]	Y0-2	Y0-2	G0-7	R0-3	G0-2	G0-2

Table 3–3. Supported Pixel Word Input Formats *(cont.)*

Pixel Word VSD[31:0]	YUV 16-bit Non-Tagged	YUV 16-bit Tagged	RGB 16-bit Non-Tagged	RGB 16-bit Tagged	RGB 24-bit Non-Tagged	RGB 24-bit Tagged
VSD[9]	Y0-1	Y0-1	G0-6	G0-7	G0-1	G0-1
VSD[8]	Y0-0	Y0-0	G0-5	G0-6	G0-0	G0-0
VSD[7]	U0-7	U0-7	G0-4	G0-5	B0-7	B0-7
VSD[6]	U0-6	U0-6	G0-3	G0-4	B0-6	B0-6
VSD[5]	U0-5	U0-5	G1-2	G0-3	B0-5	B0-5
VSD[4]	U0-4	U0-4	B1-7	B0-7	B0-4	B0-4
VSD[3]	U0-3	U0-3	B1-6	B0-6	B0-3	B0-3
VSD[2]	U0-2	U0-2	B1-5	B0-5	B0-2	B0-2
VSD[1]	U0-1	U0-1	B1-4	B0-4	B0-1	B0-1
VSD[0]	U0-0	TAG 0	B1-3	B0-3	B0-0	B0-0

3.2.2.1 RGB Video Input Data

For RGB video input data, the Format Aligner can be programmed to accept either:

- 5-6-5, 5-5-5-TAG, 8-8-8, or 8-8-8-TAG formats, where n-n-n indicates the bits allocated to the red, green, and blue planes respectively, or
- pseudocolor, where the most-significant input byte is passed to the red, green and blue outputs.

Unused bit locations should be grounded prior to FIFO input. For RGB data, the input simply passes to the output in proper bit alignment.

3.2.2.2 YUV 4:2:2 Video Input Data

For 4:2:2 YUV video input data, the Format Aligner can be programmed to simultaneously accept two pixels of data in CCIR 601 format. The Format Aligner video input formats are shown on Table 3–3. An optional input TAG may be used in place of the LSb of the chrominance values. Note that the chrominance values align with the odd luminance values. For 4:2:2 YUV data, the Format Aligner simply passes input data (as shown in Table 3–4) to the Chrominance Interpolator.

Table 3–4. YUV 4:2:2 Format

Luminance Values

Y Frame	1	2	3	4	5	6	7	8
Y7	Y07	Y17	Y07	Y17	Y07	Y17	Y07	Y17
Y6	Y06	Y16	Y06	Y16	Y06	Y16	Y06	Y16
Y5	Y05	Y15	Y05	Y15	Y05	Y15	Y05	Y15
Y4	Y04	Y14	Y04	Y14	Y04	Y14	Y04	Y14
Y3	Y03	Y13	Y03	Y13	Y03	Y13	Y03	Y13
Y2	Y02	Y12	Y02	Y12	Y02	Y12	Y02	Y12
Y1	Y01	Y11	Y01	Y11	Y01	Y11	Y01	Y11
Y0	Y00	Y10	Y00	Y10	Y00	Y10	Y00	Y10

Chrominance Values

UV Frame	1		2		3		4	
UV7	U7	V7	U7	V7	U7	V7	U7	V7
UV6	U6	V6	U6	V6	U6	V6	U6	V6
UV5	U5	V5	U5	V5	U5	V5	U5	V5
UV4	U4	V4	U4	V4	U4	V4	U4	V4
UV3	U3	V3	U3	V3	U3	V3	U3	V3
UV2	U2	V2	U2	V2	U2	V2	U2	V2
UV1	U1	V1	U1	V1	U1	V1	U1	V1
UV0	U0	V0	U0	V0	U0	V0	U0	V0

3.2.2.3 Chrominance Interpolator

The Chrominance Interpolator increases the sampling rate of the color difference signals when they are input at a rate less than 4:4:4, and it acts as a data source for the Color Space Matrix. The Chrominance Interpolator always operates in the same mode as the Format Aligner.

The Chrominance Interpolator contains two identical circuits — one for the U component and one for the V component. The output of the Time Demultiplexer feeds the Chrominance Interpolator input, setting the missing U and V values to '0' on display window boundary conditions.

3.2.2.4 Color Space Converter

The Color Space Converter is enabled automatically when it is necessary to convert the video data to the RGB format that is passed to the DAC.

3.2.2.5 RGB Video Input Data

The Chrominance Interpolator is not required when using RGB video input data.

3.2.3 Zoom Control Codes

The Zoom Control circuitry accepts input from the Color Space Matrix and outputs to the Gamma Corrector. A 4-bit zoom code accompanies each pixel pair to specify the output sequence in the CL-PX2080 (when used with CL-PX2070).

3.2.4 Gamma Correction

The Gamma Corrector accepts input from the Zoom Control circuitry and outputs video data to the mixing circuitry for alignment with incoming graphics, cursor, and background border. The Gamma Corrector can be programmed either with a custom correction table or to remove the gamma coding that is normally present in a YUV television signal.

The Gamma Corrector comprises three 256 x 8 memories, one for each color channel. The transfer function is user-definable and programmable. The Gamma Corrector is an optional feature; the user can bypass it by setting Bit 4 in VFC Register to a '1'.

3.3 Graphics Frame Buffer Interface and Processing

The CL-PX2080 accepts data from the graphics display source through either of two paths — an 8-bit VGA data path (VGA[7:0]) or a 32-bit VRAM serial data path (GSD[31:0]). One data path is selected at a time. The GPS Pin and Bits 6 and 5 in the CSC Register determine which input is selected. These two paths are provided to allow next-generation PC graphics subsystems based on the CL-PX2080 to maintain compatibility with the large installed base of VGA systems while achieving higher performance and higher resolution via the VRAM serial data path.

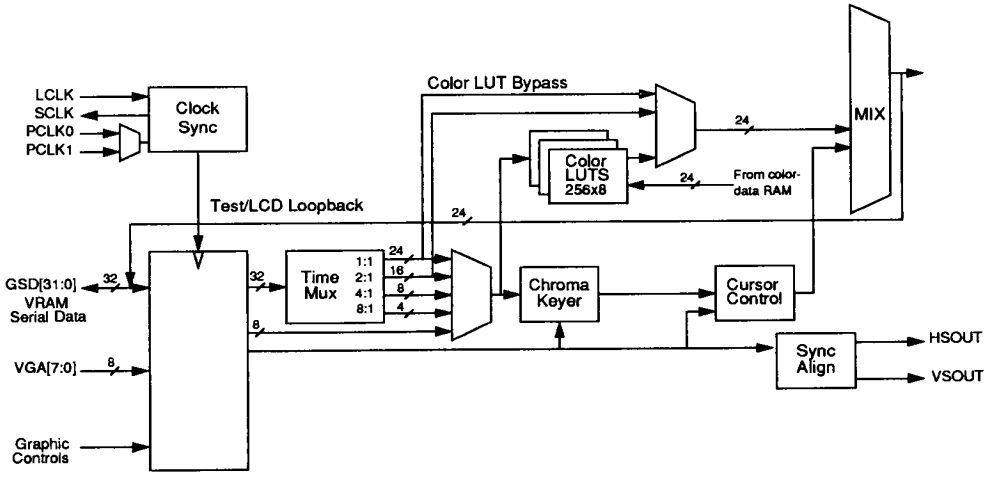


Figure 3–9. CL-PX2080 Graphics Datapath

3.3.1 VRAM Support

The graphics serial bus interface has a 32-bit data bus. The data on this bus is multiplexed under control of the Graphics Format Control Register (GFC) and is latched internally on the rising edge of LCLK. LCLK must be supplied by the graphics controller and should be derived from SCLK. SCLK is derived from PCLK according to the state of Bit 2 of the GFC Register. The maximum transfer rate on this bus is 40 MHz (32-bit words per second).

3.3.2 VRAM Operation

3.3.2.1 Graphics Data — GSD[31:0]

The VRAM shift clock (SCLK) is generated by the CL-PX2080. In 1:1/VGA Mode, SCLK equals LCLK. Table 3–5 describes the relationship of SCLK and LCLK in various pixel modes.

Table 3–5. SCLK and LCLK Relationships

Multiplex Ratio	SCLK/LCLK Relationship
8:1	SCLK = LCLK = PCLK x 8
4:1	SCLK = LCLK = PCLK x 4
2:1	SCLK = LCLK = PCLK x 2
1:1	SCLK = LCLK = PCLK

GSD[31:0] is the input pixel data, 8 bits per pixel (4:1 MUX) and 4 bits per pixel (8:1 MUX) for four and eight horizontally consecutive output pixels. GSD[31:0] is always latched on the rising edge of LCLK.

The pixel clock is specified to be either PCLK0 or PCLK1 by Bit 4 of the CSC Register.

3.3.2.2 GSD[31:0] Mapping to Pixel Port Interface

Regardless of mode, the least-significant word, byte, or nibble is the first to be displayed in time. For example, when in 4:1 Mode, there are four 8-bit pixel ports encoded within GSD[31:0]. Port GSD[7:0] corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by GSD[15:8], then GSD[23:16], and finally GSD[31:24], repeating the pattern from LSB to MSB until the first scanline is completely displayed.

3.3.2.3 Odd/Even Field Definition

The output data sequence depends on Bit 3, DM of the CSC Register and the ODD/EVEN* input. For graphics data processing, the CL-PX2080 treats interlaced graphics data in the same manner as non-interlaced data, merely transferring it for output processing. Interlaced data alignment is performed and controlled outside the CL-PX2080. Cursor pattern RAM data, however, is managed by the CL-PX2080 in Interlaced Mode.

In Interlaced Mode, Scanline 1 is always displayed first and is considered the first line of the even field. In Non-interlaced Mode, Scanline 2 immediately follows Scanline 1. In Interlaced Mode, Scanline 2 is considered to be the first line of the odd field and is displayed only after the entire even field has been displayed and the ODD/EVEN* pin has toggled.

Only the odd lines or only the even lines will be displayed if ODD/EVEN* does not change. Figure 3–10 shows the interlaced and non-interlaced display scan. Non-interlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

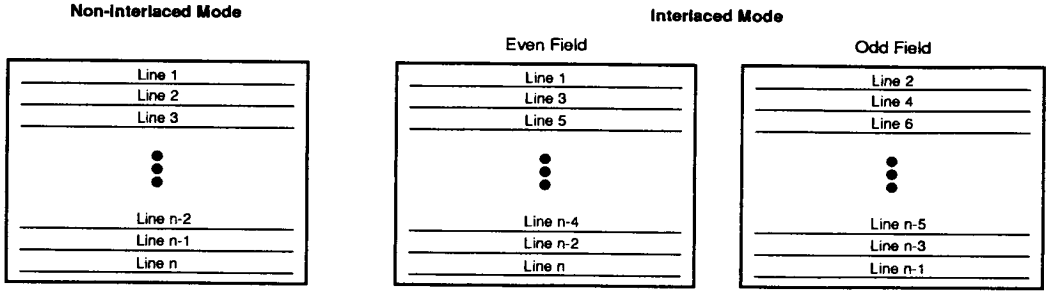


Figure 3–10. Interlaced and Non-Interlaced Display Scans

3.3.2.4 Pixel Read Mask Register

Each pixel clock cycle, GSD[31:0] pixel data is AND'ed with the contents of the pixel read mask register LPM, and the result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation except when the true-color bypass is enabled.

3.3.3 VRAM Port Modes of Operation

The 32-bit VRAM port can be used as a varying number of parallel pixel ports, depending on the number of bits defined for each pixel. The following sections describe the four possible combinations. In all cases, pixel data is latched on the rising edge of LCLK, and the least-significant pixel is output first.

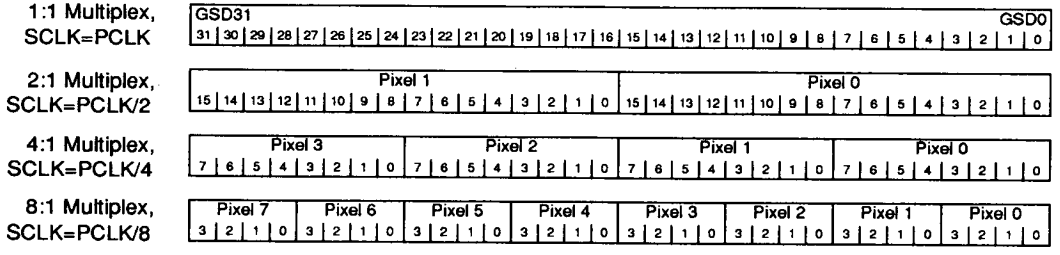


Figure 3–11. Pixel Mapping with Graphics Port

Table 3–6. Pixel Index Mapping — Pixel Mask vs. VGA[7:0] and GSD[31:0] Bit Locations

Register/Format Type Description	MSb							LSb	Function
Pixel Mask Register	7	6	5	4	3	2	1	0	Register Bits
VGA Data	7	6	5	4	3	2	1	0	Palette Index
4 Bits/Pixel	x	x	x	x	3	2	1	0	Palette Index
8 Bits/Pixel	7	6	5	4	3	2	1	0	Palette Index
16 Bits/Pixel	14	13	12	11	10	x	x	x	Red Palette Index
5:5:5 Format	9	8	7	6	5	x	x	x	Green Palette Index
Sparse	4	3	2	1	0	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	14	13	12	11	10	Red Palette Index
5:5:5 Format	x	x	x	9	8	7	6	5	Green Palette Index
Contiguous	x	x	x	4	3	2	1	0	Blue Palette Index
16 Bits/Pixel	15	14	13	12	11	x	x	x	Red Palette Index
5:6:5 Format	10	9	8	7	6	5	x	x	Green Palette Index
Sparse	4	3	2	1	0	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	15	14	13	12	11	Red Palette Index
5:6:5 Format	x	x	10	9	8	7	6	5	Green Palette Index
Contiguous	x	x	x	4	3	2	1	0	Blue Palette Index
24 Bits/Pixel	23	22	21	20	19	18	17	16	Red Palette Index
8:8:8 Format	15	14	13	12	11	10	9	8	Green Palette Index
	7	6	5	4	3	2	1	0	Blue Palette Index

3.3.3.1 16-Bits/Pixel Operation (1:1 Mux)

The 1:1 Multiplexing Mode is selected through Bit 2, MR of the GFC Register. In this mode, two independent 16-bit pixel ports, GSD[31:16] and GSD[15:0], are latched on the rising edge of LCLK, and are multiplexed 1:1. Bit 0, PS of the GFC Register, selects between the two ports. One LCLK rising edge occurs every PCLK cycle. SCLK is equal to the current PCLK selected.

GSD[31] switches between the two ports on a pixel-by-pixel basis when 5:5:5 RGB color format (Bit 3, CF of the GFC Register) and real-time pixel port switching is enabled (Bit 1, TE of the GFC Register). If GPS is '0', the VGA port is multiplexed regardless of the state of GSD[31]. GSD[15] is ignored internally when in 5:5:5 Mode. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

3.3.3.2 True Color Operation

Bit 4, TC in the GFC Register, enables or disables the true-color palette bypass feature. When Bypass Mode is selected, the pixel data are transferred directly to the proper bytes of the respective DACs bypassing the palette and the pixel mask. When the bypass mode is not selected, the pixel data index the proper locations in the palette, and the correct color information is passed to the respective DACs. Bit 1, PM of the CSC Register, selects sparse or contiguous palette mapping.

For sparse palette mapping, each independent color component of pixel data is mapped to the most-significant bits of the respective palette address; the least-significant bits are set to '0'. For contiguous palette mapping, each independent color component of the pixel data is mapped to the least-significant bits of the respective palette address; the most-significant bits are set to '0'. For either sparse or contiguous mapping, the specified color palette values are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32K or 64K simultaneous colors respectively. The DACs can be configured for 6 or 8 bits of resolution in this mode.

Table 3–7. Color Mapping to GSD[31:0] Bus

Format	MSb S	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	LSb B0
5:5:5 Mode																
Port 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port 2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Format	MSb R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	LSb B0
5:6:5 Mode																
Port 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port 2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Table 3–8. Graphics Port Operating Mode

	Pin GPS*	GFC Bit1 TE	GFC Bit0 PS	Pin GSD [31]	GFC Bit2 MR	GFC Bit3 CF	GFC Bit6 GPF1	GFC Bit5 GPf0	Ports/Mux Order	Mux Rate
VGA	0	x	x	x	x	x	0	0	VGA[7:0]	1:1
4 Bits/Pixel	x	x	x	Data	x	x	1	1	GSD[3:0] GSD[7:4] GSD[11:8] GSD[15:12] GSD[19:16] GSD[23:20] GSD[27:24] GSD[31:28]	8:1
8 Bits/Pixel	x	x	x	Data	x	x	1	0	GSD[7:0] GSD[15:8] GSD[23:16] GSD[31:24]	4:1
16 Bits/Pixel(5:5:5)	x	x	x	x	0	0	0	1	GSD[15:0] GSD[31:16]	2:1
16 Bits/Pixel(5:6:5)	x	x	x	Data	0	1	0	1	GSD[15:0] GSD[31:16]	2:1
16 Bits/Pixel(5:5:5)	1	0	0	x	1	0	0	1	GSD[15:0]	1:1
16 Bits/Pixel(5:5:5)	1	0	1	x	1	0	0	1	GSD[31:16]	1:1
16 Bits/Pixel(5:5:5)	1	1	x	0	1	0	0	1	GSD[15:0]	1:1

3.3.4 VGA Support

The VGA[7:0] data path is an 8-bit input bus multiplexed with the VRAM serial data path under control of CSC (6,5). The maximum transfer rate is 65 MHz (65 Mbytes per second).

3.3.4.1 VGA-Compatible Modes

The CL-PX2080 has the flexibility to operate in a system with a separate VGA controller/DAC or to operate as the sole display output. Many currently used VGA/DAC ICs internally decode the ISA-standard addresses for the palette RAM. The CL-PX2080 is capable of transparently replacing an existing DAC, operating in parallel, or operating as a separate subsystem at a unique address. Three access modes are available to maintain compatibility with software designed for VGA Registers.

Mode 0 is for a system with a separate, pre-existing VGA controller and palette DAC. Graphic data from the auxiliary (or 'feature') connector of the existing controller board enters the VGA graphics port of the CL-PX2080 where it is mixed with video data from an external source.

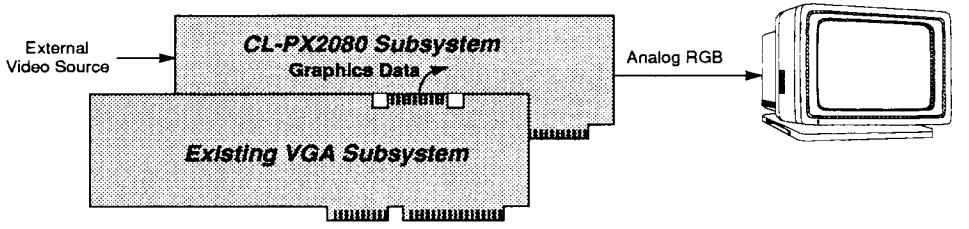


Figure 3–12. Mode 0 System Configuration

As shown in Figure 3–12, a single external monitor is connected to the analog-RGB output of the CL-PX2080. To preserve the same functionality with all VGA software drivers, the CL-PX2080 must accept writes to the standard VGA palette addresses but *not* respond to reads, allowing the existing VGA controller board to respond. The CL-PX2080 palette RAM shadows the VGA controller RAM on writes only. Mode 0 is also useful in designs configured like that shown in Figure 3–12, when the CL-PX2080 is used with a self-decoding VGA controller.

Mode 1 is designed for a system that has a VGA controller/palette DAC and a CL-PX2080 in the same subsystem. Graphic data from the auxiliary (or 'feature') connector of the existing controller board enters the VGA graphics port of the CL-PX2080 where it is mixed with video data from an external source as shown in Figure 3–13.

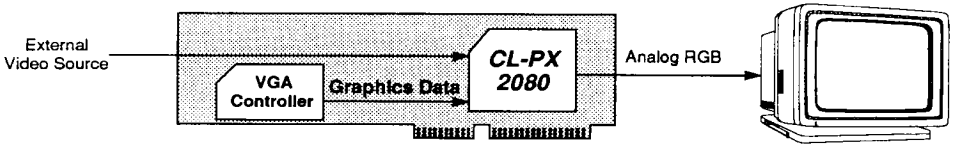


Figure 3–13. Mode 1 System Configuration

The difference between Modes 0 and 1 is that Mode 1 responds to reads at the palette RAM address. This system is compatible with existing software that manipulates the VGA palette RAM.

Mode 2 is designed for a system containing a VGA controller (with palette DAC) and a CL-PX2080 subsystem, each driving separate RGB monitors as shown in Figure 3–14. In this scenario the VGA subsystem occupies the standard VGA palette RAM addresses and the CL-PX2080 registers respond to a completely separate set of addresses.

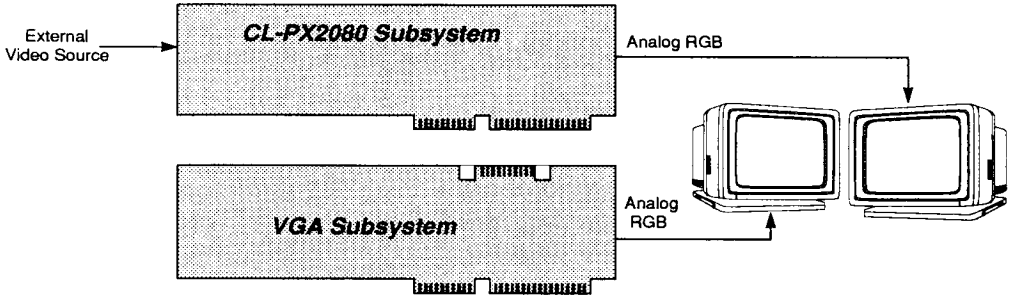


Figure 3–14. Mode 2 System Configuration

Modes are selected by the IE, RE, and RO Bits in the BIR Register as described in Section 4.1.1 on page 55.

3.3.4.2 Using the VGA Port In Extended Color Modes

In the Extended Color (EC) Modes the CL-PX2080 VGA port accepts 16-bit data, as illustrated in Figure 3–15. Extended color modes include compatibility with HiCOLOR™ modes used in some devices. An extended color mode is selected by entering the appropriate code in the VFC Register, as described in Section 4.7.3 on page 73.

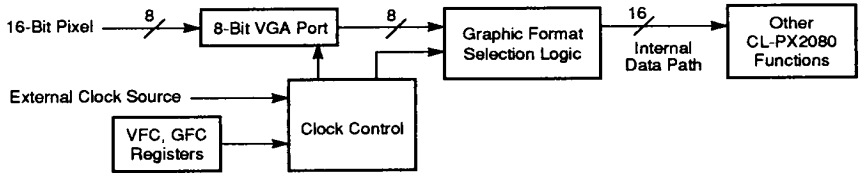


Figure 3–15. Accepting 16-Bit Color Data Through The 8-bit VGA Port

In True-color Mode, the color look-up table and read-mask circuitry are bypassed, allowing the display of a maximum of 64K colors.

Color-Data Clocking in EC Mode

In EC Mode, two bytes are transferred each LCLK cycle. Data is transferred LSB first. The most-significant byte is sampled on the falling edge, and the least-significant byte is sampled on the rising edge as shown in Figure 3–16.

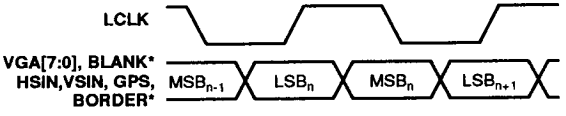


Figure 3–16. EC Mode 1 Timing

3.3.5 Hardware Cursor Operation

The CL-PX2080 has an on-chip, three-color, user-definable cursor, which is implemented in 32 x 32 x 2-bit memory. This cursor works in both interlaced and non-interlaced systems. The cursor can be programmed via the CSC Register for three modes of operation summarized in Table 3–9:

Table 3–9. Cursor 2-Bit Data Decode vs. Mode Selected

Bit 1	Bit 0	Mode 1	Mode 2	Mode 3
0	0	Data	CC1	Data
0	1	CC1	CC2	Data
1	0	CC2	Color, Gamma Data	CC1
1	1	CC3	Inverse Data	CC2

CCn = Cursor Color Register n

The pattern for the cursor is provided by the cursor RAM, which can be accessed by the BIU at any time. Cursor positioning is performed in the Cursor-position Registers (CXH, CXL, CYH, CYL). Figure 3–17 demonstrates its use.

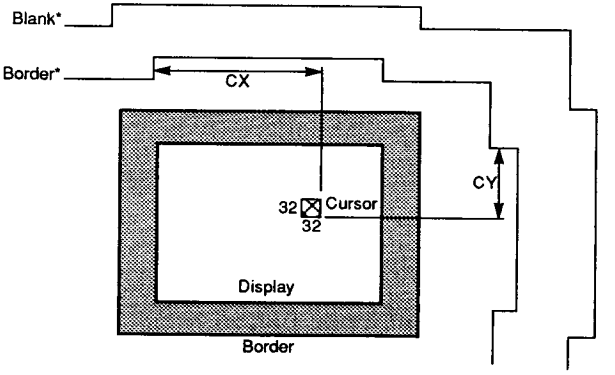


Figure 3–17. Cursor Operation

A value of (0,0) written to the Cursor-position Registers places the cursor completely off-screen, outside the viewing area. A cursor-position value of (1,1) places the lower-right pixel of the cursor on the upper left-hand corner of the screen. Only one cursor pattern per frame is displayed, regardless of updates to the Cursor-position Registers. The single restriction on position-register updates is that all position registers must be written when the cursor location is updated.

The Internal Position Register is updated when the Y upper byte (CYH) is written to ensure this operation. The cursor pattern is displayed at the last cursor location written prior to frame start. The reference point of the cursor, Row 0 Column 0, is the lower-right corner of the cursor relative to BORDER*.

The position of the cursor is not dependent upon CBLANK*. The cursor X position is relative to the first rising edge of LCLK when BORDER* is sampled at a logical '1'. The cursor Y position is relative to the first rising edge of LCLK when BORDER* is sampled at a logical '1' after the vertical blanking period has been determined.

The cursor pattern can be displayed in an interlaced system if Bit 3, DM of the CSC Register, is a logical '1'. The first cursor line displayed (Row 31 of cursor pattern RAM) depends on the state of the O/E* Pin and the position value in CYH, CYL. If the Y position is an even number, the data in Row 31 is displayed during the even field, starting at position (CX-31, CY-31), where CX is the concatenated position determined by CXH, CXL (and similarly with Y). Each subsequent scanline displayed in the even field corresponds to every alternate active cursor line after Row 31 in the cursor RAM array. During odd fields, the even rows from the cursor pattern RAM are displayed starting with Row 30 at position (CX-31, CY-30). Each subsequent scanline displayed in the odd field corresponds to every alternate active cursor line after Row 30 in the cursor RAM array.

Similarly, if the Y position value was an odd number in the first line displayed, then Row 31 and subsequent odd rows would be displayed during an odd field. Row 30 data and subsequent even rows would be displayed during the even field.

3.3.6 Internal Memory Access

Table 3–10. CL-PX2080 Register Map

Reg.	Addresses Local	Prim.	Sec.	Blk	Bit Assignments Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Memory Access Addressing and Indexing												
BIR	N/A	0x27CE	0x29E	N/A	IE	RE	SE	RO	RSVD	BLK		
Graphics Color Palette Registers (VGA Mode 0 and 1)												
LAW	0x00	0x03C8	N/A	N/A	Color LUT Write Address							
LCD	0x01	0x03C9	N/A	N/A	Color LUT Data							
LPM	0x02	0x03C6	N/A	N/A	Color LUT Pixel Mask Data							
LAR	0x03	0x03C7	N/A	N/A	Color LUT Read Address							
Graphics Color Palette Register (VGA Mode 2)												
LAW	0x00	0x27CC	0x029C	0	Color LUT Write Address							
LCD	0x01	0x27CD	0x029D	0	Color LUT Data							
LPM	0x02	0x27CA	0x029A	0	Color LUT Pixel Mask Data							
LAR	0x03	0x27CB	0x029B	0	Color LUT Read Address							
Cursor Color and Analog Setup Registers												
CAW	0x04	0x27CC	0x029C	1	RSVD						Cursor Wr Adr	
CCD	0x05	0x27CD	0x029D	1	Color Data							
ASC	0x06	0x27CA	0x029A	1	RSVD	COFF	RSVD				D24	DOFF
CAR	0x07	0x27CB	0x029B	1	RSVD						Cursor Rd Adr	
Graphic and Cursor Setup Registers												
GFC	0x08	0x27CC	0x029C	2	RSVD	GPF		TC	CF	MR	TE	PS
CSC	0x09	0x27CD	0x029D	2	SD	GPS		CS	DM	PM	CMS	
GSR	0x0A	0x27CA	0x029A	2	REV				S	IO	CP	
CPR	0x0B	0x27CB	0x029B	2	Cursor Pattern RAM Data							

Table 3–10. CL-PX2080 Register Map *(cont.)*

Reg.	Addresses Local	Prim.	Sec.	Blk	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Cursor Positioning Registers												
CXL	0x0C	0x27CC	0x029C	3	Cursor X Position Low Byte							
CXH	0x0D	0x27CD	0x029D	3	RSVD				Cur X Pos H Nibble			
CYL	0x0E	0x27CA	0x029A	3	Cursor Y Position Low Byte							
CYH	0x0F	0x27CB	0x029B	3	RSVD				Cur Y Pos H Nibble			
Video, Graphics and Sync Control Registers												
VFC	0x10	0x27CC	0x029C	4	EC	CS	RSVD	GBYP	CSF			
GOC	0x11	0x27CD	0x029D	4	T (Transparency)							
SAR	0x12	0x27CA	0x029A	4	HP	HL	VP	VL	DIR	DLY		
RSV1	0x13	0x27CB	0x029B	4	GT	CT	LC	PO	SO	WO	KO	BE
Video Gamma Correction Palette Registers												
VGW	0x14	0x27CC	0x029C	5	Video Gamma Correction Write Address							
VGD	0x15	0x27CD	0x029D	5	Video Gamma Correction Data							
RSV2	0x16	0x27CA	0x029A	5	RSVD							
VGR	0x17	0x27CB	0x029B	5	Video Gamma Correction Read Address							
Graphics Chroma Key Registers												
GCKR	0x18	0x27CC	0x029C	6	Graphics Chroma Key Red Data							
GCKG	0x19	0x27CD	0x029D	6	Graphics Chroma Key Green Data							
GCKB	0x1A	0x27CA	0x029A	6	Graphics Chroma Key Blue Data							
RSV3	0x1B	0x27CB	0x029B	6	RSVD							
GKMR	0x1C	0x27CC	0x029C	7	Graphics Chroma Key Mask Red Data							
GKMG	0x1D	0x27CD	0x029D	7	Graphics Chroma Key Mask GreenData							
GKMB	0x1E	0x27CA	0x029A	7	Graphics Chroma Key Mask Blue Data							
Rsv4	0x1F	0x27CB	0x029B	7	RSVD							

3.3.6.1 Color RAM Data Access

Color-palette, gamma-palette, cursor, and cursor-border colors are specified in terms of 24-bit RGB data, one byte per color. The host processor accesses a color memory location by first writing the index address, then performing three successive writes or reads to the data register. Upon completion of the third access, the index register points to the next location. The two internal bits used for this function are reset to '0' upon a write to the address register, but they are unaffected by a read.

For example, to update the color palette data, the processor writes the CL-PX2080 address register (RAM write mode) with the address of the color palette RAM location to be modified. The processor performs three successive write cycles (8 bits each of red, green, and blue). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the processor can modify by simply writing another sequence of red, green, and blue data. To write to a block of color values in consecutive locations, write the start address and perform continuous R, G, B write cycles until the entire block has been written. Cursor and other color information is handled the same way. Refer to appropriate Bus Interface Unit configuration for read/write timing.

When accessing the color palette RAM, the address register resets to '00h' following a blue read or write to RAM location FFh.

The processor interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R,G, and B in the block diagram) are synchronized by internal logic; the transfers occur in the period between processor accesses. To reduce noticeable sparkling on the CRT screen during processor access to the color palette RAM, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB Registers and Look-Up Table RAMs occurs.

3.3.6.2 Accessing the Cursor RAM Array

The 32 x 32 x 2 cursor RAM is accessed in a planar format where Plane 1 is Bit 1 of the cursor data and Plane 0 is Bit 0. In the planar format, only seven address bits are used. The eighth bit determines which Plane (0 or 1) data of the cursor RAM array is accessed (see Figure 3–18). A single address presented to the cursor RAM accesses 8-bit locations in Plane 0 or 1, depending on the state of address Bit 7.

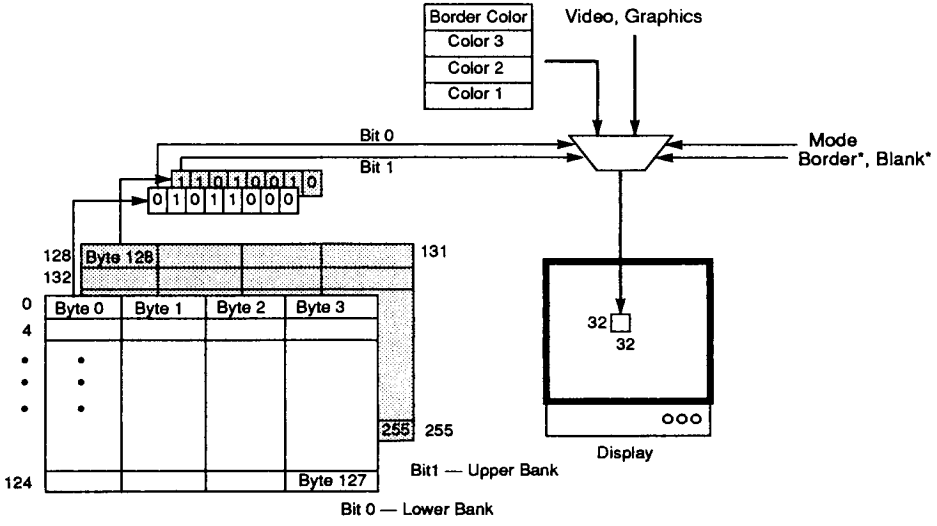


Figure 3–18. Cursor RAM Function Diagram

After each access in the planar format, the address increments. The processor uses LAW or LAR (write or read) binary address counters to access the cursor RAM array (see Table 3–11). Note that LAW (LAR) is the same binary counter used for RGB auto-incrementing access to the color palette RAM. Any write to LAW after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has been accessed again. Cursor auto-incrementing then begins from the address written. A read from the LAR does not reset the cursor auto-incrementing logic. The color palette RAM and the cursor RAM share the same internal address registers, and processor addressing for this and all other registers is determined by the appropriate register addresses documented in Section 4.

Table 3–11. Cursor Memory Mapping and Relationships for Display

Bit 1	Bit 0	Mode 1	Mode 2	Mode 3
0	0	Data	CC1	Data
0	1	CC1	CC2	Data
1	0	CC2	Data	CC1
1	1	CC3	Not Data	CC2

NOTE: CCn = Cursor Color Register n
Data = Color or Gamma Palette Data
Not = Inverse of

3.3.6.3 6-Bit/8-Bit Operation

Bit 1, D24/16 of the ASC Register, specifies whether the processor is reading and writing eight bits or six bits of color information each cycle.

For 8-bit operation, D0 is the LSb and D7 is the MSb of color data.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSb and D5 being the MSb of the color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are a logical '0'. Accessing the cursor RAM array does not depend on the resolution of the DACs.

Note that in the 6-bit Mode, the CL-PX2080 full-scale output current will be less than when it is in the 8-bit Mode since the two LSbs of each 8-bit DAC are always a logical '0' in the 6-bit Mode.

3.3.7 Mixing to Output DAC

The Output DAC contains three 85-MHz 8-bit digital-to-analog converters. The table below shows how the graphic data path is controlled at the input of the DAC by BORDER*, CBLANK*, and GPS.

Table 3–12. DAC Data Source Control

CBLANK*	BORDER*	GPS	
0	X	X	Video Blanking
1	0	X	Border Color
1	1	0	VGA or Cursor Color
1	1	1	GSD or Cursor Color

The GPS Pin is an input used to select between the VGA and VRAM graphics ports for graphics data input. CBLANK* and BORDER* both prevent graphics and video data from being presented to the DAC. If the GPS Pin is not used, it should be tied to the appropriate logical value for the graphics port selected.

3.3.7.1 Graphics Overlay Control

The graphics overlay controls consist of a 32-bit color key, a 32-bit color key mask, an 8-bit overlay op-code, and an 8:1 multiplexer.

To understand how the graphics overlay controls work, imagine the CL-PX2080 as managing two images, one in front of the other. The two image planes are the video and graphics images, with the video image behind the graphics image. Every graphics pixel is either transparent or opaque. If the graphics pixel is opaque, the graphics color information for that pixel is displayed on the screen. If the graphics pixel is transparent, the color information of the video pixel behind it is displayed on the screen.

The graphics overlay controls determine which graphics pixels are transparent. The determination is made by a combination of two overlay control features — a TAG bit component in the video pixel data and the graphics COLOR key switch. The graphics COLOR key switch is generated by AND'ing the graphics pixel data with the GKM Register and then comparing the results against the GCK Register.

The tag bit is generated outside the CL-PX2080 and switches the multiplexer. The Graphics Overlay Op-Code (GOC) Register is input to the multiplexer.

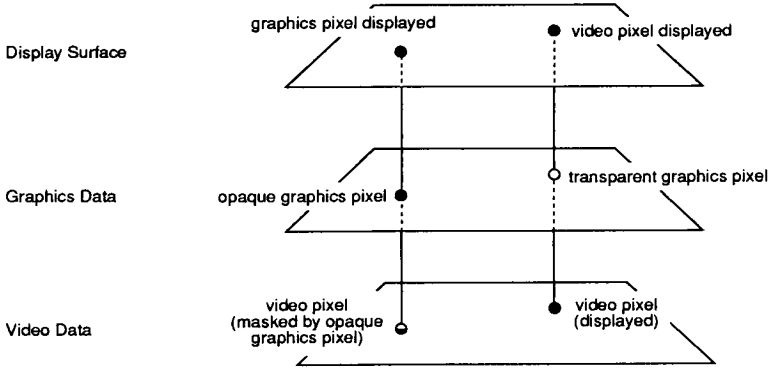


Figure 3–19. Graphics Overlay Operation

3.3.7.2 Graphics Overlay OpCode Register (GOC)

The Graphics Overlay OpCode is an 8-bit value used as input to an 8:1 multiplexer. The select signals to the multiplexer (the TAG bit and the graphics COLOR key match) determine which of the eight bits will become the transparency control for each pixel time. If a bit in the GOC Register is '1', the graphics pixel becomes transparent, enabling the video pixel for final display. The GOC Register is initialized to '0x00' during reset, selecting the graphics path and ignoring the video input stream.

3.3.8 CLK Synchronizer and SYNC Alignment

The clock generator creates all device clocks. The rising edge of LCLK latches GSD[31:0] or VGA[7:0], and CBLANK*, HSIN, VSIN, GPS, and BORDER*. The information latched by this signal is synchronized

internally with SCLK. To avoid metastability, LCLK must maintain setup and hold requirements to SCLK. Data is synchronized with the selected pixel clock (PCLK0 or PCLK1) after being internally latched with SCLK. When the input data multiplexing rate is 8:1, 4:1, 2:1, or 1:1, LCLK must be the pixel clock divided by 8, 4, 2, or 1, respectively.

The SYNC alignment circuitry generates external HSOUT and VSOUT Signals required for the monitor. The output is delayed to match the internal PCLKn delay of the RGB outputs. A sync alignment register is provided to program polarities of HSIN, HSOUT, VSIN, and VSOUT. This register also generates a programmable PCLKn delay of RGB relative to the matched HSOUT and VSOUT, as described above. This delay is programmable in both directions.

3.3.9 DAC 18-Bit Mode

The D24 Bit in the ASC Register limits the resolution of the output DACs to 18 bits. This results in a slight reduction in power consumption and provides software compatibility with many popular palette DACs.

3.3.10 Power-Down Mode

The CL-PX2080 incorporates a Power-down Mode controlled by Bits 6 and 0 of the ASC Register. While Bit 6 (COFF) and Bit 0 (DOFF) are logical '0's, the CL-PX2080 functions normally.

While Bit 6 (COFF) is a logical '0', all clock inputs, PCLKn, VCLK and LCLK, are disabled.

While Bit 0 (DOFF) is a logical '0', the DACs and power to the RAM are turned off.

Note that the RAM still retains the data. Also, the RAM can be read or written to by the processor as long as the pixel clock is running. The RAM automatically powers-up during processor read/write cycles and shuts-down when the processor access is completed. The DACs output no current, and the three command registers can still be written to or read by the processor.

Note that the output DACs require about 1 second to turn off (Sleep Mode) or turn on (normal), depending on the compensation capacitor used.

The DACs will be turned off during Sleep Mode only if a voltage reference (internal or external) is used.

External circuitry should turn off the current reference (IREF is '0') to further reduce power consumption due to biasing of portions of the internal current reference.

4. REGISTERS

Internal registers control the operations of the CL-PX2080. These registers are organized in mapping order in Table 4–1. The following sections detail the CL-PX2080 registers and organize them according to the following functions:

- Indexing
- CLUT Access
- Cursor Access
- Video, Graphics, and Cursor Control
- Video Gamma Correction Palette Access
- Graphics Overlay Control
- Cursor Positioning
- Digital-to-Analog Conversion and Controls.

NOTE: Data values reserved register locations are not guaranteed on readback. Reserved bits in used register locations are read back as '0'.

Table 4–1. CL-PX2080 Control Registers (Organized by Mapping)

NOTES: 1) RS[4:0] is direct addressing in Local Hardware Interface Mode. I/O address and BIR (Base Index Register) apply to ISA and MCA Modes.

2) The ALT Pin determines whether the primary or secondary PC address is used for the BIR Register only (Low is '0', High is '1'). For all other registers, the address range is controlled by the SE Bit (Bit 5) of the BIR Register.

Register	RS[4:0]	Pri. I/O Addr.	Sec. Addr.	BIR	Definition	Ref. Section
BIR	N/A	0x27CE	0x029E	N/A	Block Index Register	4.1.1, p. 55
LAW	0x00	0x03C8	N/A	N/A	CLUT Write Address	4.2.1, p. 56
LCD	0x01	0x03C9	N/A	N/A	CLUT Color Data	4.2.2, p. 57
LPM	0x02	0x03C6	N/A	N/A	CLUT Pixel Mask	4.2.3, p. 58
LAR	0x03	0x03C7	N/A	N/A	CLUT Read Address	4.2.4, p. 59
CAW	0x04	0x27CC	0x029C	1	Cursor Address Write	4.3.1, p. 60
CCD	0x05	0x27CD	0x029D	1	Cursor Color Data Registers	4.3.2, p. 60
ASC	0x06	0x27CA	0x029A	1	Analog Setup Control	4.8.1, p. 75
CAR	0x07	0x27CB	0x029B	1	Cursor Address Read	4.3.3, p. 61
GFC	0x08	0x27CC	0x029C	2	Graphics Format Control	4.4.2, p. 63
CSC	0x09	0x27CD	0x029D	2	Cursor Setup Control	4.4.3, p. 64
GSR	0x0A	0x27CA	0x029A	2	Graphics Status Register	4.4.1, p. 62
CPR	0x0B	0x27CB	0x029B	2	Cursor Pattern RAM	4.3.4, p. 61

Table 4–1. CL-PX2080 Control Registers (Organized by Mapping) *(cont.)*

NOTES: 1) RS[4:0] is direct addressing in Local Hardware Interface Mode. I/O address and BIR (Base Index Register) apply to ISA and MCA Modes.

2) The ALT Pin determines whether the primary or secondary PC address is used for the BIR Register only (Low is '0', High is '1'). For all other registers, the address range is controlled by the SE Bit (Bit 5) of the BIR Register.

Register	RS[4:0]	Prl. I/O Addr.	Sec. Addr.	BIR	Definition	Ref. Section
CXL	0x0C	0x27CC	0x029C	3	Cursor X Position, Low Byte	4.7.1, p. 71
CXH	0x0D	0x27CD	0x029D	3	Cursor X Position, High Byte	4.7.1, p. 71
CYL	0x0E	0x27CA	0x029A	3	Cursor Y Position, Low Byte	4.7.2, p. 72
CYH	0x0F	0x27CB	0x029B	3	Cursor Y Position, High Byte	4.7.2, p. 72
VFC	0x10	0x27CC	0x029C	4	Video Format Control	4.7.3, p. 73
GOC	0x11	0x27CD	0x029D	4	Graphics Overlay Opcode	4.6.1, p. 68
SAR	0x12	0x27CA	0x029A	4	SYNC Alignment Register	4.7.4, p. 74
RSV1	0x13	0x27CB	0x029B	4	Reserved Register 1	4.9, p. 76
VGW	0x14	0x27CC	0x029C	5	Video Gamma Write	4.5.1, p. 65
VGD	0x15	0x27CD	0x029D	5	Video Gamma Correction Data	4.5.2, p. 66
RSV2	0x16	0x27CA	0x029A	5	Reserved Register 2	4.7, p. 71
VGR	0x17	0x27CB	0x029B	5	Video Gamma Address Read	4.5.3, p. 67
GCKR	0x18	0x27CC	0x029C	6	Graphics Chroma Key Red	4.6.2, p. 69
GCKG	0x19	0x27CD	0x029D	6	Graphics Chroma Key Green	4.6.2, p. 69
GCKB	0x1A	0x27CA	0x029A	6	Graphics Chroma Key Blue	4.6.2, p. 69
RSV3	0x1B	0x27CB	0x029B	6	Reserved Register 3	4.9, p. 76
GKMR	0x1C	0x27CC	0x029C	7	Graphics Key Mask Red	4.6.3, p. 70
GKMG	0x1D	0x27CD	0x029D	7	Graphics Key Mask Green	4.6.3, p. 70
GKMB	0x1E	0x27CA	0x029A	7	Graphics Key Mask Blue	4.6.3, p. 70
RSV4	0x1F	0x27CB	0x029B	7	Reserved Register 4	4.9, p. 76

4.1 Indexing

4.1.1 BIR: Block Index Register

I/O Address	(ISA, MCA Modes)	0x27CE
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Local Hardware Interface)	N/A

Block Index Register BIR specifies one of eight 4-register banks that can be directly read and written at 16-bit PC port addresses 0x27CA-0x27CD. The CLUT access Registers LAW, LCD, LPM, and LAR are the exception. BIR is used only in ISA and MCA Bus Modes; it is not accessible in Local Hardware Interface Mode when all registers are addressed directly through RS[4:0].

IE	RE	SE	RO	RSVD	BLK2	BLK1	BLK0
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	IE	Index Enable 1 Indexed addressing 0 Direct addressing
6	R/W	0	RE	Read Enable 1 VGA read/write access 0 VGA write-only access
5	R/W	0	SE	Secondary-Address Enable 1 Secondary address range 0 Primary address range
4	R/W	0	RO	03C7h Read Override 1 Read enabled at 03C7h 0 Read disabled at 03C7h
3	R/W	0	RSVD	Reserved
2	R/W	0	BLK2	Block Select 2
1	R/W	0	BLK1	Block Select 1
0	R/W	1	BLK0	Block Select 0

Table 4–2. Read access for VGA Compatibility Modes

IE (7)	RE (6)	RO (4)	03C7h read access	03C6h, 03C8h, 03C9h read access
0	0	x	disabled	disabled
0	1	0	disabled	enabled
0	1	1	enabled	enabled
1	x	x	enabled at indexed address via BLK[2:0]	

4.2 CLUT Access

The graphics Color Look-Up Table (CLUT) expands 4-, 8-, and 16-bit graphics pixel data to 18 or 24 bits of color data. Access modes are described in Section 3.3.6.2 on page 49.

4.2.1 LAW: CLUT Write Address

I/O Address	(ISA, MCA Modes)	0x03C8
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Local Hardware Interface)	0x00

CLUT Write Address Register LAW, a modulo-256 counter, shares two functions — palette color selection and cursor pattern selection.

Palette Color Selection

In palette Color Selection Mode, LAW specifies the 24- or 18-bit graphics palette color to be written to Register LCD on the next write operation. LAW specifies the same palette color for write cycles R, G, and B. After write cycle B, LAW automatically increments by one to specify the next palette color.

WA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	WA	Color LUT Write Address for palette RAM.

Cursor Pattern Selection

In Cursor Pattern Selection Mode, LAW addresses the cursor pattern RAM, which comprises two 32 x 32-bit or 4 x 32 byte planes for a total of 128 bytes in each plane. LAW automatically increments when writing to Register CPR.

P	WA						
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	P	Plane. Specifies the cursor bit plane to be addressed. 0 LSB plane of cursor RAM 1 MSB plane of cursor RAM
6:0	R/W	0h	WA	Color LUT Write Address for cursor RAM. Byte address of cursor pixels (8 per address) being addressed for the 128 bytes in cursor RAM. Bytes 3:0 are the four bytes of the top row.

4.2.2 LCD: CLUT Color Data

I/O Address	(ISA, MCA Modes)	0x03C9
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Local Hardware Interface)	0x01

Port LCD is an 8-bit-wide path to the graphics color palette — a 256 x 18- or 24-bit memory array. LCD must be addressed three times, once for each palette color.

For read operations:

- The first read operation reads the red 6- or 8-bit component (as specified by Register ASC, Bit D24) of the palette color specified by LAR.
- The second read operation reads the green 6- or 8-bit component of the palette color specified by LAR.
- The third read operation reads the blue 6- or 8-bit component of the palette color specified by LAR.

After the blue component is read, Register LAR automatically increments to the next palette color. When in 6-bit Mode, the data shifts left two bits and the two LSbs are padded with '0's before loading into the palette.

For write operations:

- The first write operation writes the red 6- or 8-bit component of the palette color specified by LAW.
- The second write operation writes the green 6- or 8-bit component of the palette color specified by LAW.
- The third write operation writes the blue 6- or 8-bit component of the palette color specified by LAW.

After the blue component is written, Register LAW automatically increments to the next palette color. When in 6-bit Mode, the data shifts left two bits and the two LSbs are padded with '0's before loading into the palette.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	D	Color LUT Data.

4.2.3 LPM: CLUT Pixel Mask

I/O Address	(ISA, MCA Modes)	0x03C6
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Local Hardware Interface)	0x02

The graphics pixel data used to look up color information in the palette can be masked before the lookup occurs. Register LPM masks the address. The 6- or 8-bit graphics pixel is logically AND'ed with the LPM data and the result is used to address the color palette.

M							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0h	M	Color LUT Pixel Mask Data.

4.2.4 LAR: CLUT Read Address

I/O Address	(ISA, MCA Modes)	0x03C7
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Local Hardware Interface)	0x03

CLUT Read Address Register LAR is a modulo-256 counter that shares two functions — palette color selection and cursor pattern selection.

Palette Color Selection

In Palette Color Selection Mode, LAR specifies the 24- or 18-bit graphics palette color to be read on the next read operation to Register LCD. LAR specifies the same palette color for read cycles R, G, and B. After read cycle B, LAR automatically increments by one to specify the next palette color.

RA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	RA	Color LUT Read Address.

Cursor Pattern Selection

In Cursor Pattern Selection Mode, LAR addresses the cursor pattern RAM, which comprises two 32 x 32-bit or 4 x 32-byte planes for a total of 128 bytes in each plane. LAR automatically increments when writing to Register CPR.

P	RA						
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	P	Plane. Specifies the cursor bit plane to be addressed. 0 Lower plane of cursor RAM 1 Upper plane of cursor RAM
6:0	R/W	0h	RA	Color LUT Read Address. Byte address of cursor pixels (8 per address) being addressed for the 128 bytes in cursor RAM. Bytes 3:0 are the four bytes of the top row.

4.3 Cursor Access

4.3.1 CAW: Cursor Address Write

I/O Address	(ISA, MCA Modes)	0x27CC
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Local Hardware Interface)	0x04

Cursor Address Write Register (CAW) is a modulo-4 counter that specifies the 24-bit Cursor or Border Color Register that is to be modified on the next write operation to Register CCD. CAW specifies the same Cursor Color Register for write cycles R, G, and B. After write cycle B, CAW automatically increments by one to specify the next Cursor Color Register.

RSVD						WA	
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:2	R/W	0h	RSVD	Reserved (write as '0').
1:0	R/W	00	WA	Cursor Write Address.

4.3.2 CCD: Cursor Color Data Registers

I/O Address	(ISA, MCA Modes)	0x27CD
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Local Hardware Interface)	0x05

See the following also: Table 3–12. *DAC Source Control*, page 50.
Figure 3–18. *Cursor RAM Function Diagram*, page 49.

Port CCD accesses three 24-bit Cursor and Border Color Registers.

- For cursor color read operations, Register CAR must point to the cursor color to be read.
- For cursor color write operations, Register CAW must point to the cursor color to be written.

CAR and CAW point to the red component of each color only.

Three I/O operations — R, G, and B — must occur for each color. CAR and CAW automatically increment by one after I/O operation B. The components must be read and/or written in the following order: red, green, blue.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	D	Color Data.

4.3.3 CAR: Cursor Address Read

I/O Address	(ISA, MCA Modes)	0x27CB
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Local Hardware Interface)	0x07

Register CAR is a modulo-4 counter that specifies the 24-bit Cursor Color Register to be read on the next read operation to Register CCD. CAR specifies the same Cursor Color Register for read cycles R, G, and B. After read cycle B, CAR automatically increments by one to specify the next Cursor Color Register.

RSVD						RA	
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:2	R/W	0h	RSVD	Reserved (write as '0').
1:0	R/W	00	RA	Cursor Read Address.

4.3.4 CPR: Cursor Pattern RAM

I/O Address	(ISA, MCA Modes)	0x27CB
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Local Hardware Interface)	0x0B

Registers LAW and LAR address Register CPR. The cursor pattern RAM comprises two 32 x 32-bit (or 4 x 32-byte) planes for a total of 128 bytes for each plane. A write or read to the CPR writes or reads the cursor pattern data.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	D	Cursor Pattern RAM Data.

4.4 Video, Graphics, and Cursor Control

4.4.1 GSR: Graphics Status Register

I/O Address	(ISA, MCA Modes)	0x27CA
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Local Hardware Interface)	0x0A

Read-only Register GSR is a modulo-3 counter that sets up and monitors the CL-PX2080 revisions and I/O cycles.

REV				S	IO	CP	
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:4	Read Only	0h	REV	Revision level. Current REV is '0000'.
3	Read Only	0	S	Sense bit status. 0 All analog outputs are below the 335-mV level. 1 At least one of the analog outputs have exceeded the 335-mV level.
2	Read Only	0	IO	I/O read/write access status. 0 LAW, CAW, or VGW has been specified (Write Mode). 1 LAR, CAR, or VGR has been specified (Read Mode).
1:0	Read Only	00	CP	Color Pointer. Color component to be accessed by Host on next I/O cycle to a palette: 00 Red is specified. 01 Green is specified. 10 Blue is specified.

4.4.2 GFC: Graphics Format Control

I/O Address	(ISA, MCA Modes)	0x27CC
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Local Hardware Interface)	0x08

Register GFC sets up the graphic interface timing and color format controls.

RSVD	GPF		TC	CF	MR	TE	PS
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	RSVD	Reserved (write as '0').
6:5	R/W	00	GPF	Graphics Port Format. Selects data type: 00 24-bit pixel 8:8:8 RGB data (PCLK:LCLK = 1:1). 01 16-bit pixel mode (mux ratios set by Bit 2 of Register GFC). 10 Four 8-bit pixels (PCLK:LCLK = 4:1). 11 Eight 4-bit pixels (PCLK:LCLK = 8:1).
4	R/W	0	TC	True Color graphics palette bypass: 0 Pixel data is pseudocolor; PS, TE, MR, CF are ignored. 1 Pixel data is true color.
3	R/W	0	CF	Color Format. Controls 16-bit graphics port RGB color format: 0 5:5:5 1 5:6:5
2	R/W	0	MR	Multiplexing Rate. Controls 16-bit graphics port data multiplexing rate: 0 The PCLK to LCLK ratio is 2:1 (two-pixel bus). 1 The PCLK to LCLK ratio is 1:1 (one-pixel bus).
1	R/W	0	TE	Tag Enable. Specifies graphics 5:5:5 RGB 1:1 Mux Data Mode pixel selector: 0 Bit 0 in Register GFC is pixel selector. 1 GSD[31:0] is video pixel selector in the 5:5:5 RGB Graphics Data Mode.
0	R/W	0	PS	Pixel Selector. Selects Graphics pixel for 5:6:5 and 5:5:5 RGB 1:1 mux data: 0 Graphics pixel 0 (graphics data on port GSD[15:0]). 1 Graphics pixel 1 (graphics data on port GSD[31:16]).

4.4.3 CSC: Cursor Setup Control

I/O Address	(ISA, MCA Modes)	0x27CD
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Local Hardware Interface)	0x09

Register CSC sets cursor modes and controls palette indexing for 16-bit graphics data modes and clock selections.

SD	GPS		CS	DM	PM	CMS	
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	SD	SCLK Disable: 0 SCLK is enabled. 1 SCLK is disabled.
6:5	R/W	00	GPS	Graphics data Port Selection pin enable: 00 Pin GPS is disabled (VGA port always selected). 01 Pin GPS is enabled (VGA or Serial Graphics port). 10 Pin GPS is disabled (Serial Graphics port always selected). 11 Pin GPS is disabled (Serial Graphics port is output, VGA input).
4	R/W	0	CS	Pixel Clock Selection: 0 PCLK0 is selected. 1 PCLK1 is selected.
3	R/W	0	DM	Display Mode: 0 Progressive scan displays. 1 Interlaced scan displays.
2	R/W	0	PM	Palette Mapping for 16-bit graphics data to 18-bit DAC: 0 Color components are mapped to MSbs of their appropriate palettes. 1 Color components are mapped to LSbs of their appropriate palettes. All unused bits of color components are padded with '0's.
1:0	R/W	00	CMS	Cursor Mode Select. 00 Cursor disabled. 01 Three color cursor. 10 Two color cursor with highlighting. 11 Two color cursor.

4.5 Video Gamma Correction Palette Access

The video gamma correction palette is a 256 x 24-bit memory array that maps non-linear video pixel data to linear color data. The gamma palette is accessed through Registers VGR, VGD, and VGW when Register BIR is '5h'.

4.5.1 VGW: Video Gamma Write

I/O Address	(ISA, MCA Modes)	0x27CC
Base Index Register	(ISA, MCA Modes)	5
Direct Address	(Local Hardware Interface)	0x14

Register VGW is a modulo-256 counter that specifies the 24-bit video gamma palette color to be written on the next write operation to Register VGD. Register VGW points to the same palette color for write cycles R, G, and B. After the write cycle B, it automatically increments by one to specify the next palette color.

WA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	WA	Gamma Correction Write Address. Byte address of gamma palette RAM.

4.5.2 VGD: Video Gamma Correction Data

I/O Address	(ISA, MCA Modes)	0x27CD
Base Index Register	(ISA, MCA Modes)	5
Direct Address	(Local Hardware Interface)	0x15

The VGD port is an 8-bit-wide path to the graphics color palette (a 256 x 24-bit memory array) and must be addressed three times for each palette color.

For read operations:

- The first read operation reads the red 8-bit component of the palette color specified by VGR.
- The second read operation reads the green 8-bit component of the palette color specified by VGR.
- The third read operation reads the blue 8-bit component of the palette color specified by VGR.

After the blue component is read, Register VGR automatically increments to the next palette color. When in 6-bit Mode, the data shifts left two bits and the two LSbs are padded with '0's before loading into the palette.

For write operations:

- The first write operation writes the red 8-bit component of the palette color specified by VGW.
- The second write operation writes the green 8-bit component of the palette color specified by VGW.
- The third write operation writes the blue 8-bit component of the palette color specified by VGW.

After the blue component is written, Register VGW automatically increments to the next palette color.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	D	Video gamma correction Data.

4.5.3 VGR: Video Gamma Address Read

I/O Address	(ISA, MCA Modes)	0x27CB
Base Index Register	(ISA, MCA Modes)	5
Direct Address	(Local Hardware Interface)	0x17

Register VGR is a modulo-256 counter that specifies the next 24-bit video gamma palette color to be read on the next read operation to Register VGD. VGR specifies the same palette color for read cycles R, G, and B. After the read cycle B, it automatically increments by one to specify the next palette color.

RA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	RA	Gamma Correction Read Address. Byte address of gamma palette RAM.

4.6 Graphics Overlay Control

The graphics overlay controls comprise:

- an 8-bit Graphics Overlay Opcode — Register GOC;
- a 32-bit Graphics Chroma Key — Registers GKMc;
- a 32-bit Graphics Key Mask — Registers GKMc;
- an 8:1 multiplexer.

The CL-PX2080 can be viewed as a dual image formatter. The graphics image is in front; the video image is in back.

Every graphics pixel is either opaque or transparent.

- If the graphics pixel is opaque, its graphics color information is displayed on the screen.
- If the graphics pixel is transparent, the color information of the video pixel behind it is displayed on the screen.

The graphics overlay controls determine which graphics pixels are transparent, based on a combination of two overlay control features:

- a TAG Bit component in the video pixel data, which is generated outside the CL-PX2080;
- the graphics COLOR key switch, which is generated by AND'ing the graphics pixel data with the GKM Register and then comparing the results against the GCK Register.

4.6.1 GOC: Graphics Overlay Opcode

I/O Address	(ISA, MCA Modes)	0x27CD
Base Index Register	(ISA, MCA Modes)	4
Direct Address	(Local Hardware Interface)	0x11

GOC is an 8-bit value that inputs to an 8:1 multiplexer. The select signals to the multiplexer — the TAG Bit and the graphics COLOR key match — determine which of the eight bits become the transparency control for each pixel time. A high bit in Register GOC enables video and makes graphics transparent. This value selects the graphics path and ignores video input stream.

T							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	T	Transparency. Graphics pixel transparency control bitmap for function (TAG, COLOR), as shown in Table 4–3. 1 Select video pixel for function. 0 Select graphics pixel for function.

Table 4–3. GOC Control Bit Mapping

TAG	COLOR	GOC Control Bit
0	0	T0
0	1	T1
1	0	T2
1	1	T3
0	0	T4
0	1	T5
1	0	T6
1	1	T7

4.6.2 GKMc: Graphics Chroma Key

I/O Address	(ISA, MCA Modes)	0x27CC (GCKR: Graphics Chroma Key Red) 0x27CD (GCKG: Graphics Chroma Key Green) 0x27CA (GCKB: Graphics Chroma Key Blue)
Base Index Register	(ISA, MCA Modes)	6 (GCKR: Graphics Chroma Key Red) 6 (GCKG: Graphics Chroma Key Green) 6 (GCKB: Graphics Chroma Key Blue)
Direct Address	(Local Hardware Interface)	0x18 (GCKR: Graphics Chroma Key Red) 0x19 (GCKG: Graphics Chroma Key Green) 0x1A (GCKB: Graphics Chroma Key Blue)

Registers GCKR, GCKG, and GCKB control the Graphics Chroma Key function.

- When the CL-PX2080 uses the 8-bit VGA port for graphics data, the data in Registers GCKc is compared against four adjacent graphics pixels. GCKR is compared to the least-significant pixel.
- When the CL-PX2080 uses the 32-bit graphics port, the data in Registers GCKc is used as specified by the PCLK:SCLK ratio.

4.6.2.1 GCKR: Graphics Chroma Key Red

CKR							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	CKR	Chroma Key Red Data.

4.6.2.2 GCKG: Graphics Chroma Key Green

CKG							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	CKG	Chroma Key Green Data.

4.6.2.3 GCKB: Graphics Chroma Key Blue

CKB							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	CKB	Chroma Key Blue Data.

4.6.3 GKMc: Graphics Key Mask

I/O Address	(ISA, MCA Modes)	0x27CC (GKMR: Graphics Key Mask Red) 0x27CD (GKMG: Graphics Key Mask Green) 0x27CA (GKMB: Graphics Key Mask Blue)
Base Index Register	(ISA, MCA Modes)	7 (GKMR: Graphics Key Mask Red) 7 (GKMG: Graphics Key Mask Green) 7 (GKMB: Graphics Key Mask Blue)
Direct Address	(Local Hardware Interface)	0x1C (GKMR: Graphics Key Mask Red) 0x1D (GKMG: Graphics Key Mask Green) 0x1E (GKMB: Graphics Key Mask Blue)

Registers GKMR, GKMG, and GKMB control the Graphics Color Key Mask function.

- When the CL-PX2080 uses the 8-bit VGA port for graphics data, the data in Registers GKMc is AND'ed with four adjacent graphics pixels. GKMR is compared to the least-significant pixel.
- When the CL-PX2080 uses the 32-bit graphics port, the data in Registers GKMc is used as specified by the PCLK:SCLK ratio.

4.6.3.1 GKMR: Graphics Key Mask Red

MR							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	1	MR	Graphics Key Mask Red Data.

4.6.3.2 GKMG: Graphics Key Mask Green

MG							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	1	MG	Graphics Key Mask Green Data.

4.6.3.3 GKMB: Graphics Key Mask Blue

MB							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	1	MB	Graphics Key Mask Blue Data.

4.7 Cursor Positioning

4.7.1 CXb: Cursor X Position

I/O Address	(ISA, MCA Modes)	0x27CC (CXL: Cursor X Position, Low Byte) 0x27CD (CXH: Cursor X Position, High Byte)
Base Index Register	(ISA, MCA Modes)	3 (CXL: Cursor X Position, Low Byte) 3 (CXH: Cursor X Position, High Byte)
Direct Address	(Local Hardware Interface)	0x0C (CXL: Cursor X Position, Low Byte) 0x0D (CXH: Cursor X Position, High Byte)

The 8-bit Registers CXL and CXH specify the X position of the bottom right corner of the cursor relative to the left side of the display screen.

- When CXL is '1' and CXH is '0', the right-most column of pixels of the cursor is positioned at the left-most column of pixels of the display screen.
- When CXL is '0' and CXH is '0', the cursor is positioned completely off-screen one column to the left of the first displayed column of pixels on the screen.
- During reset, CXH is '0x00' and CXL is '0x00'; the cursor is positioned in the upper left corner, off-screen.

4.7.1.1 CXL: Cursor X Position, Low Byte

X							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	X	Cursor X position Low Byte.

4.7.1.2 CXH: Cursor X Position, High Byte

RSVD				X			
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:4	R/W	0	RSVD	Reserved (read as '0').
3:0	R/W	0	X	Cursor X position High Byte.

4.7.2 CYb: Cursor Y Position

I/O Address	(ISA, MCA Modes)	0x27CA (CYL: Cursor Y Position, Low Byte) 0x27CB (CYH: Cursor Y Position, High Byte)
Base Index Register	(ISA, MCA Modes)	3 (CYL: Cursor Y Position, Low Byte) 3 (CYH: Cursor Y Position, High Byte)
Direct Address	(Local Hardware Interface)	0x0E (CYL: Cursor Y Position, Low Byte) 0x0F (CYH: Cursor Y Position, High Byte)

Registers CYb specify the Y position of the bottom right corner of the cursor relative to the top of the display screen.

- When CYL is '1' and CYH is '0', the bottom row of pixels of the cursor is positioned at the top row of pixels of the display screen.
- When CYL is '0' and CYH is '0', the cursor is positioned completely off-screen, one column above the first displayed row of pixels on the screen.
- During reset, CYH is '0' and CYL is '0'; the cursor is positioned in the upper left corner, off-screen.

4.7.2.1 CYL: Cursor Y Position, Low Byte

Y							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	Y	Cursor Y position Low Byte.

4.7.2.2 CYH: Cursor Y Position, High Byte

RSVD				Y			
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:4	R/W	0	RSVD	Reserved (read as '0').
3:0	R/W	0	Y	Cursor Y position High Byte.

4.7.3 VFC: Video Format Control

I/O Address	(ISA, MCA Modes)	0x27CC
Base Index Register	(ISA, MCA Modes)	4
Direct Address	(Local Hardware Interface)	0x10

Register VFC sets up the video bus interface timing and color format controls.

EC	CS	RSVD	GBYP	CSF			
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	EC	Extended Color Mode for VGA data. 0 Normal Mode. 1 Extended Color Mode.
6	R/W	0	CS	Clock Select for graphics data. 0 LCLK 1 PCLK
5	R/W	000	RSVD	Reserved (write as '0').
4	R/W	0	GBYP	Gamma Bypass. Disables Gamma Correction. 0 Gamma enabled. 1 Gamma disabled.
3:0	R/W	0000	CSF	Color Space Format of Video Bus: 0000 YUV 4:2:2 format non-tagged data. 0001 Y(U:T)(V:T) 4:(2):(2) format (LSb of U and V are tag data). 1000 RGB 5:6:5 format. 1010 RGB 5:5:5 format 1011 TRGB 1:5:5:5 format (MSb is tag data). 1110 RGB 8:8:8 format non-tagged. 1111 TRGB 1:8:8:8 format (Bit 31 is tag bit). All other bit configurations are reserved.

4.7.4 SAR: SYNC Alignment Register

I/O Address	(ISA, MCA Modes)	0x27CA
Base Index Register	(ISA, MCA Modes)	4
Direct Address	(Local Hardware Interface)	0x12

Register SAR programs incoming and outgoing sync signals to match the monitor in both polarity and PCLK delay relative to the DAC outputs and internal pixel pipeline. SAR also sets the output sync signals VSOUT and HSOUT to align with the DAC R, G, and B outputs in PCLK time units.

HP	HL	VP	VL	DIR	DLY		
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	HP	Horizontal sync Input Polarity: 0 HSIN = active low. 1 HSIN = active high.
6	R/W	0	HL	Active display output polarity in LCD Mode: 0 WINACT = active low. 1 WINACT = active high.
5	R/W	0	VP	Vertical sync Input Polarity: 0 VSIN = active low. 1 VSIN = active high.
4	R/W	0	VL	Horizontal and vertical sync output polarity in LCD Mode: 0 HSOUT = active low. 1 HSOUT = active high.
3	R/W	0	DIR	Delay Direction of HSOUT, VSOUT relative to R, G, and B. 0 Sync Signals behind DAC outputs. 1 Sync Signals ahead of DAC outputs.
2:0	R/W	000	DLY	Delay in number of PCLKs. 000 No delay. 111 7 PCLK difference.

4.8 Digital-to-Analog Conversion and Controls

The analog RGB signals produce 0.7-volt peak white amplitude with an IREF of 8.8 mA when driving a doubly-terminated 75-ohm load. This process corresponds to an effective DAC output load (R effective) of 37.5 ohms.

The following equation calculates IREF for various peak white voltages and output loading values:

$$IREF = \frac{Vpeak\ white}{2.097 \times R\ effective}$$

The following equation applies to all values of IREF and output loading:

$$Vbacklevel = zero\ volts$$

The analog circuitry is powered by the AVDD voltage, which is bonded-out separately from the digital power. A decoupling capacitor must be attached externally between AVDD and VSS.

4.8.1 ASC: Analog Setup Control

I/O Address	(ISA, MCA Modes)	0x27CA
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Local Hardware Interface)	0x06

Register ASC sets up the DAC and analog output.

RSVD	COFF	RSVD				D24	DOFF
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7	R/W	0	RSVD	Reserved (write as '0').
6	R/W	0	COFF	Clock Off 0 Normal operation. 1 Powers down the CL-PX2080. Clocks forced high.
5:2	R/W	0	RSVD	Reserved (write as '0').
1	R/W	0	D24	18/24-Bit Data 0 18-bit DAC. 1 24-bit DAC.
0	R/W	0	DOFF	DAC Off 0 Normal operation. 1 Disables the analog circuitry.

4.9 Reserved Registers

I/O Address	(ISA, MCA Modes)	0x27CB (RSV1: Reserved Register 1) 0x27CA (RSV2: Reserved Register 2) 0x27CB (RSV3: Reserved Register 3) 0x27CB (RSV4: Reserved Register 4)
Base Index Register	(ISA, MCA Modes)	4 (RSV1: Reserved Register 1) 5 (RSV2: Reserved Register 2) 6 (RSV3: Reserved Register 3) 7 (RSV4: Reserved Register 4)
Direct Address	(Local Hardware Interface)	0x13 (RSV1: Reserved Register 1) 0x16 (RSV2: Reserved Register 2) 0x1B (RSV3: Reserved Register 3) 0x1F (RSV4: Reserved Register 4)

Registers RSV1, RSV2, RSV3, and RSV4 are reserved.

RSVD							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0h	RSVD	Reserved (write as '0').

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the CL-PX2080. Stresses above those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Storage temperature ..... -65° to +150° C

Voltage on any pin with respect to ground ..... -0.5 volts to V_{DD} + 0.5 volts

Power supply voltage ..... 7 volts

Lead temperature (10 seconds) ..... 300° C

5.2 CL-PX2080 DC Specifications (Digital)

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{DD}	Power Supply Voltage	4.75	5.25	V	Normal Operation
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{DD} + 0.8	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA
V_{ILC}	Input Low Voltage CMOS		0.8	V	
V_{IHC}	Input High Voltage CMOS	3.0		V	
V_{OLC}	Output Low Voltage CMOS		0.4	V	I_{OLC} = 3.2 mA
V_{OHC}	Output High Voltage CMOS	3.5		V	I_{OHC} = -200 µA
I_{DD}	Digital Supply Current		N/A	mA	V_{DD} Nominal
I_{DDT}	Total Supply Current		N/A	mA	Note 1
I_L	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTES: 1) I_{DDT} is the sum of I_{DD} + $DACI_{DD}$ + $CLKI_{DD}$; it must be <200 mA (package constraint).
2) DACVSS must not exceed V_{DD}.

5.3 CL-PX2080 DC Specifications (RAMDAC)

(V_{DD} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD	Power Supply Voltage	4.75	5.25	V	Normal Operation
I_{REF}	DAC Reference Current	-7.0	-10.0	mA	Notes 1, 2
$DACI_{DD}$	DAC Supply Current		85	mA	Note 3

NOTES: 1) Reference Current (IREF) outside the specified limits may cause the analog outputs to become invalid.
2) The dotclock must be stable for a period of 100 µs after power-up before proper DAC operation is guaranteed.
3) DACIDD is specified with the three analog outputs (R,G,B) each loaded with 37.5 ohms.

5.4 CL-PX2080 DAC Characteristics

(V_{DD} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
R	Resolution	8		bits	
I_{Omax}	Output Current		-27	mA	V_O < 1 V
Co	Output Capacitance		12	pF	
t_D	Analog Output Delay		30	ns	Notes 1, 2, 3
t_R	Analog Output Rise/Fall time		3	ns	Notes 2, 3, 4
t_S	Analog Output Settling time		13	ns	Notes 2, 3, 5
t_{SK}	Analog Output Skew		TBD	ns	Notes 2, 3, 6, 8
FT	Clock and Data Feedthrough		-30	db	Notes 2, 3, 6
DT	DAC-to-DAC Variability		± 2	%	Notes 6, 7
GI	Glitch Impulse		TBD		Notes 2, 3, 6, 8
CT	DAC-to-DAC Crosstalk		-23	db	Notes 2, 3, 6

NOTES: 1) t_D is measured from the 50% point of VDCLK to 50% point of full-scale transition.
2) Load is 37.5 ohms and 30 pF per analog output.
3) I_{REF} = -8.8 mA.
4) t_R is measured from 10% to 90% full scale.
5) t_S is measured from 50% point of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale deflection.
8) TBD = to be determined.

5.5 AC Characteristics/Timing Information

This section includes system timing requirements for the CL-PX2080. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0° to 70° C, and V_{DD} varying from 4.75 to 5.25 volts DC.

NOTES: 1) All timings assume a load of 50 pF.
2) TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

5.5.1 Index of Timing Information

Item **Page Number**

5.5.2 I/O Timing (ISA Bus)

Table 5–1. I/O Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time, valid address to IOR*/IOW* active	25		ns
t_2	Delay, IOR*/IOW* active to DEN* active, DDIR change		20	ns
t_3	Delay, IOR* active to data output low Z	5	25	ns
t_4	Delay, IOR* active to data out valid		40	ns
t_5	Pulse width, IOR*/IOW*	50		ns
t_6	Delay, IOR*/IOW* inactive to DEN* inactive, DDIR chng		20	ns
t_7	IOR* inactive to Three-State delay		15	ns
t_8	Address hold time from IOR*/IOW* active	0		ns
t_9	Setup time, data valid to IOW* inactive	20		ns
t_{10}	Hold time, IOW* inactive to data invalid	0		ns
t_{11}	Delay, IOW* inactive to next IOW* or IOR* active	50		ns
t_{12}	Setup, AEN rising edge to IOW* or IOR* active	10		ns
t_{13}	Delay, IOW* or IOR* inactive to AEN falling edge	10		ns

NOTES: 1) AEN must be low.
2) The low-byte address-buffer enable must be qualified by IOR* to avoid data contention. See Section 3.1.1 on page 26 for additional information.

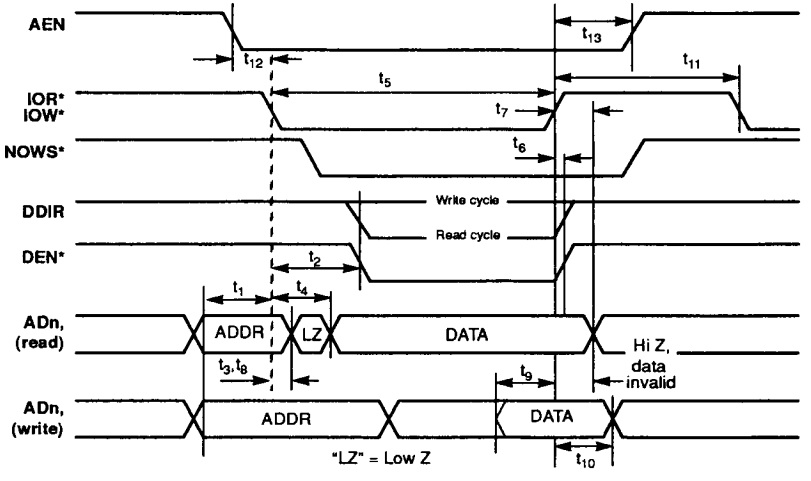


Figure 5–1. I/O Timing (ISA Bus)

5.5.3 CMD* Timing (MCA Bus)

Table 5–2. CMD* Timing (MCA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time, address valid to CMD* active	25		ns
t_2	Delay, CMD* active to DEN* active		20	ns
t_{3a}	Hold time, address valid from CMD* active	0		ns
t_{3b}	Delay, CMD* active to data output low Z	5	25	
t_4	Delay, CMD* active to read data valid		40	ns
t_5	Pulse width, CMD*	50		ns
t_6	Delay, CMD* inactive to data invalid, high Z		15	ns
t_7	Setup time, write data valid to CMD* inactive	20		ns
t_8	Hold time, write data valid to CMD* inactive	0		ns
t_9	Delay, CMD* inactive to next CMD* active	50		ns
t_{10}	Setup time, status valid to CMD* active	25		ns
t_{11}	Hold time, CMD* active to status invalid	5		ns
t_{12}	Delay, CMD* inactive to DEN* inactive, DDIR change		20	ns

NOTE: See Write Cycle and Read Cycle diagrams for data timing with respect to CMD*.

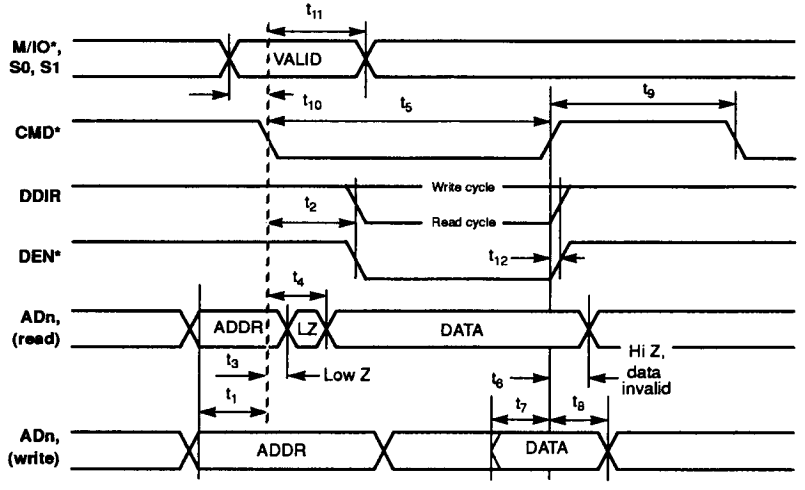


Figure 5–2. CMD* Timing (MCA Bus)

5.5.4 I/O Timing (Local Hardware Interface Bus)

Table 5–3. I/O Timing (Local Hardware Interface Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time, valid address to IOR*/IOW* active	25		ns
t_2	Delay, IOR*/IOW* active to DEN* active, DDIR change		20	ns
t_3	Delay, IOR* active to data out low Z	5	25	ns
t_4	Delay, IOR* active to data out valid		40	ns
t_5	Pulse width, IOR*/IOW*	50		ns
t_6	Delay, IOR*/IOW* inactive to DEN* inactive, DDIR chng		20	ns
t_7	Delay, IOR* inactive to data Hi Z		15	ns
t_8	Hold time from IOR*/IOW* active to Address invalid	0		ns
t_9	Setup time, data valid to IOW* inactive	20		ns
t_{10}	Hold time, IOW* inactive to data invalid	0		ns
t_{11}	Delay, IOW* inactive to next IOW* or IOR* active	50		ns
t_{12}	Setup, CS* falling edge to IOW* or IOR* active	10		ns
t_{13}	Delay, IOW* or IOR* inactive to CS* inactive	10		ns

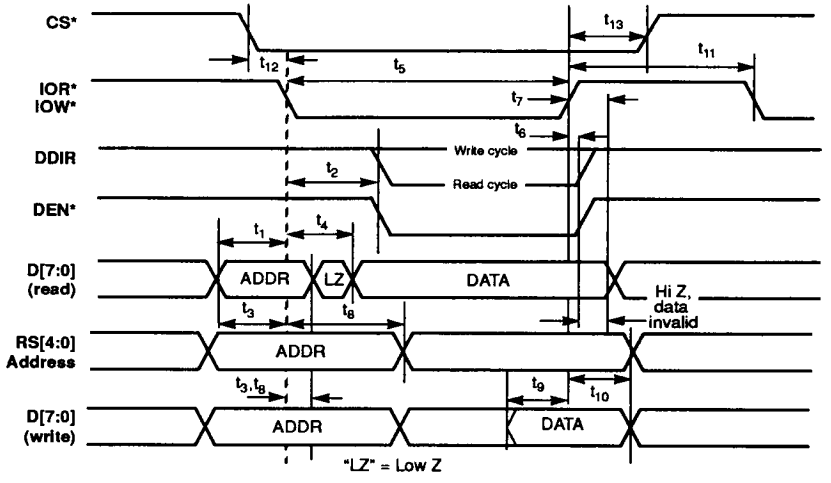


Figure 5–3. I/O Timing (Local Hardware Interface Bus)

5.5.5 Clocks as Inputs (LCLK = 1:1 Mux Rate)

Table 5–4. Clocks as Inputs (LCLK = 1:1 Mux Rate)

		85 MHz		65 MHz		
Symbol	**Parameter**	**MIN**	**MAX**	**MIN**	**MAX**	**Unit**
t_1	Rise time:					
	PCLK0		1		1	ns
	PCLK1		1		1	ns
	LCLK		1		1	ns
	VCLK		1		1	ns
t_2	Fall time:					
	PCLK0		1		1	ns
	PCLK1		1		1	ns
	LCLK		1		1	ns
	VCLK		1		1	ns
t_3	High Period (Note 1):					
	PCLK0	4		6		ns
	PCLK1	4		6		ns
	LCLK	4		6		ns
	VCLK	8		8		ns
t_4	Low Period (Note 1):					
	PCLK0	4		8		ns
	PCLK1	4		6		ns
	LCLK	4		4		ns
	VCLK	8		8		ns
t_5	Cycle time					
	PCLK0	1:5		15		ns
	PCLK1	11.5		15		ns
	LCLK	11.5		15		ns
	VCLK	20		20		ns

NOTE: LCLK and SCLK cycle and pulse width times are multiplied by 2, 4, and 8 in 2:1, 4:1, and 8:1 Multiplexing Modes, respectively.

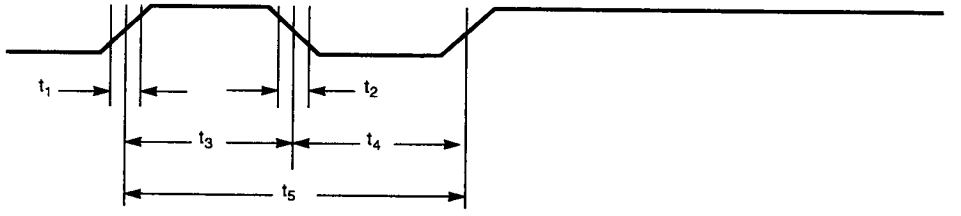


Figure 5–4. Clocks as Inputs (LCLK = 1:1 Mux Rate)

5.5.6 Sync, RGB, and GSD[23:0] Output Timing from PCLKn

Table 5–5. Sync, RGB, and GSD[23:0] Output Timing from PCLKn

Symbol	Parameter	MIN	MAX	Unit
t_1	PCLKn rise to R,G,B output delay		30	ns
t_2	R,G,B output rise/fall	3		ns
t_3	R,G,B output full-scale settling time		15	ns
t_4	PCLK rise to VSOUT, HSOUT output delay	2	10	ns
t_5	PCLK rise to GSD[23:0] output delay	2	10	ns
not shown	R,G,B output to SENSE output delay		1	µs

NOTES: 1) Output delay is measured from the 50% point of the rising edge of PCLK to the 50% point of full-scale transition.
2) Settling time is measured from the 50% point of full-scale transition to the output remaining within +/- 1 LSB.
3) Output rise/fall time is measured between the 10% and 90% points of full-scale transition.
4) In 1:1 Multiplexing Mode, RGB data is clocked out directly from LCLK, and synchronizing with SCLK and PCLK is unnecessary and bypassed. All timing PCLK references in the table above apply to LCLK when in 1:1 Multiplexing Mode.

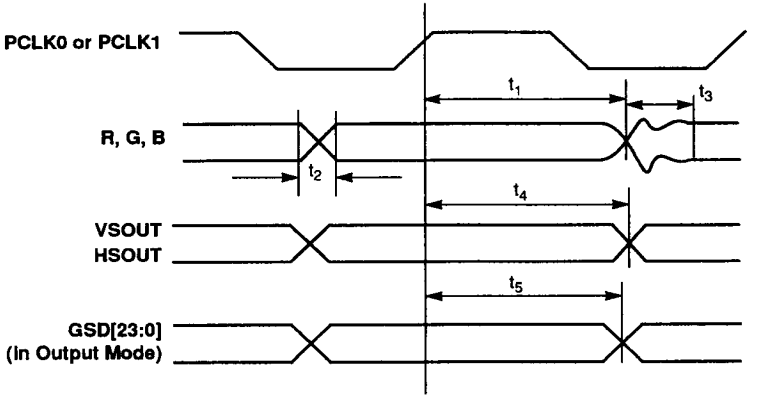


Figure 5–5. Sync, RGB, and GSD[23:0] Output Timing from PCLKn

5.5.7 Graphics Port Input Timing

Table 5–6. Graphics Port Input Timing

Symbol	Parameter	MIN	MAX	Unit
t_1	SCLK rise to LCLK rise synchronizer hold time	0		ns
t_{2a}	PCLKn rise to SCLK output delay (1:1 Mode)		10	ns
t_{2b}	PCLKn rise to SCLK output delay (2:1, 4:1, 8:1 Mode)		15	ns
t_3	Graphics data, control to LCLK rise setup time	1		ns
t_4	Graphics data, control to LCLK rise hold time	5		ns

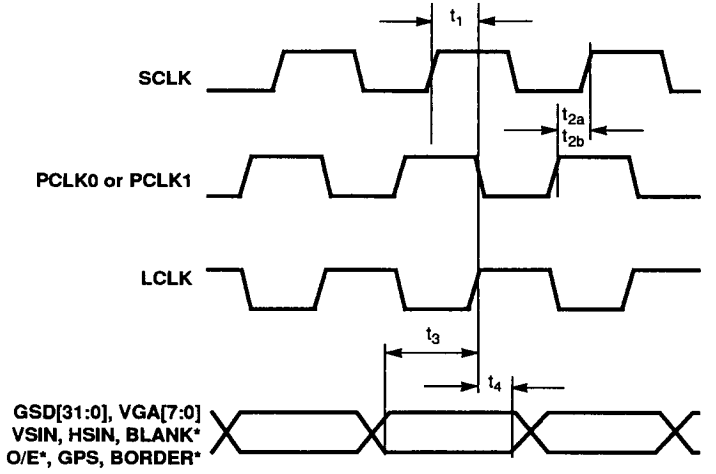


Figure 5–6. Graphics Port Interface Timing

5.5.8 VGA Port Interface Timing, EC Mode

Table 5–7. VGA Port Interface Timing, EC Mode

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time, MSB data valid to falling edge PCLK	-1		ns
t_2	Hold time, PCLKn falling edge to MSB data	7		ns
t_3	Setup time, LSB data and graphics controls valid to rising edge PCLK	-1		ns
t_4	Hold time, PCLKn rising edge to LSB data, graphics controls invalid	7		ns
t_5	Pulse width, PCLK low	8		ns
t_6	Pulse width, PCLK high	8		
t_7	Period, PCLK	20		
t_8	Delay, PCLK rising edge to RGB output		30	
t_9	Settling time, full-scale RGB output		15	ns
t_{10}	Delay, RGB out to SENSE valid	0	1	µs
t_{11}	Pipeline delay		32	PCLK cycles

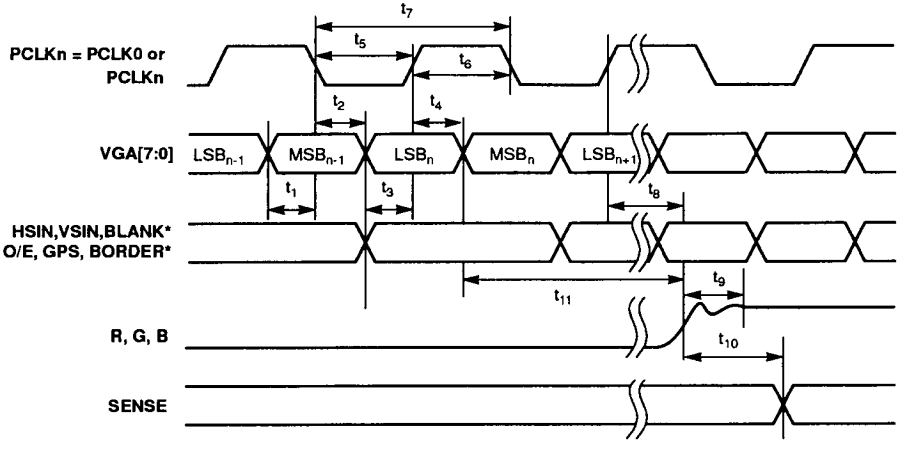


Figure 5–7. VGA Port Interface Timing, EC Mode (16-Bit)

6. PACKAGE DIMENSIONS — 160-Lead PQFP

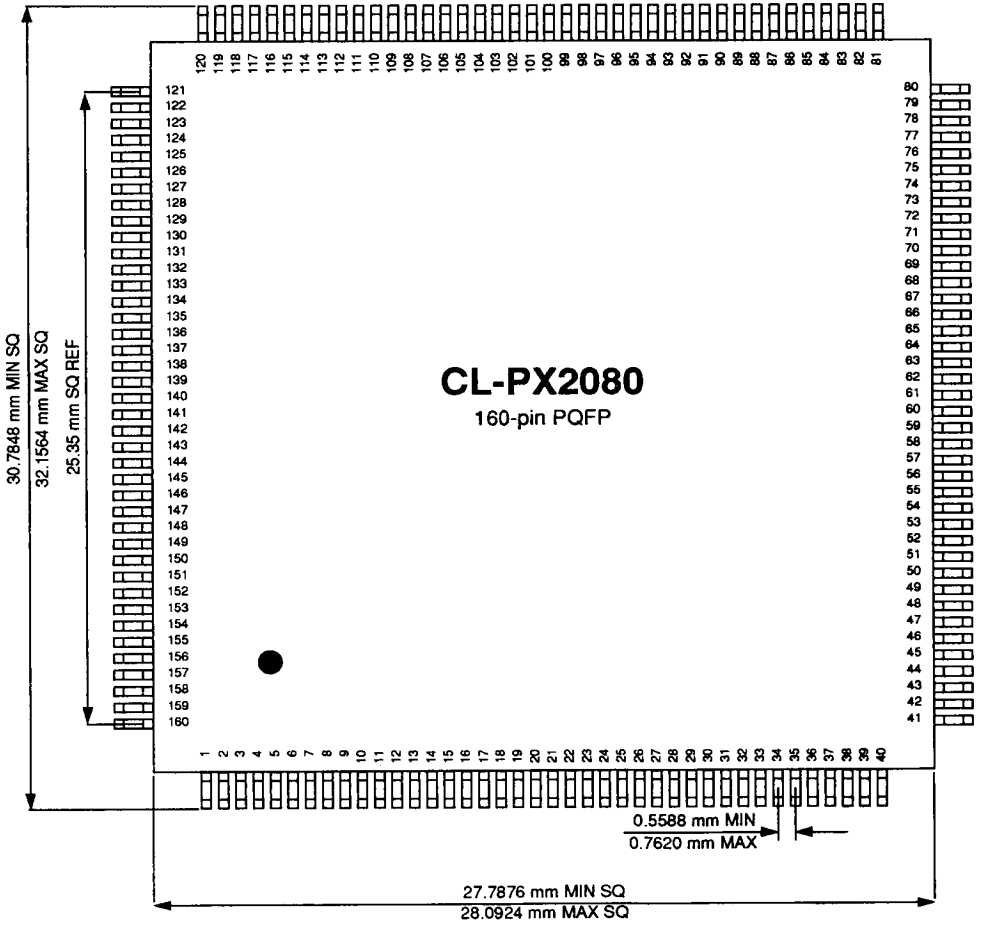


Figure 6–1. CL-PX2080 Package Information

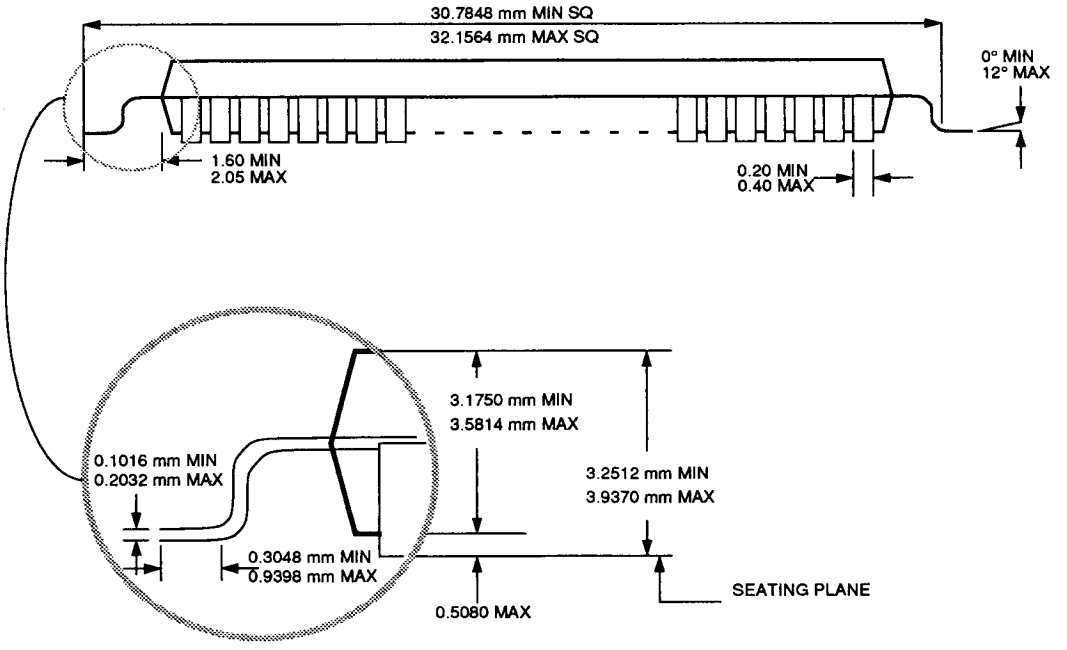
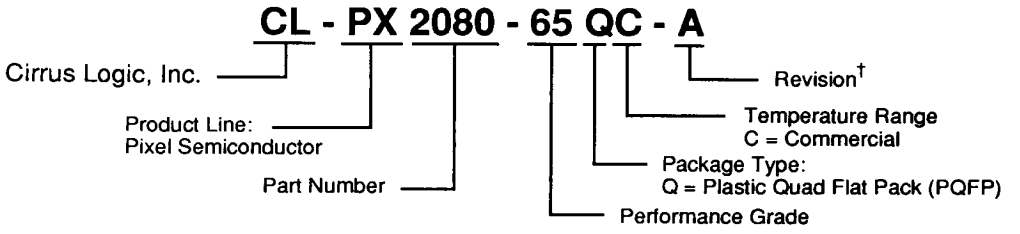


Figure 6–2. CL-PX2080 Package Information (Expanded View)

7. ORDERING INFORMATION

When ordering the CL-PX2080, use the following format:



† Contact Cirrus Logic for up-to-date information on revisions.

Appendix A. CL-PX2080 REGISTER MAP

Reg.	Addresses Local	Prim.	Sec.	Blk	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Memory Access Addressing and Indexing												
BIR	N/A	0x27CE	0x29E	N/A	IE	RE	SE	RO	RSVD	BLK		
Graphics Color Palette Registers (VGA Mode 0 and 1)												
LAW	0x00	0x03C8	N/A	N/A	Color LUT Write Address							
LCD	0x01	0x03C9	N/A	N/A	Color LUT Data							
LPM	0x02	0x03C6	N/A	N/A	Color LUT Pixel Mask Data							
LAR	0x03	0x03C7	N/A	N/A	Color LUT Read Address							
Graphics Color Palette Register (VGA Mode 2)												
LAW	0x00	0x27CC	0x029C	0	Color LUT Write Address							
LCD	0x01	0x27CD	0x029D	0	Color LUT Data							
LPM	0x02	0x27CA	0x029A	0	Color LUT Pixel Mask Data							
LAR	0x03	0x27CB	0x029B	0	Color LUT Read Address							
Cursor Color and Analog Setup Registers												
CAW	0x04	0x27CC	0x029C	1	RSVD						Cursor Wr Adr	
CCD	0x05	0x27CD	0x029D	1	Color Data							
ASC	0x06	0x27CA	0x029A	1	RSVD	COFF	RSVD				D24	DOFF
CAR	0x07	0x27CB	0x029B	1	RSVD						Cursor Rd Adr	
Graphic and Cursor Setup Registers												
GFC	0x08	0x27CC	0x029C	2	RSVD	GPF		TC	CF	MR	TE	PS
CSC	0x09	0x27CD	0x029D	2	SD	GPS		CS	DM	PM	CMS	
GSR	0x0A	0x27CA	0x029A	2	REV				S	IO	CP	
CPR	0x0B	0x27CB	0x029B	2	Cursor Pattern RAM Data							

Reg.	Addresses Local	Prim.	Sec.	Blk	Bit Assignments Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Cursor Positioning Registers												
CXL	0x0C	0x27CC	0x029C	3	Cursor X Position Low Byte							
CXH	0x0D	0x27CD	0x029D	3	RSVD				Cur X Pos H Nibble			
CYL	0x0E	0x27CA	0x029A	3	Cursor Y Position Low Byte							
CYH	0x0F	0x27CB	0x029B	3	RSVD				Cur Y Pos H Nibble			
Video, Graphics and Sync Control Registers												
VFC	0x10	0x27CC	0x029C	4	EC	CS	RSVD	GBYP	CSF			
GOC	0x11	0x27CD	0x029D	4	T (Transparency)							
SAR	0x12	0x27CA	0x029A	4	HP	HL	VP	VL	DIR	DLY		
RSV1	0x13	0x27CB	0x029B	4	GT	CT	LC	PO	SO	WO	KO	BE
Video Gamma Correction Palette Registers												
VGW	0x14	0x27CC	0x029C	5	Video Gamma Correction Write Address							
VGD	0x15	0x27CD	0x029D	5	Video Gamma Correction Data							
RSV2	0x16	0x27CA	0x029A	5	RSVD							
VGR	0x17	0x27CB	0x029B	5	Video Gamma Correction Read Address							
Graphics Chroma Key Registers												
GCKR	0x18	0x27CC	0x029C	6	Graphics Chroma Key Red Data							
GCKG	0x19	0x27CD	0x029D	6	Graphics Chroma Key Green Data							
GCKB	0x1A	0x27CA	0x029A	6	Graphics Chroma Key Blue Data							
RSV3	0x1B	0x27CB	0x029B	6	RSVD							
GKMR	0x1C	0x27CC	0x029C	7	Graphics Chroma Key Mask Red Data							
GKMG	0x1D	0x27CD	0x029D	7	Graphics Chroma Key Mask Green Data							
GKMB	0x1E	0x27CA	0x029A	7	Graphics Chroma Key Mask Blue Data							
Rsv4	0x1F	0x27CB	0x029B	7	RSVD							

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The Company

Cirrus Logic, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation.

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Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

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