Clock Distributor with Enable and 10 Differential Outputs

Description

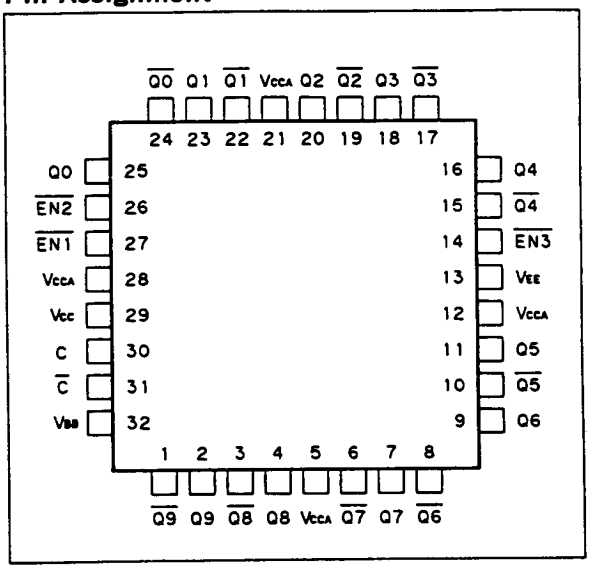
The CXB1515Q-Y is an ultra high speed monolithic clock distributor, with low skew (80ps typ.). Clock input has differential input pins C and $\overline{C}$. The input signal is fanned out to 10 differential outputs.

Enable inputs ($\overline{EN1}$-$\overline{EN3}$) control clock inputs. Built-in reference voltage is provided at V_{BB} pin to facilitate the use of single input operation.

Features

- Small gate-to-gate skew: 80ps (typ.)
- Differential clock input and output
- Built-in reference voltage for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

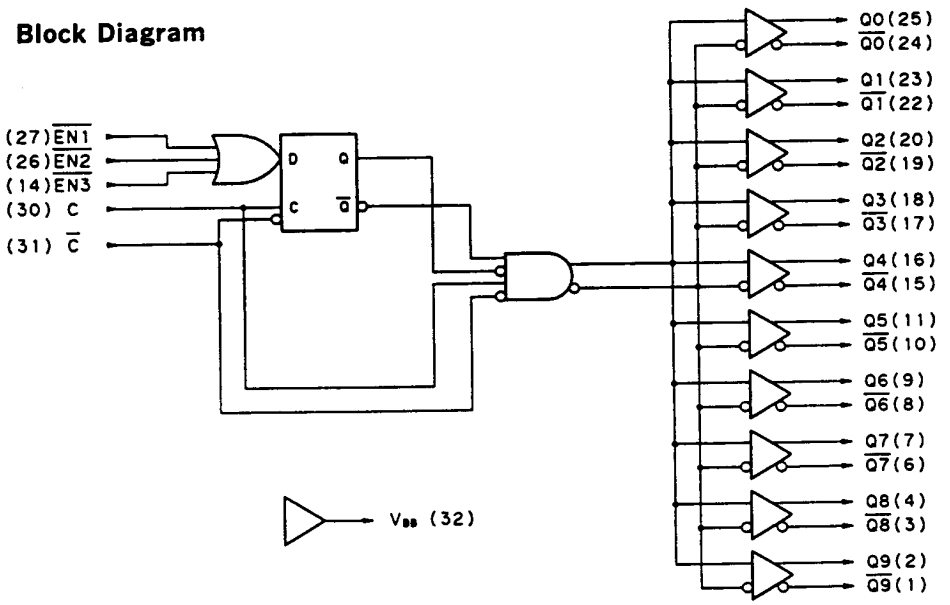
Pin Assignment



Pin Names

C, $\overline{C}$	Clock inputs
Qn, $\overline{Qn}$	Clock outputs
$\overline{ENn}$	Clock enables (active LOW)
V_{BB}	Reference voltage output
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Block Diagram



DC Characteristics

V_{EE} = −4.5V±0.3V, V_{CC}=V_{CCA}=GND, V_{TT} = −2.0V, T_C=0°C to +85°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−244	−178	−124	mA

AC Characteristics

V_{EE} = −4.5V±0.3V, V_{CC}=V_{CCA}=GND, V_{TT} = −2.0V, T_C=0°C to +85°C, R_T=50Ω to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation Delay time	T_{PLH}	C	Qn		570	810	1070	ps
	T_{PHL}				570	810	1070	
Gate-to-Gate Skew	T_{SG-G}					80	150	
Set up time	Ts				150			
Hold time	Th				260			
Rise time	T_{TLH}			20% to 80%		230	330	
Fall time	T_{THL}					230	330	