

8/9/10-BIT BUS INTERFACE REGISTERS

FEATURES

- Function, Pinout and Drive Compatible with the FCT, F and Am29821/23/25 Logic
- FCT-C speed at 6.0ns max. (Com'I)
FCT-B speed at 7.5ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'I), 32 mA (Mil)
15 mA Source Current (Com'I), 12 mA (Mil)
- High-Speed Parallel Registers with positive edge-triggered D-type Flip-Flops
- Buffered Common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input (CLR)

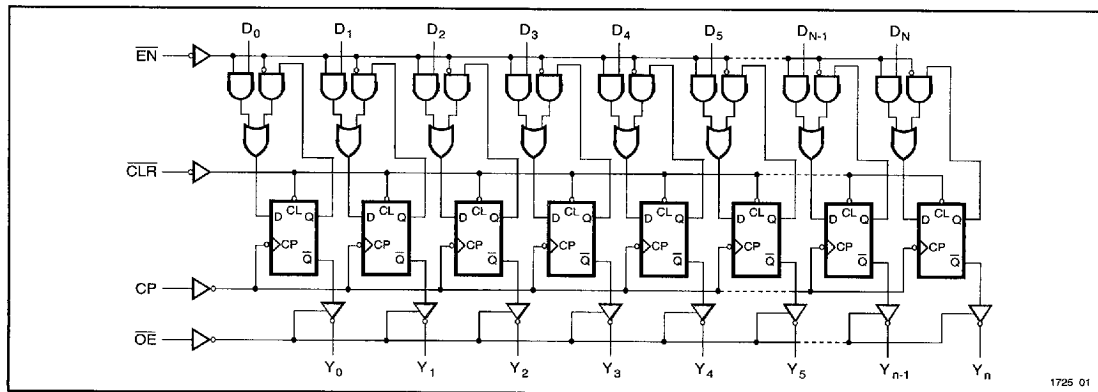
DESCRIPTION

The 'FCT820T series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT821T is a buffered, 10 bit wide version of the popular 'FCT374 function. The 'FCT823T is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The 'FCT825T is a 8-bit buffered register with all the 'FCT823T controls plus multiple enables ($\overline{OE}_1, \overline{OE}_2$,

$\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/WR. They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

The 'FCT800T family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



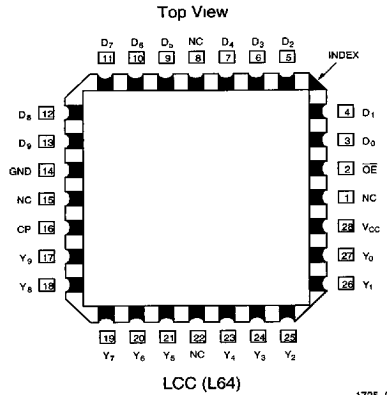
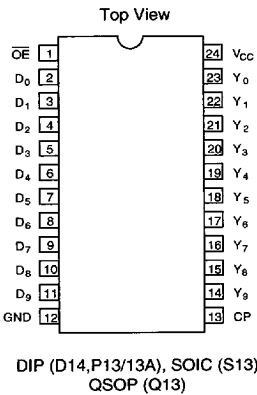
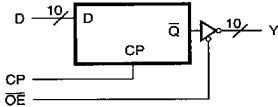
PRODUCT SELECTOR GUIDE

Non-inverting	Device		
	10-Bit	9-Bit	8-Bit
	'FCT821T	'FCT823T	'FCT825T

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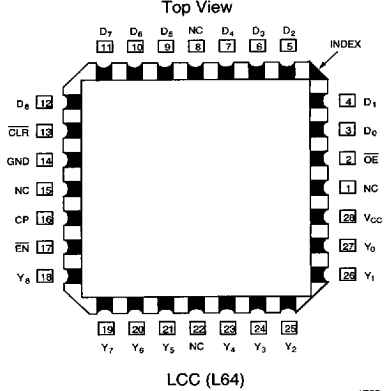
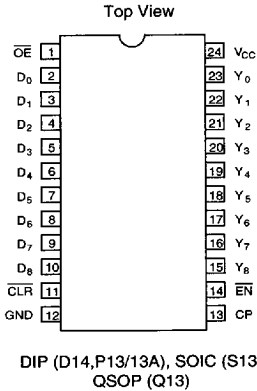
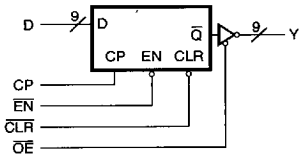
LOGIC SYMBOLS

'FCT821T (10-Bit Register)



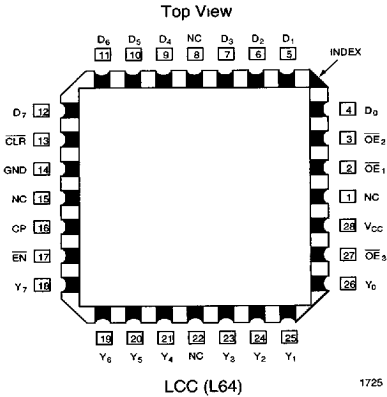
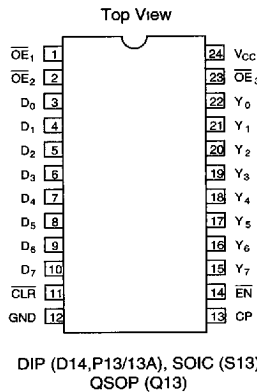
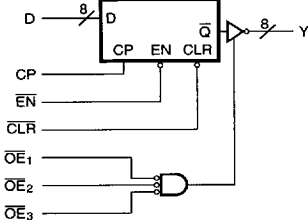
1725 02

'FCT823T (9-Bit Register)



1725 03

'FCT825T (8-Bit Register)



1725 04

ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Ambient Temperature Under Bias	-65 to +135	°C
V _{CC}	V _{CC} Potential to Ground	-0.5 to +7.0	V
P _T	Power Dissipation	0.5	W

Notes: 1725 Tbl 02

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I _{OUTPUT}	Current Applied to Output	120	mA
V _{IN}	Input Voltage	-0.5 to +7.0	V
V _{OUT}	Voltage Applied to Output	-0.5 to +7.0	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V _{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ ¹	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		
V _{IL}	Input LOW Voltage				0.8	V		
V _H	Hysteresis			0.2		V		All inputs
V _{IK}	Input Clamp Diode Voltage			−0.7	−1.2	V	MIN	I _{IN} = −18mA
V _{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I _{OH} = −12mA
		Commercial	2.4	3.3		V	MIN	I _{OH} = −15mA
V _{OL}	Output LOW Voltage	Military Commercial Commercial		0.3	0.5	V	MIN	I _{OL} = 32mA
				0.3	0.5	V	MIN	I _{OL} = 48mA
				0.3	0.5	V	MIN	I _{OL} = 64mA
I _I	Input HIGH Current				20	μA	MAX	V _{IN} = V _{CC}
I _{IH}	Input HIGH Current				5	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current				−5	μA	MAX	V _{IN} = 0.5V
I _{OZH}	Off State I _{OUT} HIGH-Level Output Current				10	μA	MAX	V _{OUT} = 2.7V
I _{OZL}	Off State I _{OUT} LOW-Level Output Current				−10	μA	MAX	V _{OUT} = 0.5V
I _{OS}	Output Short Circuit Current ²		−60	−120	−225	mA	MAX	V _{OUT} = 0.0V
I _{OFF}	Power-off Disable				100	μA	0V	V _{OUT} = 4.5V
C _{IN}	Input Capacitance ³			6	10	pF	MAX	All inputs
C _{OUT}	Output Capacitance ³			8	12	pF	MAX	All outputs
I _{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	V _{IN} ≤ 0.2V, V _{IN} ≥ V _{CC} − 0.2V

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Notes:

- Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs) ³	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_i = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.25	mA/ MHz	$V_{CC} = \text{MAX}$, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	1.7	4.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_i = 5\text{MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_i = 5\text{MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		4.0	7.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_i = 2.5\text{MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_i = 2.5\text{MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

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Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_i N_i)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

- D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Sym.	Parameter	Test Conditions	'FCT821AT-825AT				'FCT821BT-825BT				'FCT821CT-825CT				Units	Fig. No.*
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Y ₁ (OE = LOW)	C _L = 50pF R _L = 500Ω	-	11.5	-	10.0	-	8.5	-	7.5	-	7.0	-	6.0	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay CP to Y ₁ (OE = LOW)	C _L = 300pF ² R _L = 500Ω	-	20.0	-	20.0	-	16.0	-	15.0	-	13.5	-	12.5	ns	1,5
t_{PLH}	Propagation Delay CLR to Y ₁	C _L = 50pF R _L = 500Ω	-	15.0	-	14.0	-	9.5	-	9.0	-	8.5	-	8.0	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time OE to Y ₁	C _L = 50pF R _L = 500Ω	-	13.0	-	12.0	-	9.0	-	8.0	-	8.0	-	7.0	ns	1,7,8
t_{PZH} t_{PZL}	Output Enable Time OE to Y ₁	C _L = 300pF ² R _L = 500Ω	-	25.0	-	23.0	-	16.0	-	15.0	-	13.5	-	12.5	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time OE to Y ₁	C _L = 5pF ² R _L = 500Ω	-	8.0	-	7.0	-	7.0	-	6.5	-	6.2	-	6.2	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time OE to Y ₁	C _L = 50pF R _L = 500Ω	-	9.0	-	8.0	-	8.0	-	7.5	-	6.5	-	6.5	ns	1,7,8

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AC OPERATING REQUIREMENTS

Sym.	Parameter	Test Conditions	'FCT821AT-825AT				'FCT821BT-825BT				'FCT821CT-825CT				Units	Fig. No.*
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t _{SU}	Data to CP Set-up Time	C _L = 50pF R _L = 500Ω	4.0	–	4.0	–	3.0	–	3.0	–	3.0	–	3.0	–	ns	4
t _n	Data CP Hold Time		2.0	–	2.0	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	4
t _{SU}	Enable $\overline{EN}$ to CP Set-up Time		4.0	–	4.0	–	3.0	–	3.0	–	3.0	–	3.0	–	ns	9
t _n	Enable $\overline{EN}$ to CP Hold Time		2.0	–	2.0	–	0.0	–	0.0	–	0.0	–	0.0	–	ns	9
t _{REM}	Clear Recovery Time $\overline{CLR}$ to CP		7.0	–	6.0	–	6.0	–	6.0	–	6.0	–	6.0	–	ns	6
t _w	Clock Pulse Width		7.0	–	7.0	–	6.0	–	6.0	–	6.0		6.0	–	ns	5
t _w	$\overline{CLR}$ Pulse Width LOW		7.0	–	6.0	–	6.0	–	6.0	–	6.0		6.0	–	ns	5

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays

2. These parameters are guaranteed but not tested.

* See "Parameter Measurement Information" in the General Information Section.

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PIN DESCRIPTION

Name	I/O	Description
D ₁	I	The D flip-flop data inputs.
$\overline{\text{CLR}}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{\text{OE}}$ is LOW, the Q ₁ outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y ₁ , $\overline{\text{Y}}_1$	O	The register three-state outputs.
$\overline{\text{EN}}$	I	Clock Enable. When the clock enable is LOW, data on the D ₁ input is transferred to the Q ₁ output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q ₁ outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When the $\overline{\text{OE}}$ input is HIGH, the Y ₁ outputs are in the high impedance state. When the $\overline{\text{OE}}$ input is LOW, the TRUE register data is present at the Y ₁ outputs.

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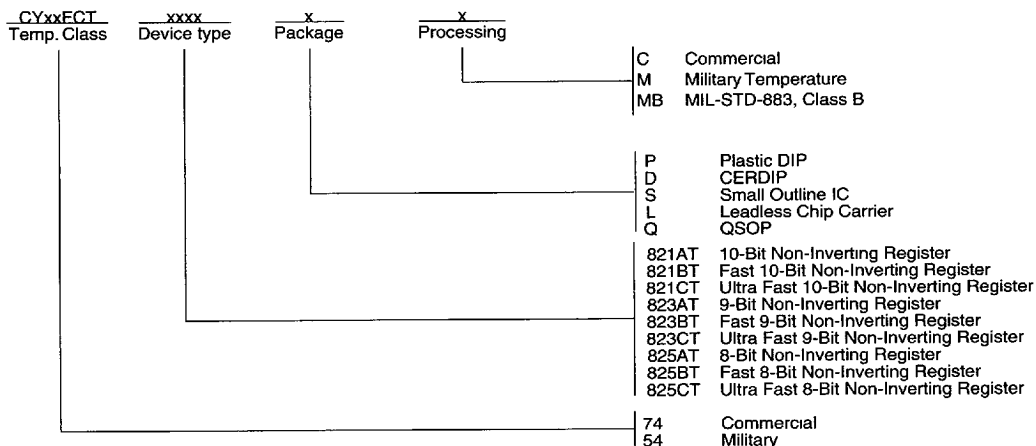
FUNCTION TABLES

Inputs					Internal Outputs		Function
$\overline{\text{OE}}$	CLR	EN	D ₁	CP	Q ₁	Y ₁	
H	H	L	L	$\uparrow$	L	Z	High Z
H	H	L	H	$\uparrow$	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	$\uparrow$	L	Z	Load
H	H	L	H	$\uparrow$	H	Z	
L	H	L	L	$\uparrow$	L	L	
L	H	L	H	$\uparrow$	H	H	

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H = HIGH, L = LOW, X = Don't Care, NC = No Change,
 $\uparrow$ = LOW-to-HIGH Transition, Z = HIGH Impedance

ORDERING INFORMATION



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