



1024K x 8 MoBL Static RAM

Features

- **High Speed**
 - 55 ns and 70 ns Availability
- **Voltage range:**
 - CY62158CV25: 2.2V–2.7V
 - CY62158CV30: 2.7V–3.3V
 - CY62158CV33: 3.0V–3.6V
- **Ultra low active power**
 - Typical active current: 1 mA @ f = 1 MHz
 - Typical active current: 7 mA @ f = f_{max} (70 ns speed)
- **Low standby power**
- **Easy memory expansion with $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The CY62158CV25/30/33 are high-performance CMOS static RAMs organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™)

in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}_1$ HIGH or $\overline{CE}_2$ LOW).

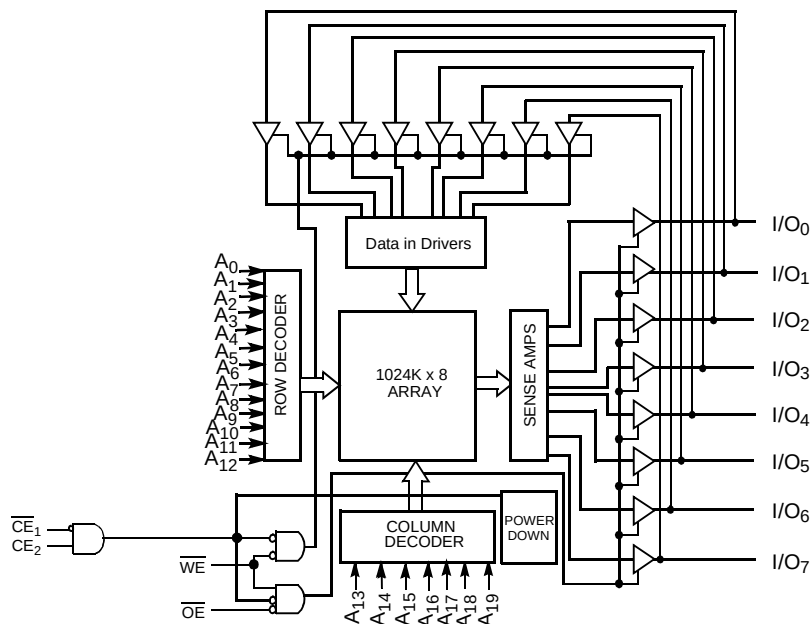
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH and $\overline{WE}$ LOW).

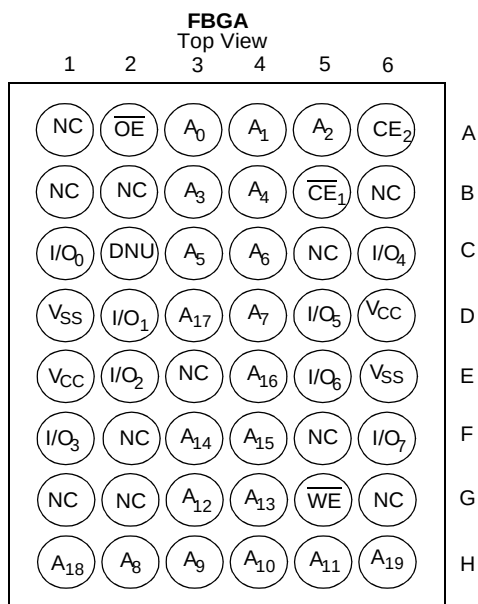
The CY62158CV25/30/33 are available in a 48-ball FBGA package.

Logic Block Diagram



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Pin Configurations ^[1, 2]



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature-65°C to +150°C

Ambient Temperature with

Power Applied55°C to +125°C

Supply Voltage to Ground Potential ...-0.5V to V_{CCmax} + 0.5V

DC Voltage Applied to Outputs

in High Z State^[3] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[3]-0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage>2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current>200 mA

Operating Range

Product	Range	Ambient Temperature	V _{CC}
CY62158CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62158CV30			2.7V to 3.3V
CY62158CV33			3.0V to 3.6V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating (I _{CC})				Standby (I _{SB2})	
					f = 1 MHz		f = f _{max}			
	Min.	Typ. ^[4]	Max.		Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.
CY62158CV25	2.2V	2.5V	2.7V	55 ns	1.5 mA	3 mA	12 mA	25 mA	6 μA	25 μA
				70 ns	1.5 mA	3 mA	7 mA	15 mA		
CY62158CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	12 mA	25 mA	8 μA	25 μA
				70 ns	1.5 mA	3 mA	7 mA	15 mA		
CY62158CV33	3.0V	3.3V	3.6V	55 ns	1.5 mA	3 mA	12 mA	25 mA	10 μA	30 μA
				70 ns	1.5 mA	3 mA	7 mA	15 mA		

Notes:

- NC pins are not connected to the die.
- C2 (DNU) can be left as NC or V_{SS} to ensure proper application.
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62158CV25-55			CY62158CV25-70			Unit
				Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = −0.1 mA	V _{CC} = 2.2V	2.0			2.0			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 2.2V			0.4			0.4	V
V _{IH}	Input HIGH Voltage			1.8		V _{CC} +0.3V	1.8		V _{CC} +0.3V	V
V _{IL}	Input LOW Voltage			−0.3		0.6	−0.3		0.6	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		−1		+1	−1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		−1		+1	−1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 2.7V I _{OUT} = 0 mA CMOS Levels		12	25		7	15	mA
		f = 1 MHz			1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	CE ₁ ≥ V _{CC} − 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} − 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f=0 (OE,WE)			6	25		6	25	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	CE ₁ ≥ V _{CC} − 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} − 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 2.7V								

Parameter	Description	Test Conditions		CY62158CV30-55			CY62158CV30-70			Unit
				Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V			0.4			0.4	V
V _{IH}	Input HIGH Voltage			2.2		V _{CC} +0.3V	2.2		V _{CC} +0.3V	V
V _{IL}	Input LOW Voltage			−0.3		0.8	−0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		−1		+1	−1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		−1		+1	−1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.3V I _{OUT} = 0 mA CMOS Levels		12	25		7	15	mA
		f = 1 MHz			1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	CE ₁ ≥ V _{CC} − 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} − 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f=0 (OE, WE)			8	25		8	25	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	CE ₁ ≥ V _{CC} − 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} − 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.3V								

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62158CV33-55			CY62158CV33-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 3.0V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 3.0V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} f = 1 MHz		12	25		7	15	mA
		V _{CC} = 3.6V I _{OUT} = 0 mA CMOS Levels		1	2		1	2	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = f _{max} (Address and Data Only), f=0 (OE, WE)		10	30		10	30	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} = 3.6V							

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)}	6	pF
C _{OUT}	Output Capacitance		8	pF

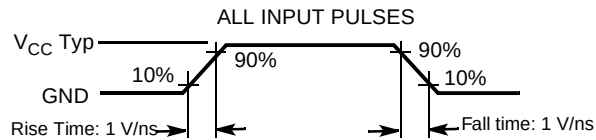
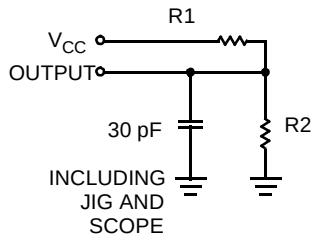
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance ^[5] (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ _{JA}	55	°C/W
Thermal Resistance ^[5] (Junction to Case)		θ _{JC}	16	°C/W

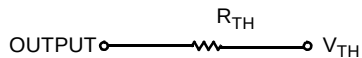
Note:

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

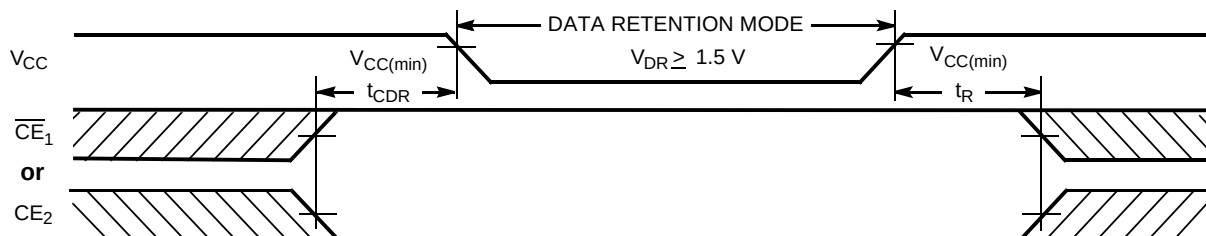


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	K Ω
R2	15.4	1.550	1.374	K Ω
R_{TH}	8	0.645	0.645	K Ω s
V_{TH}	1.20	1.75	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5		V_{CCmax}	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5V$ $CE_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		4	20	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[6]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Note:

- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100 \mu s$ or stable at $V_{CC(min.)} \geq 100 \mu s$.

Switching Characteristics Over the Operating Range^[7]

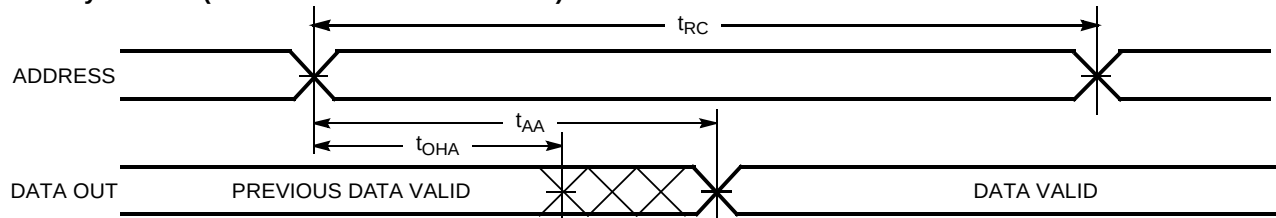
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[8]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[8, 9]		20		25	ns
t _{LZCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Low Z ^[8]	10		10		ns
t _{HZCE}	$\overline{CE}_1$ HIGH or CE ₂ LOW to High Z ^[8, 9]		20		25	ns
t _{PU}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Power-Up	0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH or CE ₂ LOW to Power-Down		55		70	ns
WRITE CYCLE ^[10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[8, 9]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[8]	5		5		ns

Notes:

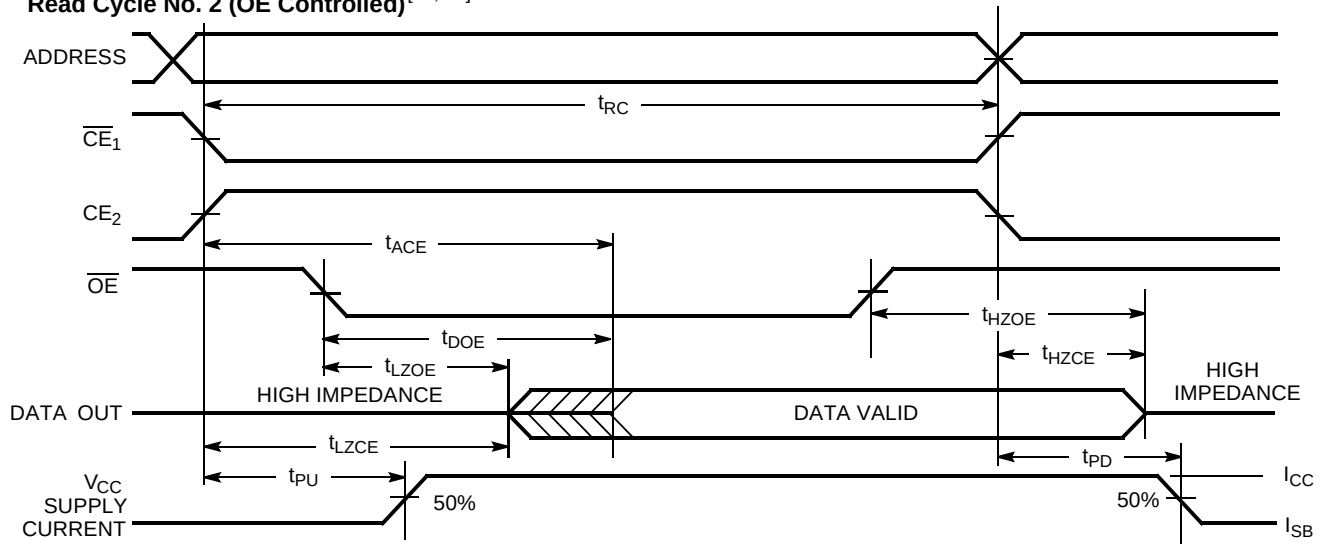
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of $\overline{WE}$, $CE = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[11, 12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)^[12, 13]

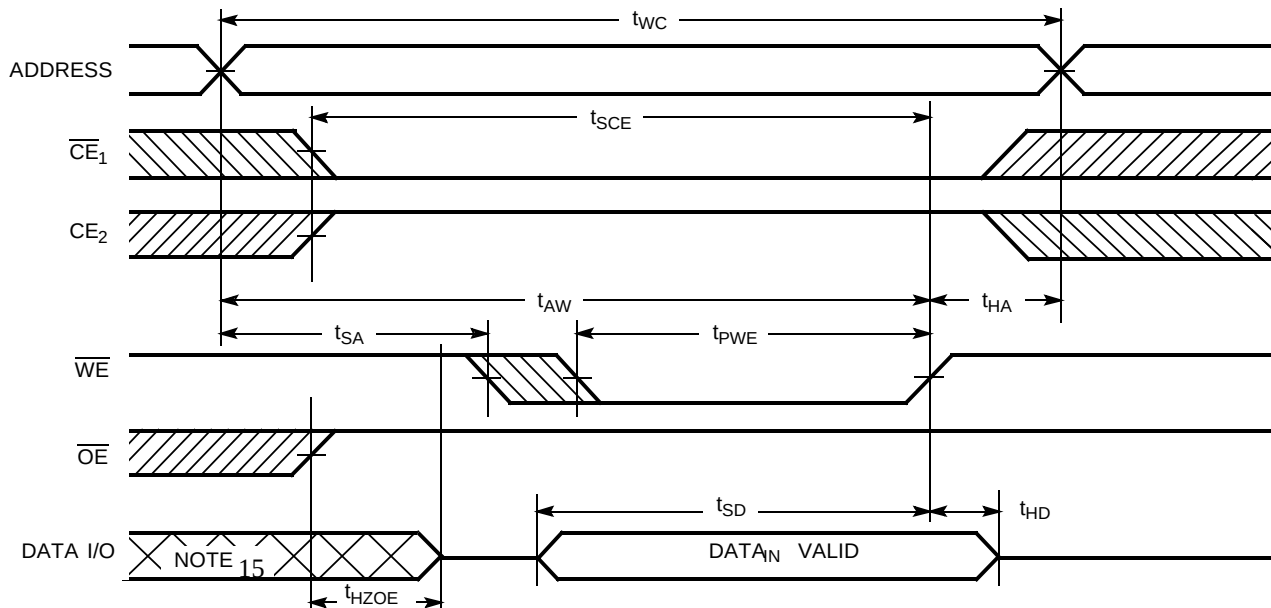


Notes:

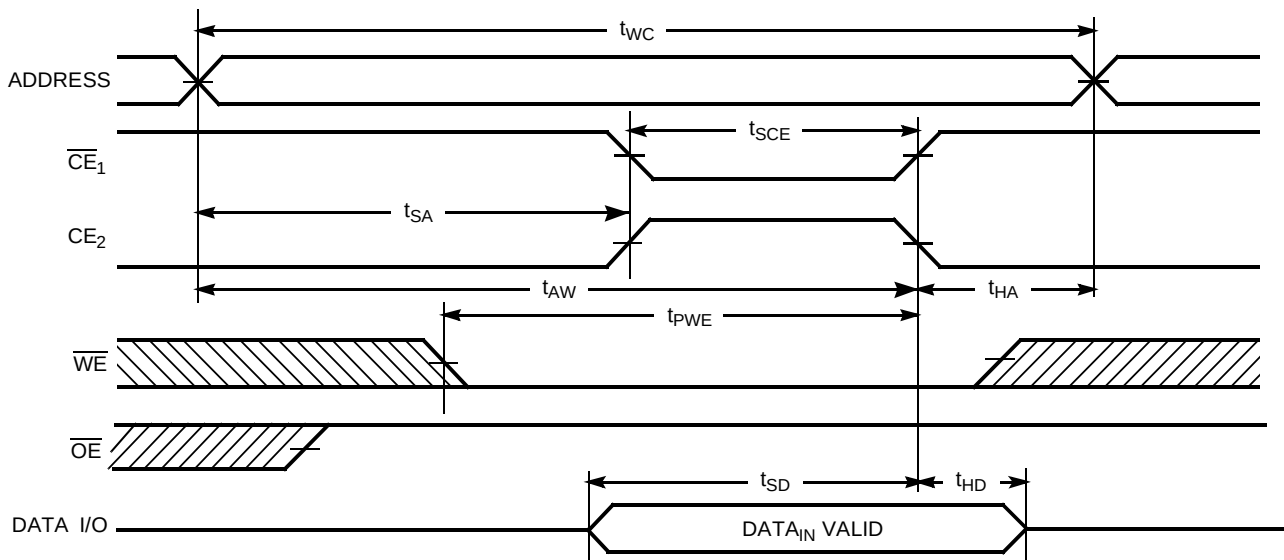
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms

Write Cycle No. 1(WE Controlled) [10, 14, 16]



Write Cycle No. 2($\overline{CE}_1$ or CE_2 Controlled) [10, 14, 16]

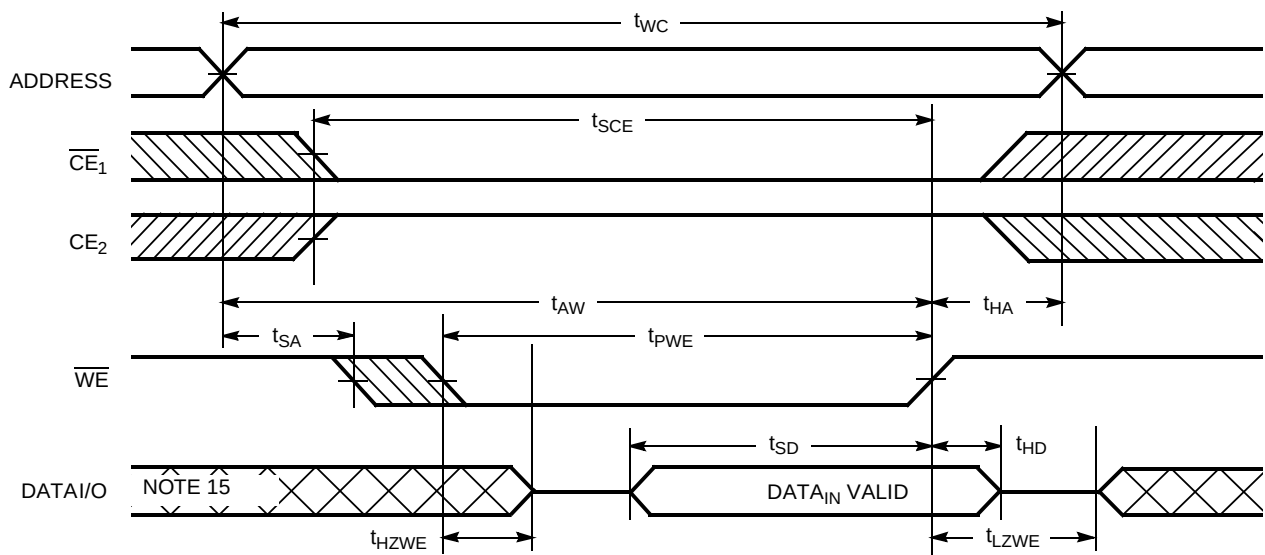


Notes:

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. During this period, the I/Os are in output state and input signals should not be applied.
16. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.

Switching Waveforms

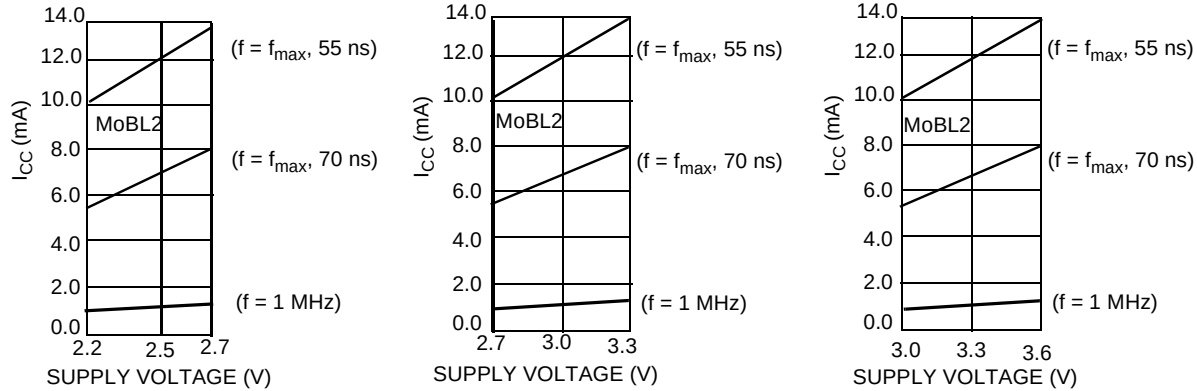
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) ^[16]



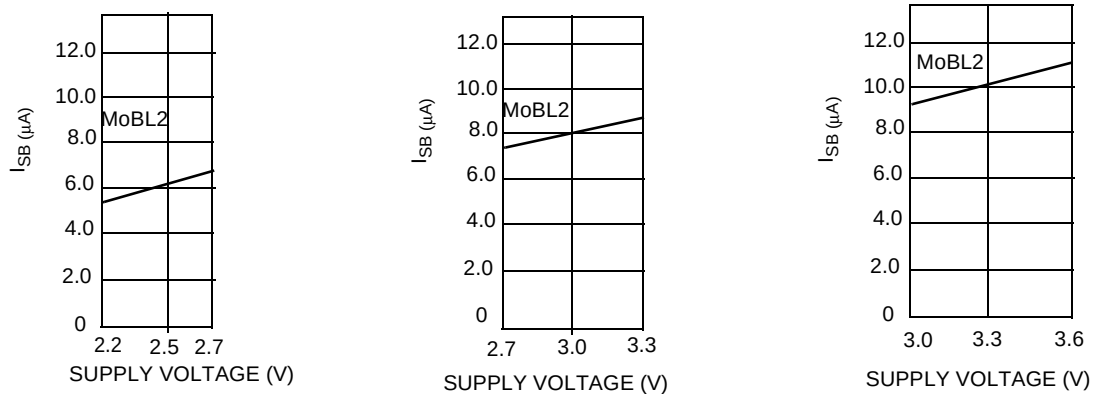
Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^\circ\text{C}$.)

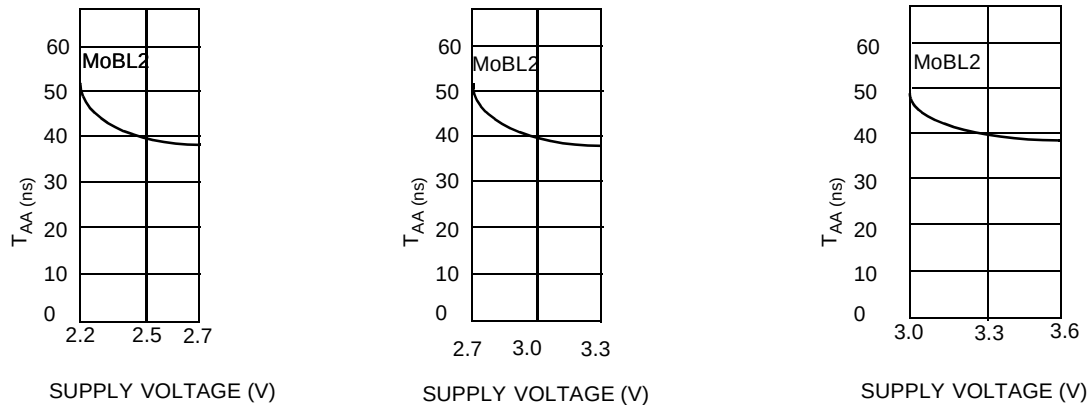
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

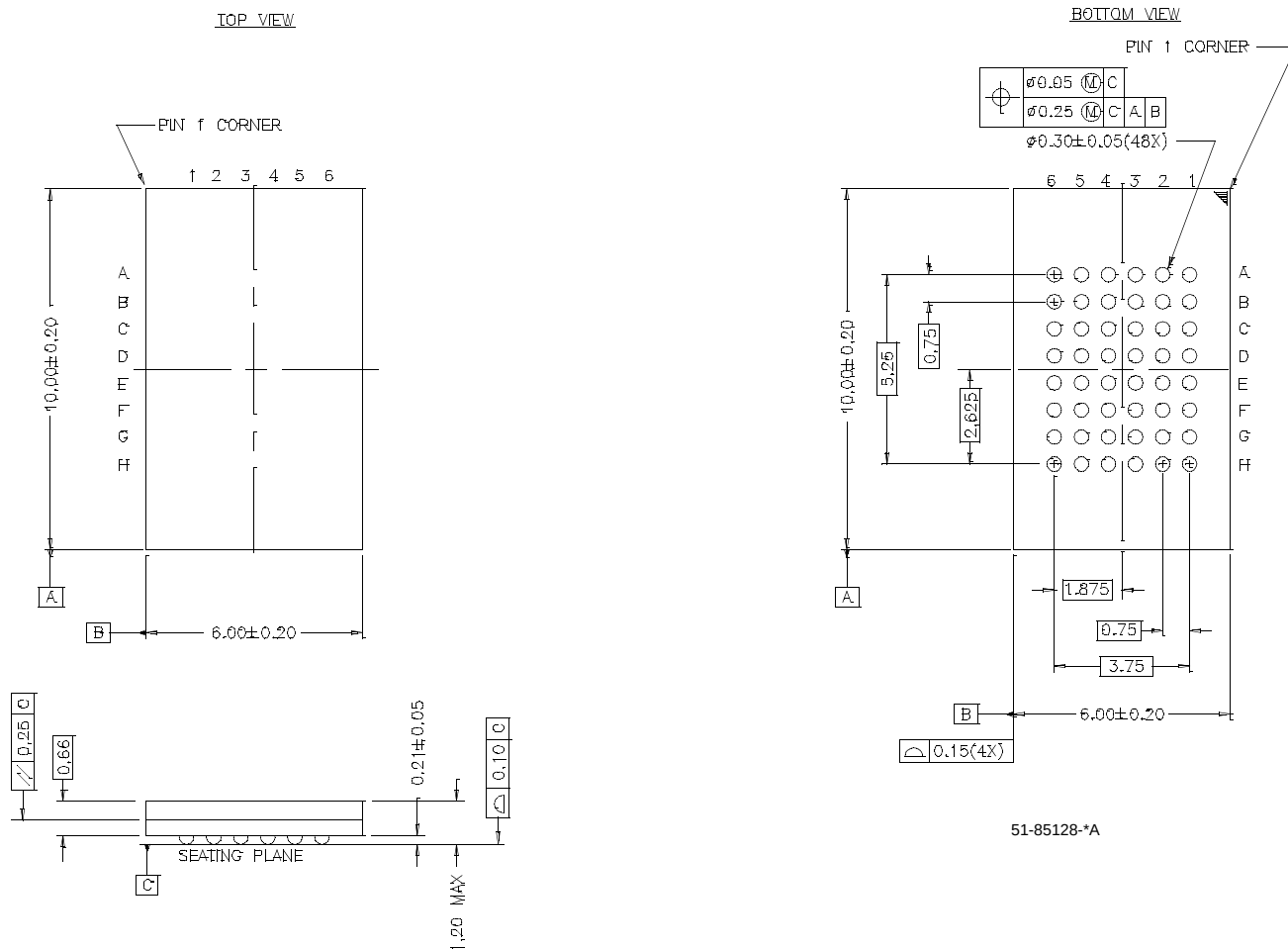
CE_1	CE_2	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	Data Out (I/O_0 - I/O_7)	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in (I/O_0 - I/O_7)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62158CV25LL-70BAI	BA48F	48-Ball Fine Pitch BGA	Industrial
	CY62158CV30LL-70BAI			
	CY62158CV33LL-70BAI			
55	CY62158CV25LL-55BAI			
	CY62158CV30LL-55BAI			
	CY62158CV33LL-55BAI			

Package Diagrams

48-Ball (6 mm x 10 mm x 1.2 mm) FBGA BA48F





Document Title: CY62158CV25/30/33 MoBL™, 1024K x 8 MoBL Static RAM Document Number: 38-05019				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106361	05/22/01	MGN	New Data Sheet - Advance Information
*A	107773	07/16/01	MGN	Add 55 ns Bin to Advance Information
*B	111945	11/27/01	GAV	Advance to Final