National Semiconductor Corporation

PRELIMINARY

DM54ALS1645A/DM74ALS1645A Octal TRI-STATE® Bus Transceivers

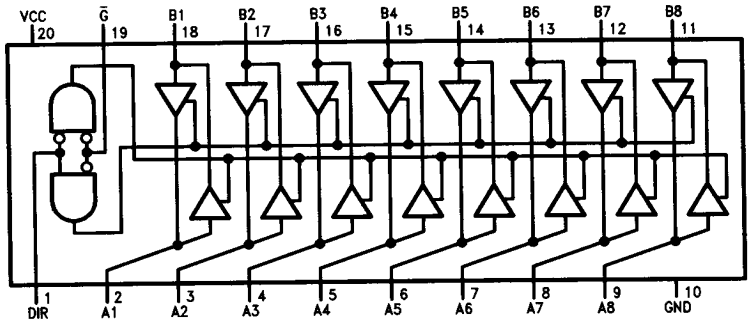
General Description

This device contains eight pairs of TRI-STATE logic elements configured as octal bus transceivers. This device is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the direction (DIR) input. Data either transmits from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled by the enable (G) input which causes outputs to enter the high impedance mode, so that the buses are effectively isolated.

Features

- Low power version of the ALS645A
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- PNP input design reduces input loading
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching specifications guaranteed over the full temperature and V_{CC} range

Connection Diagram



TL/F/9164–1

Order Number DM54ALS1645AJ, DM74ALS1645AWM or DM74ALS1645AN
See NS Package Number J20A, M20A or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

L = Low Logic Level
H = High Logic Level
X = Don't Care (Either Low or High Logic Level)
Hi-Z = High Impedance

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1645A			DM74ALS1645A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		DM54ALS1645A			DM74ALS1645A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max			25	40		25	36	mA

Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state currents. (I_{OZH}, I_{OZL})

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS1645A		DM74ALS1645A		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_1 = 500Ω, R_2 = 500Ω, C_L = 50 pF	A or B to B or A	2	15	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	2	15	2	13	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	8	28	8	25	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	8	28	8	25	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	2	14	2	12	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$ to A or B	3	22	3	18	ns

Note 1: See Section 1 for test waveforms and output load.