National Semiconductor

DM74LS645 Octal Bus Transceivers

General Description

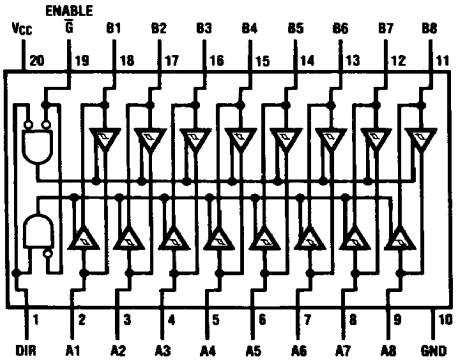
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-directional bus transceivers in high-density 20-pin packages
- Hysteresis at bus inputs improves noise margins
- TRI-STATE® outputs

Connection Diagram

Dual-In-Line Package



TL/F/9056–1

Order Number DM74LS645WM or DM74LS645N
See NS Package Number M20B or N20A

Function Table

Control Inputs		'LS645
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level
L = Low Level
X = Irrelevant

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS645			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage (Note 1)	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.6	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 2)			Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = 18 mA					−1.5	V
H_{YS}	Hysteresis ($V_{T+} - V_{-}$) A or B Input	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max		I_{OH} = −3 mA	2.4	3.4		V
				I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max		I_{OL} = 12 mA		0.25	0.4	V
				I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, G at 2V, V_O = 2.7V					20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = Max, G at 2V V_O = 0.4V					−400	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or G	V_I = 7V			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.4V					−0.4	mA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max			−40		−225	mA
I_{CC}	Total Supply Current	Outputs High		V_{CC} = Max, Outputs Open		48	70	mA
		Outputs Low				62	90	
		Outputs at Hi-Z				64	95	

Note 1: Voltage values are with respect to the network ground terminal.

Note 2: For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 5 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to B		15			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to B		15			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to A		15			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to A		15			ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$ to A		40			ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$ to A		40			ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$ to B		40			ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$ to B		40			ns
t_{PLZ}	Output Disable Time to Low Level	$\overline{G}$ to A				25	ns
t_{PHZ}	Output Disable Time to High Level	$\overline{G}$ to A				25	ns
t_{PLZ}	Output Disable Time to Low Level	$\overline{G}$ to B				25	ns
t_{PHZ}	Output Disable Time to High Level	$\overline{G}$ to B				25	ns