HM6216255HCI Series

Wide Temperature Range Version
4M High Speed SRAM (256-kword × 16-bit)

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Description

The HM6216255HCI Series is a 4-Mbit high speed static RAM organized 256-k word × 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 44-pin plastic SOJ and 400-mil 44-pin plastic TSOPII.

Features

- Single 5.0 V supply: 5.0 V ± 10%
- Access time: 12 ns (max)
- Completely static memory
  — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  — All inputs and outputs
- Operating current: 160 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
- Center V_{cc} and V_{ss} type pin out
- Temperature range: −40 to +85°C

Ordering Information

| Type No.	Access time	Device marking	Package
HM6216255HCJPI-12	12 ns	HM6216255CJPI12	400-mil 44-pin plastic SOJ (CP-44D)
HM6216255HCTTI-12	12 ns	HM6216255CTTI12	400-mil 44-pin plastic TSOPII (TTP-44DE)

Pin Arrangement

44-pin SOJ

A0	1	44	A17
A1	2	43	A16
A2	3	42	A15
A3	4	41	$\overline{OE}$
A4	5	40	$\overline{UB}$
$\overline{CS}$	6	39	$\overline{LB}$
I/O1	7	38	I/O16
I/O2	8	37	I/O15
I/O3	9	36	I/O14
I/O4	10	35	I/O13
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O5	13	32	I/O12
I/O6	14	31	I/O11
I/O7	15	30	I/O10
I/O8	16	29	I/O9
$\overline{WE}$	17	28	NC
A5	18	27	A14
A6	19	26	A13
A7	20	25	A12
A8	21	24	A11
A9	22	23	A10

(Top View)

44-pin TSOP

A0	1	44	A17
A1	2	43	A16
A2	3	42	A15
A3	4	41	$\overline{OE}$
A4	5	40	$\overline{UB}$
$\overline{CS}$	6	39	$\overline{LB}$
I/O1	7	38	I/O16
I/O2	8	37	I/O15
I/O3	9	36	I/O14
I/O4	10	35	I/O13
VCC	11	34	VSS
VSS	12	33	VCC
I/O5	13	32	I/O12
I/O6	14	31	I/O11
I/O7	15	30	I/O10
I/O8	16	29	I/O9
$\overline{WE}$	17	28	NC
A5	18	27	A14
A6	19	26	A13
A7	20	25	A12
A8	21	24	A11
A9	22	23	A10

(Top View)

Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{UB}$	Upper byte select
$\overline{LB}$	Lower byte select
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

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Block Diagram

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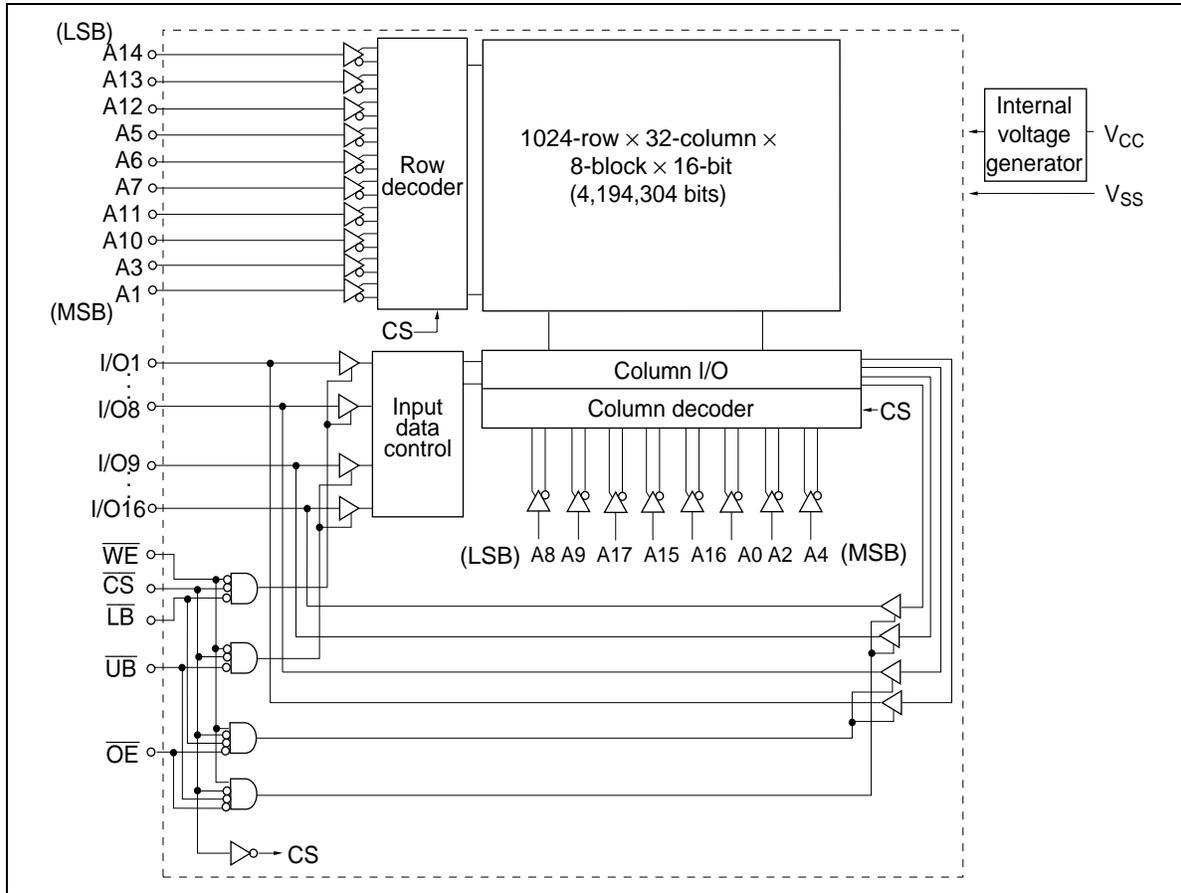
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Operation Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	V_{cc} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	×	×	×	×	Standby	I_{SB}, I_{SB1}	High-Z	High-Z	—
L	H	H	×	×	Output disable	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	Read	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	—	I_{CC}	High-Z	High-Z	—
L	×	L	L	L	Write	I_{CC}	Input	Input	Write cycle
L	×	L	L	H	Lower byte write	I_{CC}	Input	High-Z	Write cycle
L	×	L	H	L	Upper byte write	I_{CC}	High-Z	Input	Write cycle
L	×	L	H	H	—	I_{CC}	High-Z	High-Z	—

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	−0.5[*1] to V_{CC} + 0.5[*2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−40 to +85	°C

Notes: 1. V_T (min) = −2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_T (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.

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Recommended DC Operating Conditions

(Ta = −40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*[3]	4.5	5.0	5.5	V
	V_{SS}*[4]	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5*[2]	V
	V_{IL}	−0.5*[1]	—	0.8	V

Notes: 1. V_{IL} (min) = −2.0 V for pulse width (under shoot) ≤ 6 ns.
2. V_{IH} (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.
3. The supply voltage with all V_{CC} pins must be on the same level.
4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

(Ta = −40 to +85°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$|I_{LI}|$	—	—	2	μA	V_{IN} = V_{SS} to V_{CC}
Output leakage current*[1]	$|I_{LO}|$	—	—	2	μA	V_{IN} = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	160	mA	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA Other inputs = V_{IH}/V_{IL}
Standby power supply current	I_{SB}	—	—	40	mA	$\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}
	I_{SB1}	—	2.5	5	mA	V_{CC} ≥ $\overline{CS}$ ≥ V_{CC} − 0.2 V, (1) 0 V ≤ V_{IN} ≤ 0.2 V or (2) V_{CC} ≥ V_{IN} ≥ V_{CC} − 0.2 V
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

| Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	C_{IN}	—	—	6	pF	V_{IN} = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics

(Ta = −40 to +85°C, V_{CC} = 5.0 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)

Output load (A)

Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, and t_{OW})
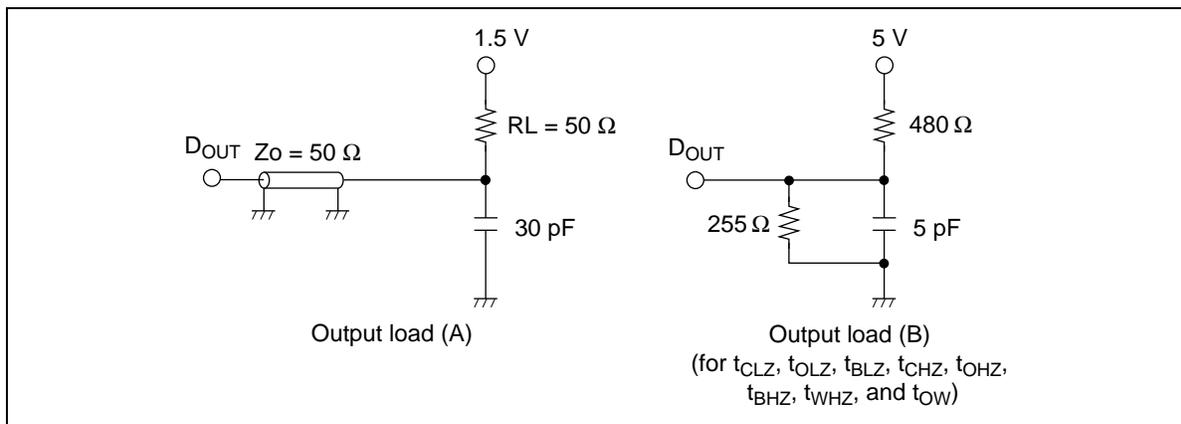
Read Cycle

Parameter	Symbol	HM6216255HCI -12 Min	Max	Unit	Notes
Read cycle time	t_{RC}	12	—	ns	
Address access time	t_{AA}	—	12	ns	
Chip select access time	t_{ACS}	—	12	ns	
Output enable to output valid	t_{OE}	—	6	ns	
Byte select to output valid	t_{BA}	—	6	ns	
Output hold from address change	t_{OH}	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	ns	1
Byte select to output in low-Z	t_{BLZ}	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	6	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	ns	1
Byte deselect to output in high-Z	t_{BHZ}	—	6	ns	1

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Write Cycle

Parameter	Symbol	HM6216255HCI -12 Min	Max	Unit	Notes
Write cycle time	t_{WC}	12	—	ns	
Address valid to end of write	t_{AW}	8	—	ns	
Chip select to end of write	t_{CW}	8	—	ns	8
Write pulse width	t_{WP}	8	—	ns	7
Byte select to end of write	t_{BW}	8	—	ns	
Address setup time	t_{AS}	0	—	ns	5
Write recovery time	t_{WR}	0	—	ns	6
Data to write time overlap	t_{DW}	6	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	ns	1
Write enable to output in high-Z	t_{WHZ}	—	6	ns	1

Notes: 1. Transition is measured ±200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.

2. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.

4. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

5. t_{AS} is measured from the latest address transition to the latest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going low.

6. t_{WR} is measured from the earliest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going high to the first address transition.

7. A write occurs during the overlap of a low $\overline{CS}$, a low $\overline{WE}$ and a low $\overline{LB}$ or a low $\overline{UB}$ (t_{WP}). A write begins at the latest transition among $\overline{CS}$ going low, $\overline{WE}$ going low and $\overline{LB}$ going low or $\overline{UB}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high, $\overline{WE}$ going high and $\overline{LB}$ going high or $\overline{UB}$ going high.

8. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.

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Timing Waveforms

**Read Timing Waveform (1)** ($\overline{WE} = V_{IH}$)

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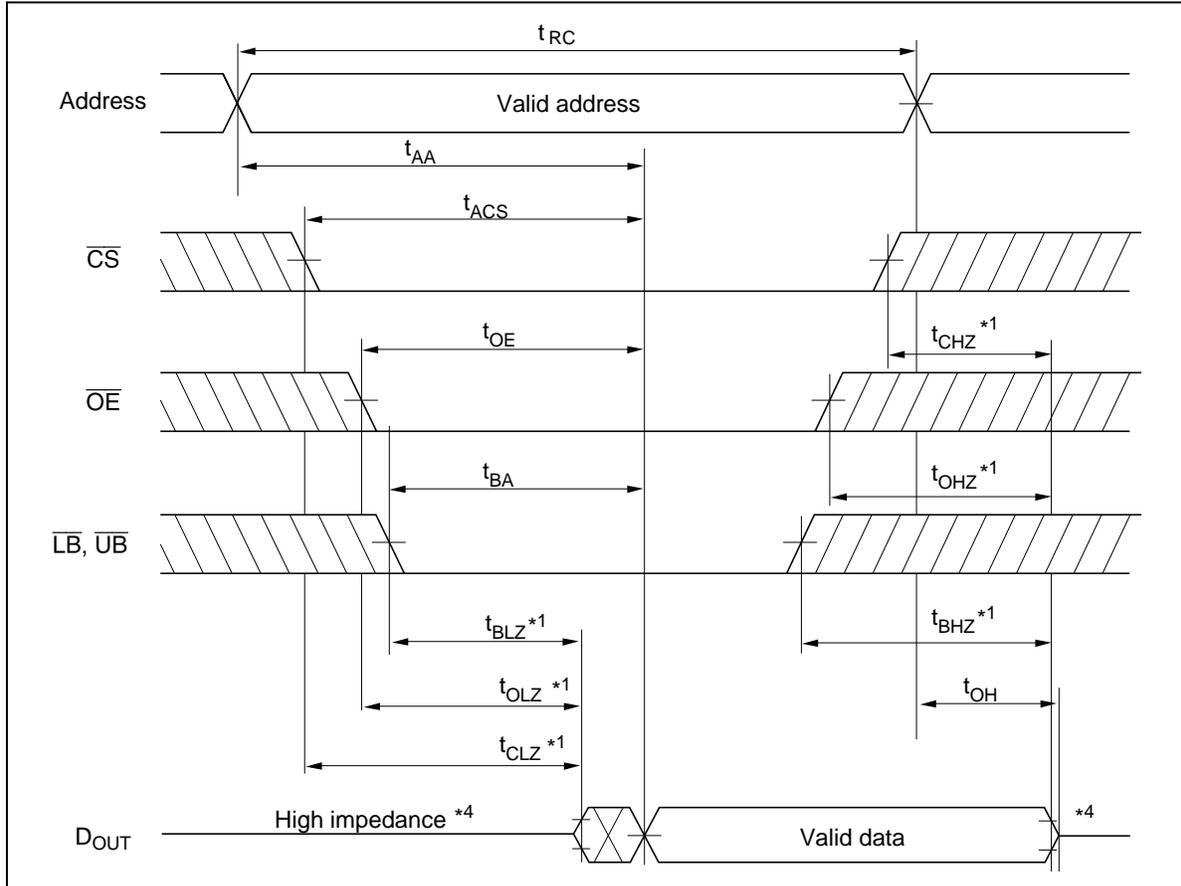
Read Timing Waveform (2) ($\overline{\text{WE}} = V_{\text{IH}}$, $\overline{\text{LB}} = V_{\text{IL}}$, $\overline{\text{UB}} = V_{\text{IL}}$)

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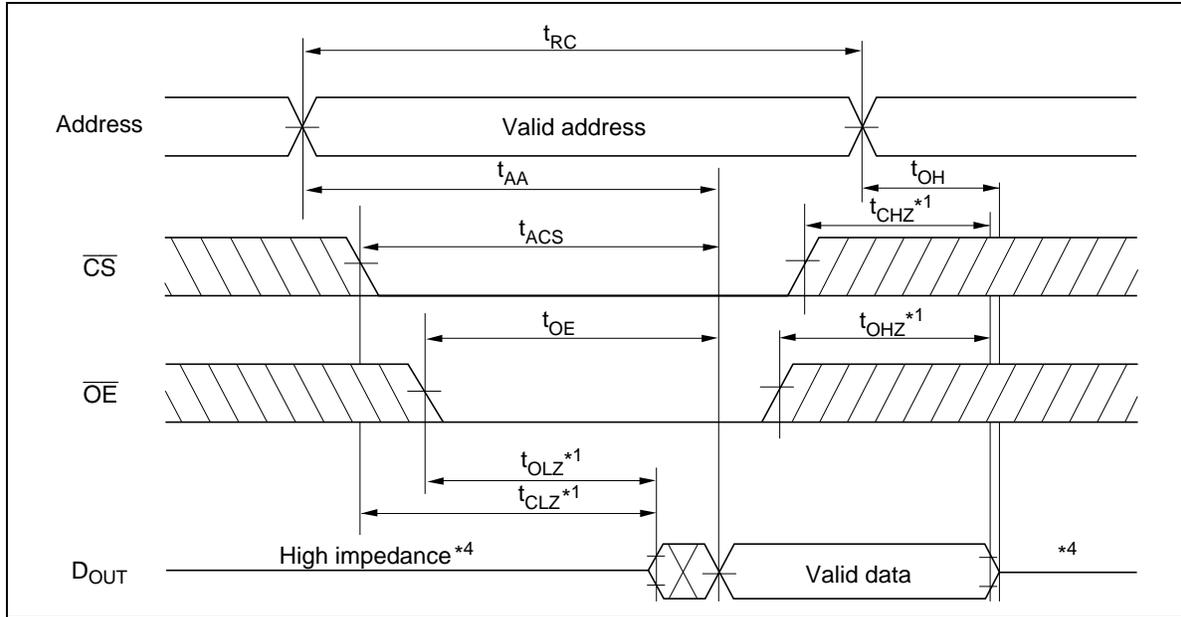
Write Timing Waveform (1) ($\overline{\text{WE}}$ Controlled)

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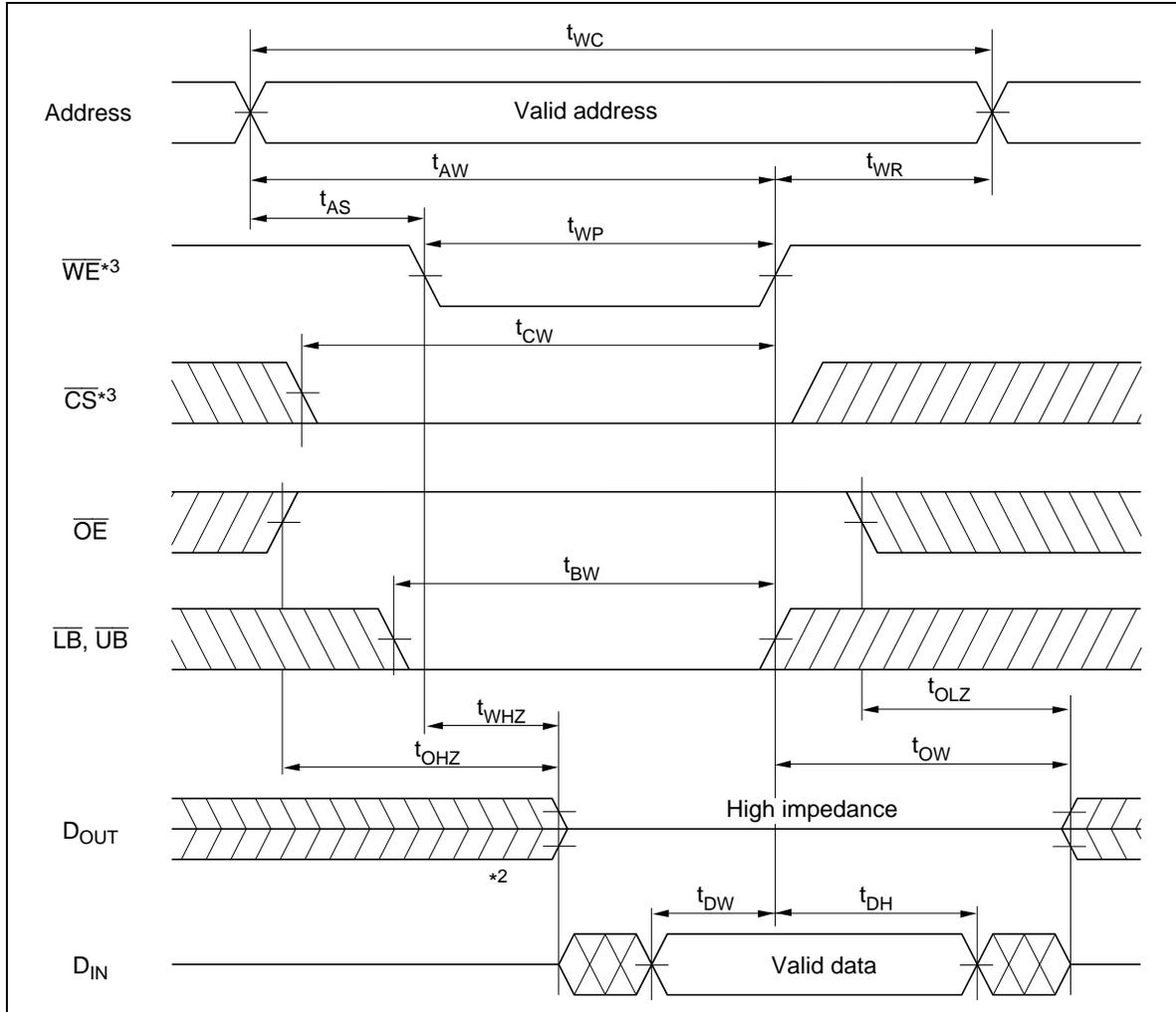
Write Timing Waveform (2) ($\overline{\text{CS}}$ Controlled)
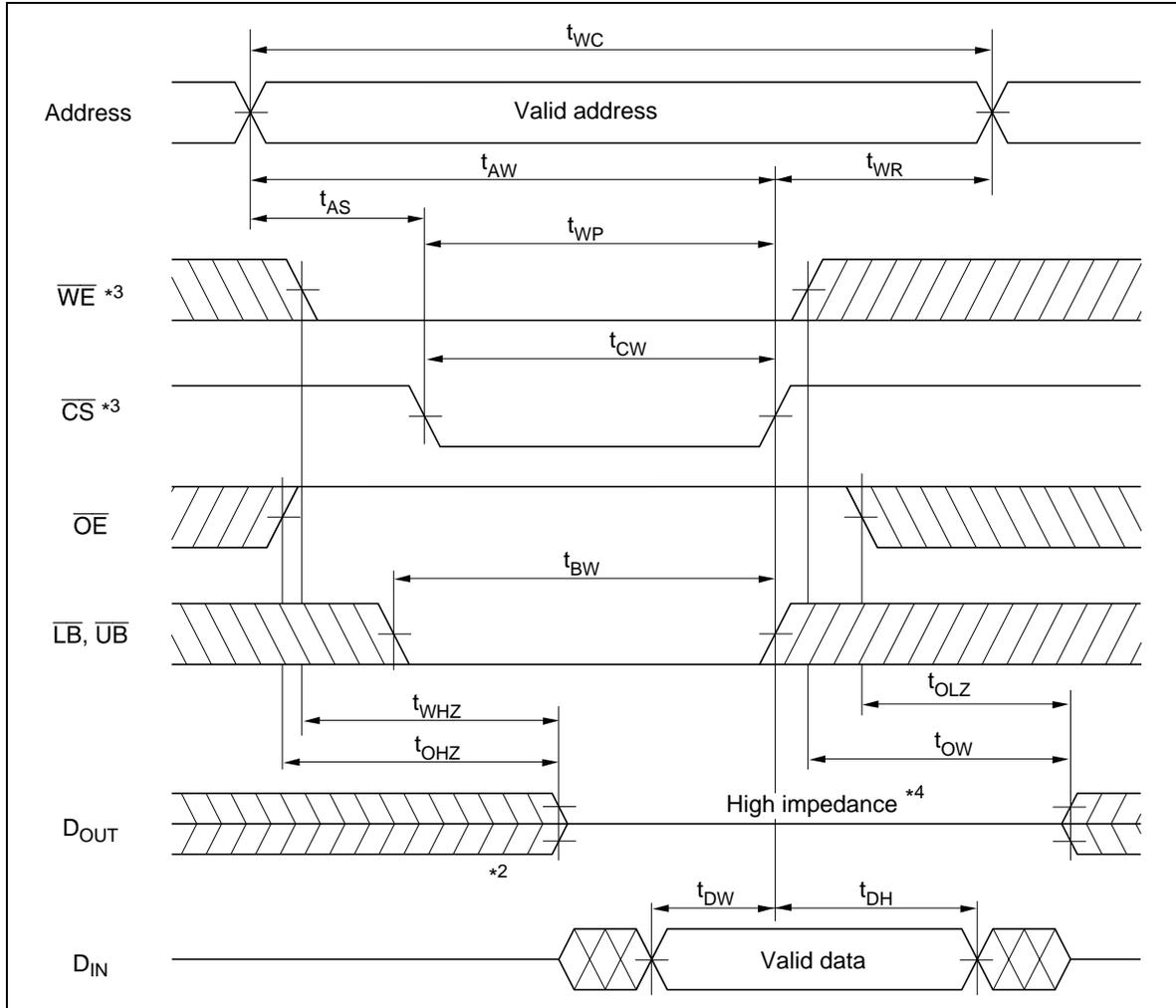
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**Write Timing Waveform (3)** ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, $\overline{\text{OE}}$ = V_{IH})
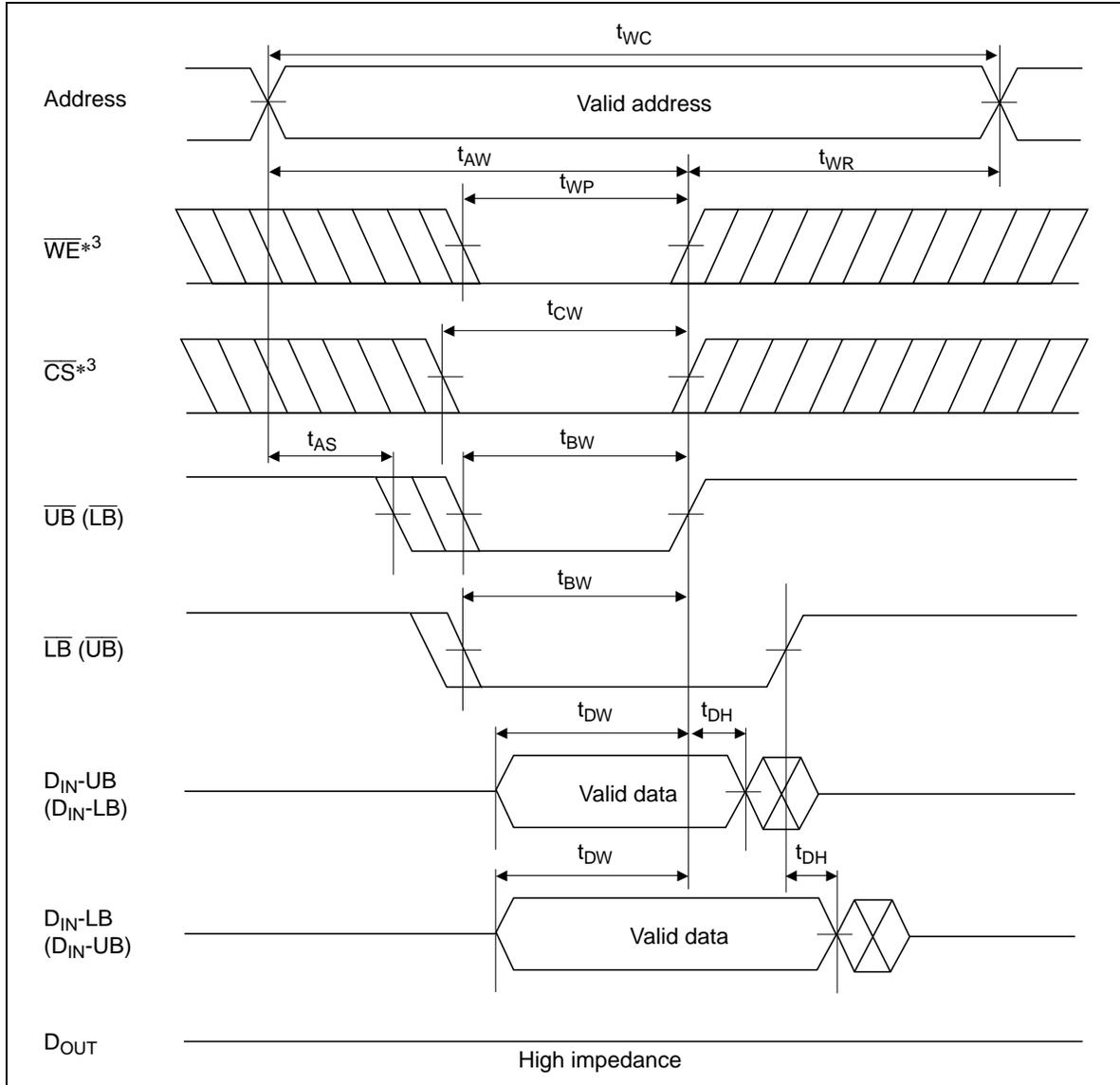
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Package Dimensions

HM6216255HCJPI Series (CP-44D)

As of July, 2002
Unit: mm

28.33
28.90 Max

44   23

10.16 ± 0.13
11.18 ± 0.13

1   22

0.74

1.30 Max

3.50 ± 0.26

0.80 +0.25 −0.17

2.65 ± 0.12

*0.43 ± 0.10
0.41 ± 0.08

1.27

9.40 ± 0.25

△ 0.10

*Dimension including the plating thickness
Base material dimension

Hitachi Code	CP-44D
JEDEC	Conforms
JEITA	—
Mass (reference value)	1.8 g
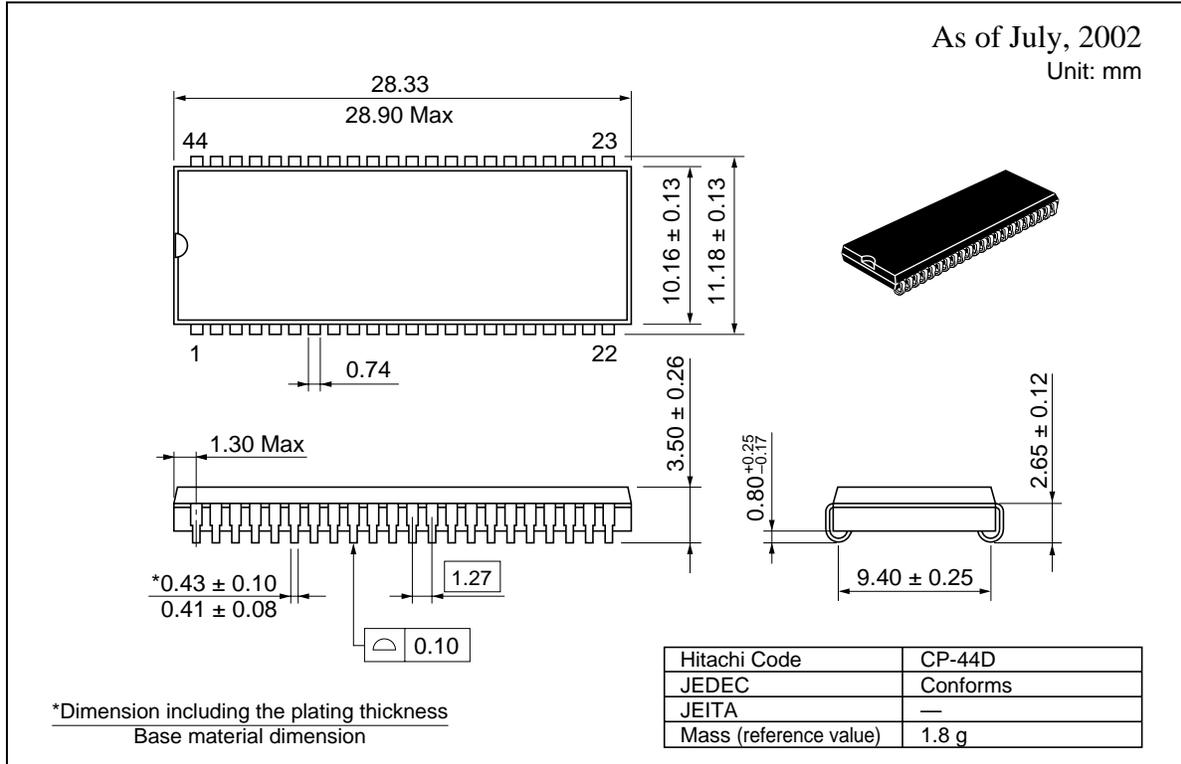
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HM6216255HCTTI Series (TTP-44DE)

As of July, 2002
Unit: mm

18.41
18.81 Max

44   23

10.16

1   22

0.80

*0.27 ± 0.07
0.25 ± 0.05

⊕ 0.13 Ⓜ

0.80

1.005 Max

1.20 Max

⌴ 0.10

11.76 ± 0.20

0˚ − 5˚

*0.145 ± 0.05
0.125 ± 0.04

0.13 ± 0.05

0.50 ± 0.10

0.68

*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
JEITA	—
Mass (reference value)	0.43 g
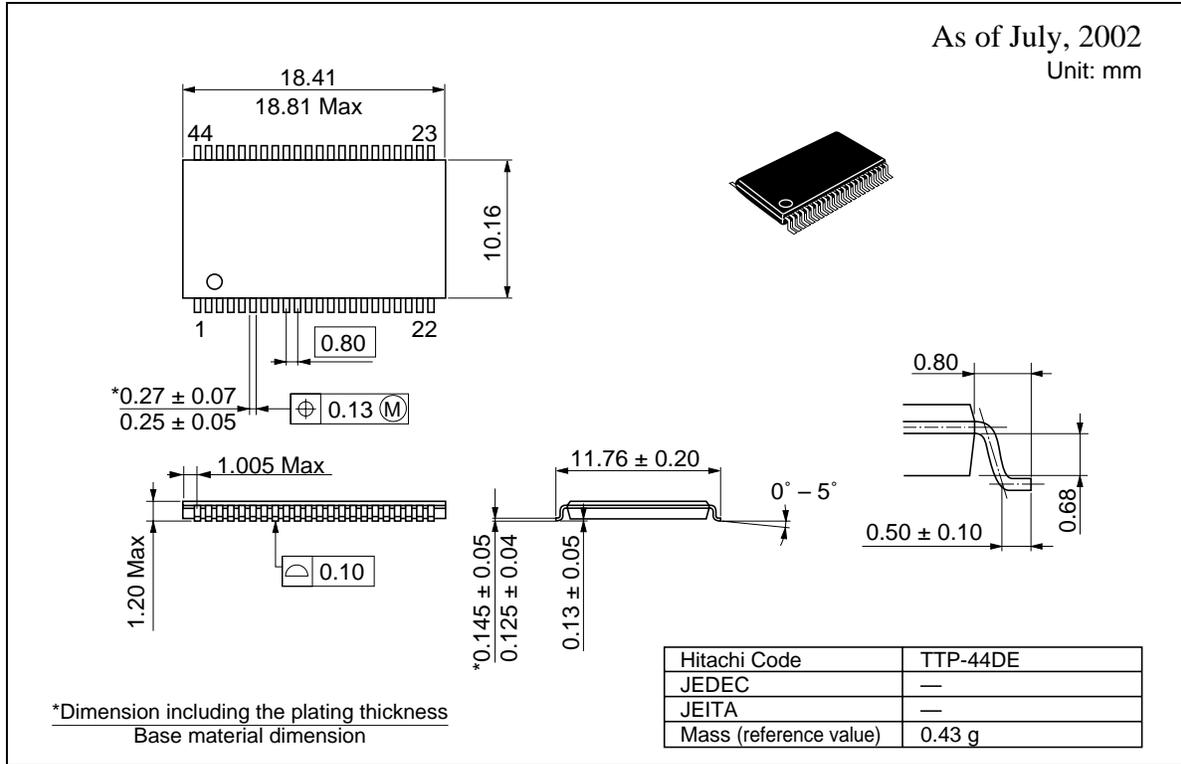
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