Other QUALCOMM VLSI Products

- Viterbi Decoders – 256 Kbps to 25 Mbps Maximum Data Rates
- Dual Direct Digital Synthesizers (DDS)
- Phase Locked Loop (PLL) Frequency Synthesizers
- DDS and PLL Evaluation Boards
- VCOs

QUALCOMM Incorporated
VLSI Products Division
10555 Sorrento Valley Road
San Diego, CA 92121-1617 USA

May 1992
DL80-3749-2 X1
DJS

CONTENTS

FIGURES

TABLES

FEATURES

- Trellis-Coded Modulation Encoder/Pragmatic Trellis-Coded Modulation Decoder and Convolutional Encoder/Viterbi Decoder on one device
- Full-duplex (encoder/decoder) Rate 2/3 (8-PSK) and Rate 3/4 (16-PSK) modulation
- Processor Interface that simplifies control and status
- Backwards-compatible with the Q0256 and Q1650 Viterbi Decoders
- 3.2 dB Coding Gain (Rate 2/3), 3.1 dB Coding Gain (Rate 3/4) at 10^{-5} BER
- Automatic Synchronization Capability for Pragmatic Trellis-Coded Modulation Decoder and Viterbi Decoder
- Data rates up to 60 Mbps for Rate 3/4
- Low -power CMOS Implementation
- Standard 84-Pin LCC Package

Preliminary Data

APPLICATIONS

- Direct Broadcast Satellite
- Microwave Point-to-Point Data Links
- Bandwidth-Efficient Digital Communication Systems
- Digital Video Transmission Systems

GENERAL DESCRIPTION

Typically, forward error correction (FEC) is used to improve performance in power-limited systems through increased bandwidth. However, the improvement provided by FEC can be produced without expanding bandwidth, if higher order signal sets are used in the modulation in conjunction with trellis-coded modulation (TCM).

TCM is an FEC technique that provides higher throughput data rates with improved bit error rate (BER) performance for power-limited and bandwidth-limited digital communication channels. Pragmatic trellis-coded modulation (PTCM) decoding is a new technique, based on the industry standard k=7 Viterbi decoding algorithm, used to decode information that has been TCM encoded. TCM encoding of data combined with PTCM decoding at the receiving node is a powerful new FEC technique for digital communication channels (figure 1), especially those concerned with errors caused by the introduction of additive white Gaussian noise (AWGN). Satellite communication channels are examples of this noise environment.

The Q1875 PTCM Decoder operates in two general modes: convolutional coding mode and PTCM mode. Both operating modes implement the Viterbi algorithm for decoding. When operating in convolutional coding mode, the Q1875 decoder operates identically to QUALCOMM's Q1650 and Q0256 Viterbi decoders.

In PTCM mode, the decoder provides both TCM encoding (figure 2) and PTCM decoding (figure 3) of data channels, while also incorporating powerful built-in features. In this mode, the Q1875 processes data at two selectable code rates (2/3 [8-ary modulation] and 3/4 [16-ary modulation]), using the industry standard constraint length (k) equals seven algorithms. The decoder provides built-in synchronization capability for 8-PSK and 16-PSK modems. The capabilities of this single-chip device have been optimized for modern digital communication channels.

The Q1875 PTCM Decoder is available in different speed grades to suit a variety of system applications, from 0 to a maximum of 60 Mbps. All speed grades are

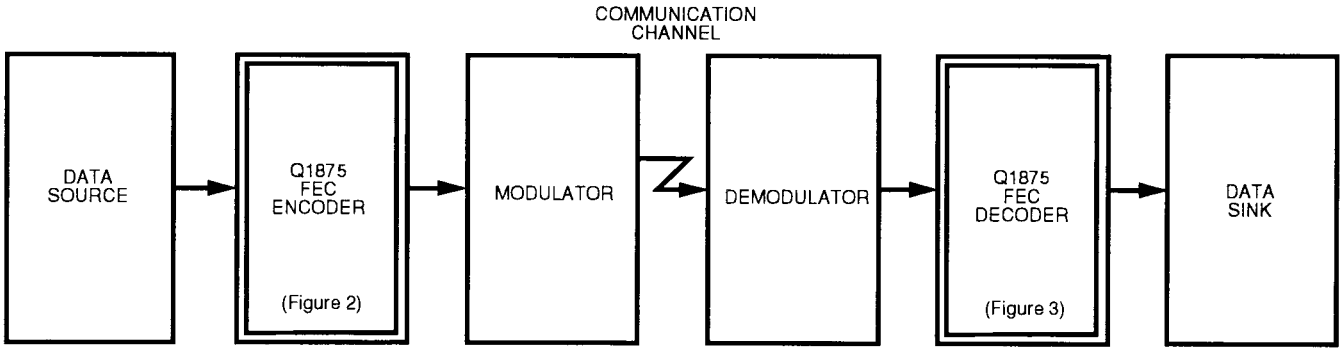


FIGURE 1. TYPICAL APPLICATION OF FEC IN A COMMUNICATIONS SYSTEM

pin-for-pin compatible; therefore, a single modem board design can be used for many data rates by installing the corresponding speed grade of the decoder for a given application.

The Q1875 PTCM Decoder includes a powerful, built-in capability for monitoring synchronization status. In addition, the decoder includes a processor interface to simplify control and status monitoring while keeping device pinout to a minimum.

The decoder is packaged in an 84-pin plastic or ceramic leaded chip carrier and is implemented using fully static CMOS logic to reduce power consumption. The decoder also uses fully parallel circuit architecture to negate the requirement for a higher speed computation clock signal.

The Q1875 PTCM Decoder is well suited for commercial satellite communications networks. This decoder's low cost and high performance also make it an ideal solution for FEC requirements in systems such as direct broadcast satellite, microwave point-to-point data links, bandwidth-efficient digital communications systems, and digital video transmission systems.

THEORY OF OPERATION

Trellis-Coded Modulation

In classical digital communications systems, the modulation and error-correction coding functions are optimized separately. Gottfried Ungerboeck described a technique that combines convolutional codes with clever signal mapping to create a system in which simple codes provide significant performance gains in systems using higher-order modulation schemes (Ungerboeck 1982). "Trellis" refers to the state-transition (trellis) diagram (similar to the trellis diagrams of binary convolutional codes) used to describe these TCM schemes.

Ungerboeck's general coding approach transmitted "n" user information bits per symbol coded with a rate "n/n+1" code, using a modulation signal constellation with 2^{n+1} points in it. For example, a rate $\frac{2}{3}$ code encodes 2 information bits into 3 coded bits that are transmitted with an 8-PSK modulator. Ungerboeck described how to choose codes for this scheme and presented the best codes for many constraint lengths. Unfortunately, these codes differed from the classical binary convolutional codes traditionally used for BPSK and QPSK modulation. In fact, different codes are required for each modulation type and code rate. Subsequently, it was shown that the industry standard k=7 rate $\frac{1}{2}$ convolutional code can replace the best codes proposed by Ungerboeck with very little loss in performance (Viterbi et al. 1989). The Q1875 device includes the circuitry necessary to use the k=7 code for rate n/n+1 coding in 8-ary and 16-ary modulation schemes, such as 8-PSK and 16-PSK modulation.

Trellis Encoder

In the TCM encoder for rate $\frac{2}{3}$ 8-PSK and rate $\frac{3}{4}$ 16-PSK modulation (figure 4), the transformation from information bits to code words for transmission is accomplished by a two-step process. First, the

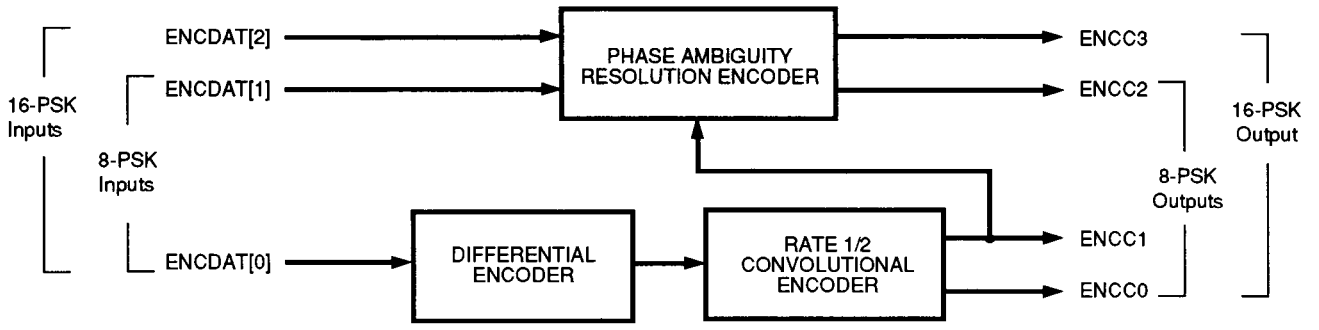


FIGURE 2. Q1875 TCM ENCODER BLOCK DIAGRAM

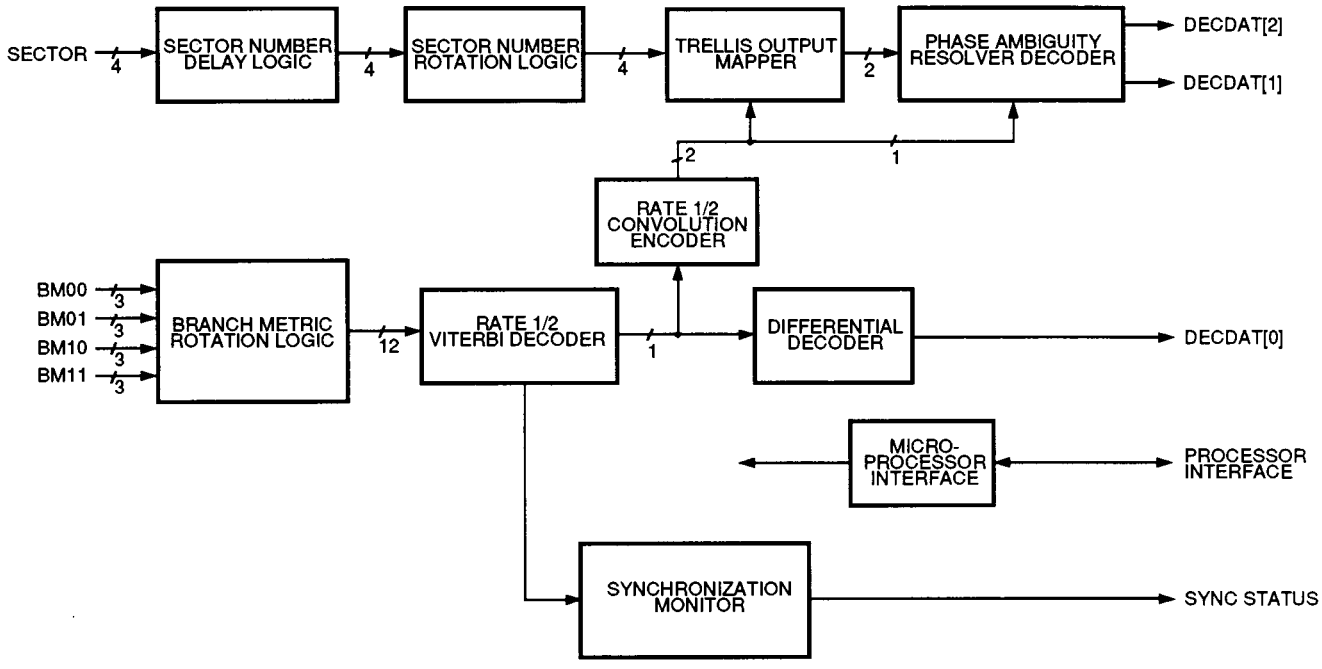


FIGURE 3. Q1875 PTCM DECODER BLOCK DIAGRAM

encoder codes the ENCDAT[0] input bit using the industry standard k=7 rate ½ convolutional code. The ENCDAT[1] input for 8-PSK modulation or the ENCDAT[1] and ENCDAT[2] inputs for 16-PSK modulation are passed through without encoding. The two bits (ENCC1 and ENCC0) output from the convolutional encoder become the least significant bits (LSBs) of the phase to be transmitted, but the order of the phases is mapped so that neighboring phases differ by only one bit position from the two code bits (ENCC1 and ENCC0). The mapping for 8-PSK and 16-PSK modulation is shown (figures 5 and 6, respectively). For example, with 8-PSK modulation, an output of 111 (binary) from the TCM encoder corresponds to a phase shift of 270° in the carrier output (figure 5). Likewise for 16-PSK modulation, an output of 0001 (binary) from the TCM encoder corresponds to a phase shift of 22.5° in the carrier output (figure 6).

Trellis coding is attractive because it possesses an aspect that other coding techniques lack: It provides error correction on all bits, although no apparent coding operation is performed on any bit other than the LSB of the input data. As such, trellis coding is an advancement over convolutional coding of input data because only one bit must be coded to achieve error correction on all data bits.

Pragmatic Trellis Decoder

While the implementation of a TCM encoder is simple, the decoding of such a coded data stream at the receiving node is quite complex. Described below is a technique used to decode TCM-coded information using an industry standard k=7 Viterbi Decoder along with supplementary circuitry (U.S. patent pending).

Fundamentally, PTCM decoding consists of three steps. First, the received symbol is converted to four "branch metrics" and a "sector number." Branch metrics are assigned based on the Euclidean distance of the received signal with respect to the four closest phase points. The sector number tells the decoder on which portion of the I-Q plane the symbol was received. Sector numbers are assigned for 8-PSK modulation (figure 5) by dividing the signal constellation into eight equal sectors. Likewise for 16-PSK modulation (figure 6), the signal constellation is divided into sixteen equal sectors. Sector numbers are assigned by numbering each sector from 0 to 7 for 8-PSK modulation and 0 to 15 for 16-PSK modulation (figures 5 and 6, respectively). The actual value input into the Q1875 PTCM Decoder is the binary representation of the sector number. Note that a sector is defined from a signal point counterclockwise to the border of the next signal point. For example, sector 2 for 8-PSK modulation begins at the phase point 011 (90°) but ends just before phase point 010 (135°).

During the second step of the decoding process, the PTCM decoder processes the branch metrics with the standard k=7 Viterbi Decoder algorithm to decode the DECDAT[0] output. This decoded output is presented at the output of the PTCM decoder.

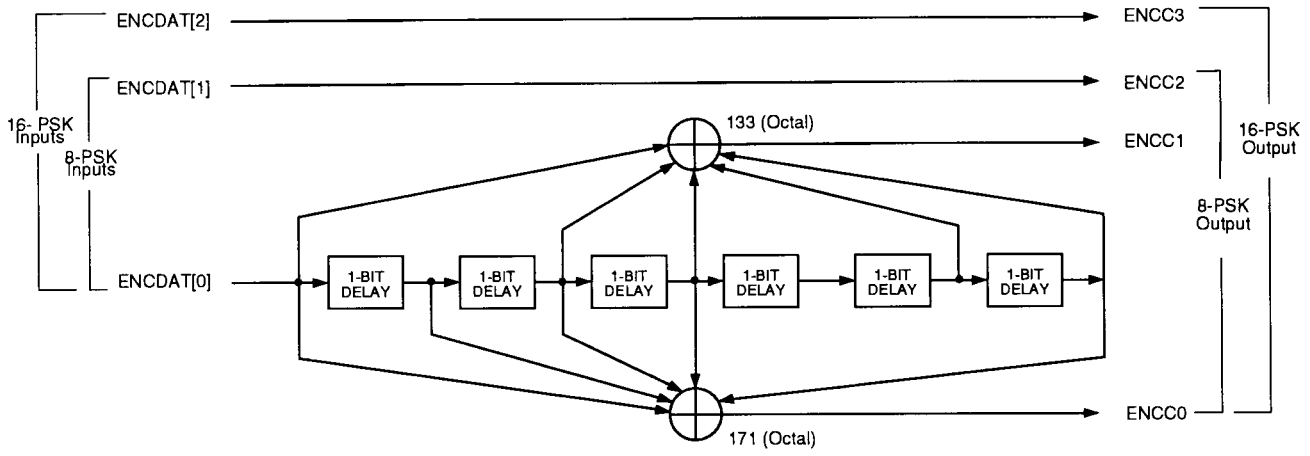


FIGURE 4. 64-STATE TCM ENCODER

The sector number generated in step one is saved within the decoder until a decision is made about the DECDAT[0] data output bit. The third step takes the DECDAT[0] data bit and re-encodes it to generate the best possible estimates of the ENCC0 and ENCC1 transmitted bits. Given these two bits, there are only two possible phases that could have been transmitted for 8-PSK modulation and only four possible phases for 16-PSK modulation. The phase closest in Euclidean distance to the sector that actually was received (indicated by the sector number) is determined to be the most likely phase.

Using 8-PSK modulation as an example, if the received signal is a phase of 100°, then this corresponds to a sector number of 2 (figure 5). If the re-encoded bit provides estimates of ENCC1=0 and ENCC1=1, then the two possible received phase points correspond to 001 and 101. Since the received phase of 100° is located in a sector that is closer to phase point 001 than to phase point 101, the DECDAT[2] data bit is determined to be 0.

A similar example can be supplied for 16-PSK modulation (figure 6). If the received signal is a phase of 175°, then this would corresponds to a sector number of 7. If the re-encoded bit provides estimates of ENCC1=0 and ENCC0=0, then four possible received phase points correspond to 0000, 0100, 1100, and 1000 (figure 6). Since the received phase of 175° is located in a sector that is closer to phase point 1100, the DECDAT[1] and DECDAT[2] data bits are determined to be DECDAT[1]=1 and DECDAT[2]=1.

Branch metrics and sector numbers are determined outside the Viterbi Decoder using an external lookup table. Tables for phase to branch metric/sector number are given in "Modes of Operation," page 14.

FUNCTIONAL OVERVIEW

Interfacing

All Q1875 data inputs are provided to the device synchronously with externally sourced clocks. Data signals are clocked into the device on the rising edge of the encoder and decoder clock inputs. Data outputs change on the rising edge of the encoder and decoder clock outputs. For rate $^2/_3$ operation, 2 information bits are input to the encoder, and 3 symbol bits are output from the encoder during each clock period.

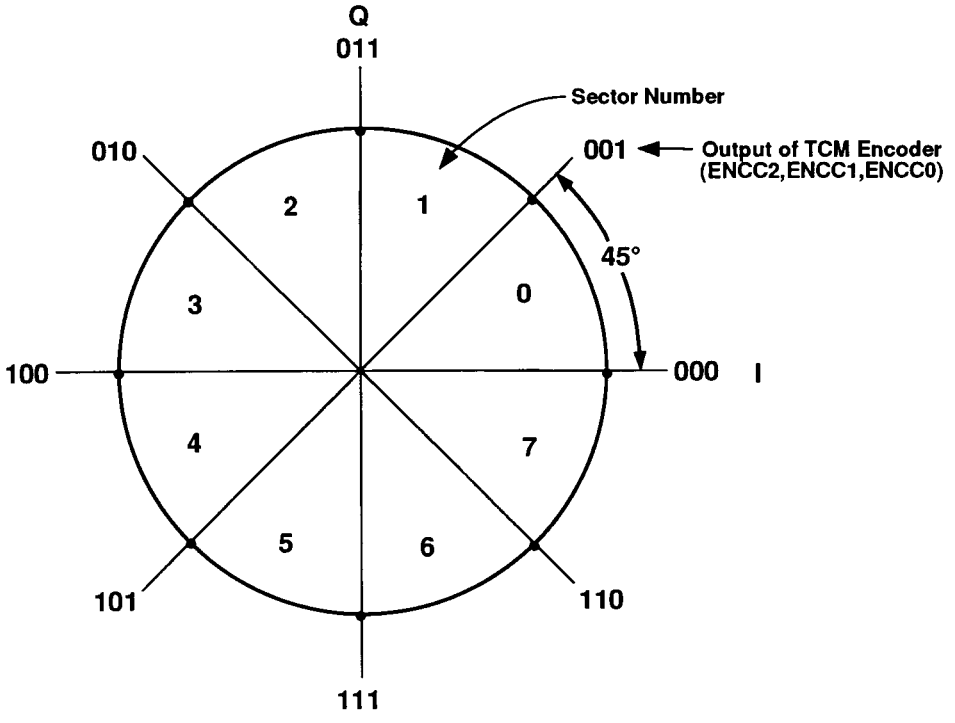


FIGURE 5. ENCODER OUTPUT MAPPING FOR 8-PSK MODULATION

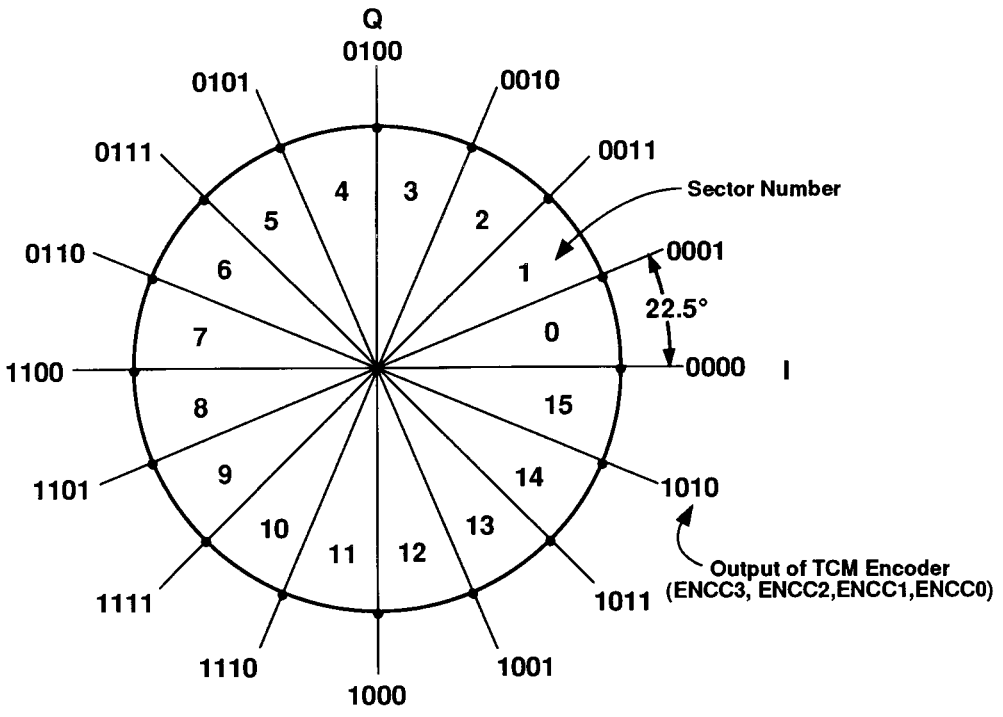


FIGURE 6. ENCODER OUTPUT MAPPING FOR 16-PSK MODULATION

At the decoder, 3 symbol bits are input, and 2 information bits are output from the decoder during each clock period.

For rate ¾ operation, 3 information bits are input to the encoder, and 4 symbol bits are output from the encoder during each clock period. At the decoder, 4 symbol bits are input, and 3 information bits are output from the decoder during each clock period.

Most control and status information is provided to and from the decoder through a bus-oriented processor interface. This interface uses an 8-bit data bus and a 5-bit address bus along with read, write, and chip-select signals to read from status ports and write to control ports in the decoder.

In addition, the encoder and decoder input and output data can be written and read directly using the processor interface. In this mode, the decoder acts as a peripheral for forward error correcting of data processed by a host processor.

Clocking Scheme

The clocking of the Q1875 PTCM Decoder is very elementary. For the encoder, the ENCINCLK and ENCOUTCLK clock inputs should be tied together and clocked at one-half the information rate for 8-PSK modulation and one-third the information rate for 16-PSK modulation. For the decoder, the DECINCLK and DECOUTCLK clock inputs should be tied together and clocked at the symbol rate.

Coding Performance

The Q1875 PTCM Decoder provides coding performance very near the theoretical limits for the best 64-state Ungerboeck code for rate ⅔ 8-PSK modulation and rate ¾ 16-PSK modulation (figure 7). A coding gain of 3.2 dB is achieved when operating at a code rate of ⅔ 8-PSK modulation and a decoded bit error rate of 10^{-5}. Coding gain is 3.1 dB for the same conditions when operating with rate ¾ 16-PSK modulation.

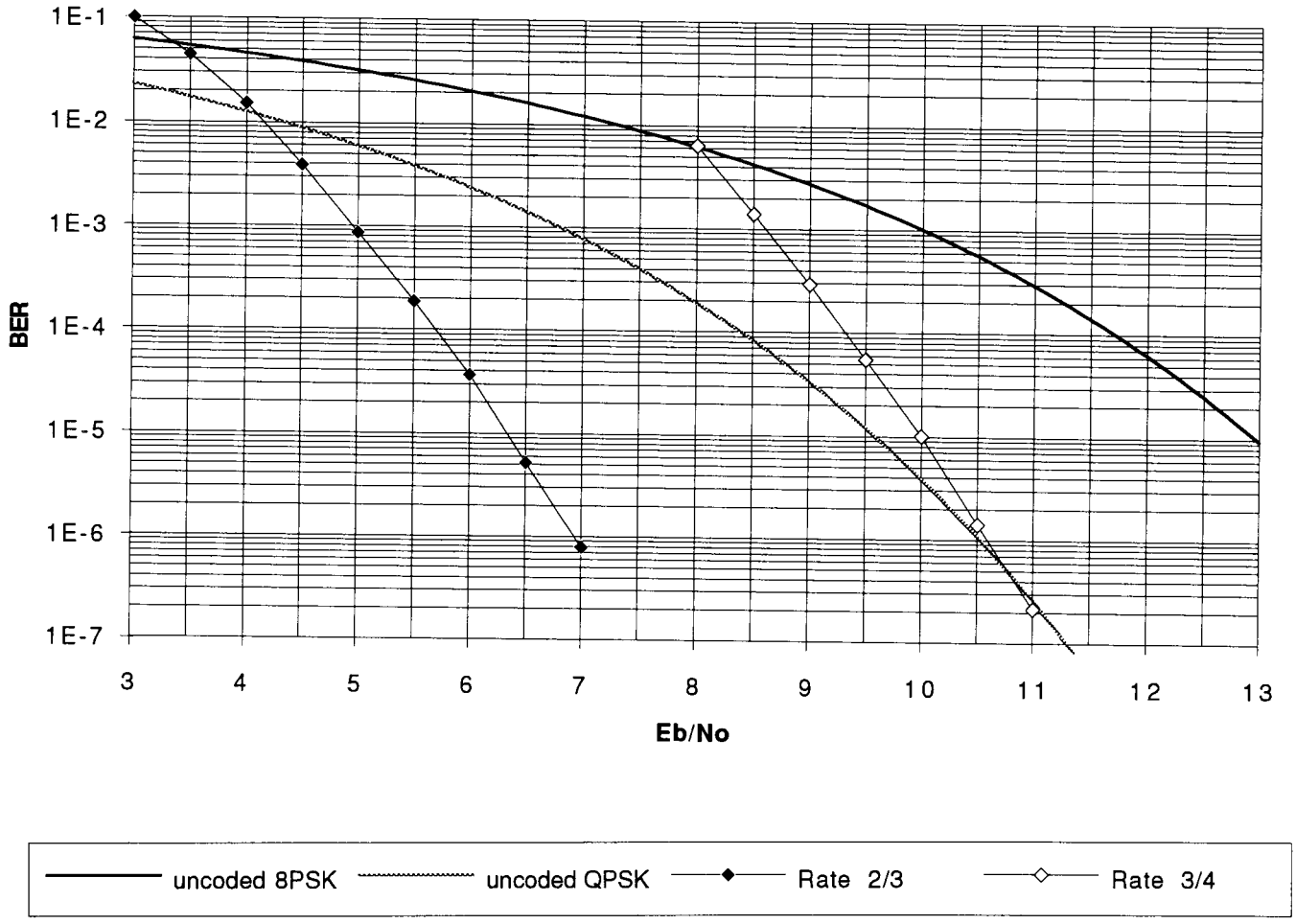


FIGURE 7. Q1875 CODING PERFORMANCE

Normalization Rate Monitor Operation (Synchronization Status Monitor)

The Q1875 PTCM Decoder provides a powerful means to monitor the performance of the PTCM decoder function. The technique monitors the rate at which the internal state metrics of the Viterbi algorithm increase in value. Rapidly increasing state metric values indicate that the decoder may be out of synchronization to the phase associated with the input symbols.

When all state metrics in the Viterbi Decoder reach a certain numeric value, a normalization circuit reduces the value of all metrics by a fixed amount to prevent metric overflow. The Q1875 PTCM Decoder monitors the rate at which these normalizations occur while decoding data.

The system designer determines an acceptable normalization rate threshold and programs this threshold into the Q1875 device. The designer controls both the period of time in which the metric normalization is monitored as well as the number of normalizations allowed during that time. These two numbers, which provide for more than 65,000 possible settings, are programmed into the device using the microprocessor interface. If the threshold is not exceeded during any test period, a signal (INSYNC) indicates that the decoder is synchronized. If the threshold is exceeded during any test period, a signal (OUTOFSYNC) indicates the detected loss of synchronization. In many cases, this signal can be used with an external D flip-flop divider to provide a correction signal to a synchronization control input pin (SYNCCHNG). In this configuration, the decoder will attempt to correct the synchronization by

changing the synchronization state of the decoder input and performing a retest. This technique provides a complete self-synchronizing decoder function for a variety of communications systems (figure 12).

The on-chip normalization circuit (figure 8) consists of two accumulators acting as counters. The system designer controls the periods of these two counters.

The first counter (T) measures the number of decoded bits. The second counter (N) measures the number of state metric normalizations. The normalization rate threshold is determined by taking the ratio of the count of normalizations (the N counter) and the time period (the T counter). Each 8-bit-wide binary counter is pre-loaded using the processor interface registers. Both the N and T counters are loaded with binary values that are the two's complements of the actual count value. The count value loaded into the T counter is multiplied by 256 to determine the actual number of decoded bits in the normalization test period.

The actual count of the N counter is determined by the following formula:

$$n = (N\text{-}1) \times 8+4$$

where "n" is the actual number of normalizations allowed, and "N" is the two's complement value of the 8-bit number loaded into the N counter. With this programming capability, the system designer selects the normalization rate threshold for determining in-sync or out-of-sync conditions as well as the period of the measurement. For example, when operating with rate 2/3 8-PSK or rate 3/4 16-PSK decoding, a normalization rate threshold of approximately 14% will reliably detect a loss of synchronization.

To avoid false detection of synchronization loss due to a noise burst, the normalization measurement should detect at least 20 to 30 normalizations before declaring a loss of synchronization. As an example, the system designer may specify 108 as the number of normalizations to be detected. By loading the 8-bit, two's complement value of 14 (i.e., F2H) into the N counter register, the actual number of normalizations allowed in a test period without indicating a loss of synchronization would be $(14\text{-}1) \times 8 + 4 = 108$. The value for the T counter must be approximately 7 times ($1/.14$) the value in the N counter; that is, loading the T counter with the two's complement value of 3 (i.e., FDH), the actual count value for T will be $(3 \times 256) = 768$. The actual normalization rate threshold will be $108/768 = 14\%$. This is an appropriate threshold for reliable synchronization when operating with rate 2/3 and rate 3/4 coding.

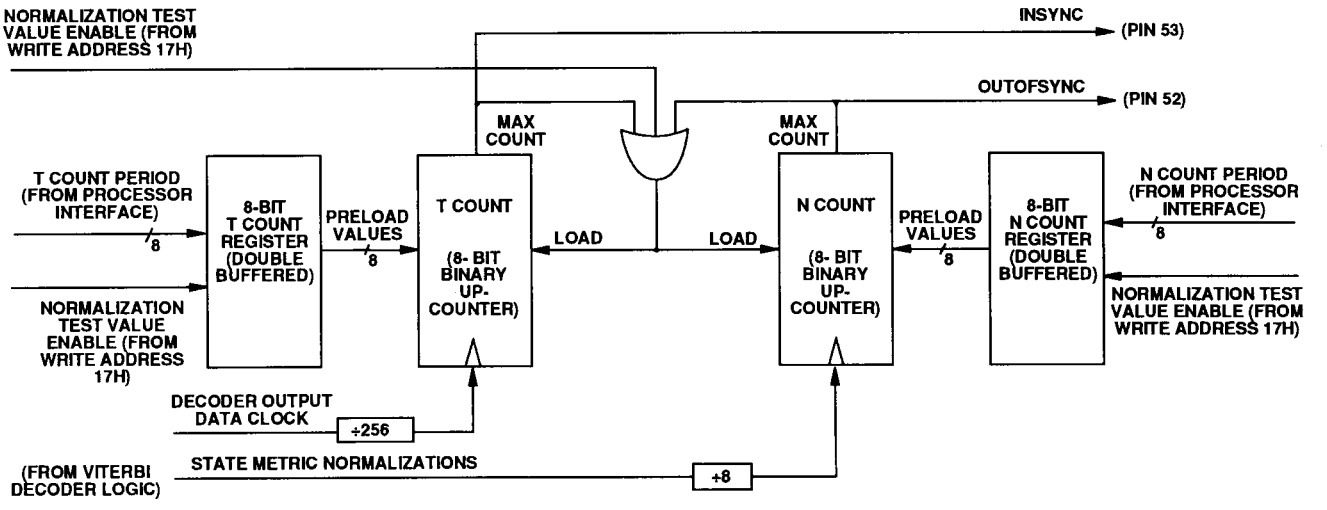


FIGURE 8. NORMALIZATION RATE MONITOR CIRCUIT

Phase Ambiguity Resolver

In a communications system utilizing TCM with 8-PSK or 16-PSK modulation without an absolute phase reference, the receiver (decoder) phase can differ from the transmitter (encoder) phase (i.e., a phase shift in the transmitted data with respect to the received data). Thus, it is necessary to encode the data in a manner that permits a decoding of the data while also overcoming the phase ambiguities caused by the transmission channel. In the case of 8-PSK modulation, the receiver may differ from the

transmitter phase by $45^\circ \times k$, where $k = 0$ to 7. Likewise for 16-PSK modulation, the receiver may differ from the transmitter phase by $22.5^\circ \times k$, where $k = 0$ to 15.

The Viterbi Decoder used in the PTCM algorithm is incapable of detecting data that is in error due to channel phase shifts of 90°, 180°, and 270° when using 8-PSK modulation. Therefore, the Viterbi Decoder produces erroneous estimates of the original data. The phase ambiguity resolution encoder for 8-PSK modulation (figure 9) is used in the encoding process to permit resolution of phase ambiguities of 90°, 180°, and 270° at the decoder (U.S. and foreign patents pending). Phase ambiguity resolution of 45°, 135°, 225°, and 315° is detailed in "Synchronization."

With 16-PSK modulation, the Viterbi Decoder is incapable of detecting data that is in error due to channel phase shifts of 45°, 90°, 135°, 180°, 225°, 270°, and 315°. The phase ambiguity resolution encoder for 16-PSK modulation (figure 10) is used in the encoding process to permit resolution of phase ambiguities by the decoder (U.S. and foreign patents pending). Phase ambiguity resolution of 22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, and 337.5° is presented in "Synchronization."

When using the phase ambiguity resolver for 8-PSK modulation, ENCDAT[0] is differentially encoded and then convolutionally encoded to form the ENCC0 and ENCC1 outputs. Coded bit ENCC1 is used to split the ENCDAT[1] data stream into two streams. Each uncoded bit stream is differentially encoded with a standard two-phase differential encoder independent of the other. For 16-PSK modulation, coded bit ENCC1 is used to split the stream of bit pairs (ENCDAT[1] and ENCDAT[2]) into two streams. Each bit pair stream of uncoded bits is differentially encoded with an independent, standard, four-phase differential encoder. The four-phase differential encoder is a two-input, two-output device that encodes the input using the present input pair, a(n) and b(n), and the previous input pair, a(n-1) and b(n-1) (see table 1). On the decoder side, a similar circuit performs the complementary function. The operation of the ambiguity resolver is "enable" or "disable" via the processor interface.

Synchronization

As described in the previous section, a communications system utilizing TCM with 8-PSK or 16-PSK modulation without an absolute phase reference can experience a phase shift in the transmitted data with respect to the received data. In the case of 8-PSK modulation, the receiver may differ from the transmitter phase by $45 \times k$, where $k = 0$ to 7. In the case of 16-PSK modulation, the receiver and the transmitter may differ by $22.5 \times k$, where $k = 0$ to 15. The phase shifts of 45°, 135°, 225°, and 315°

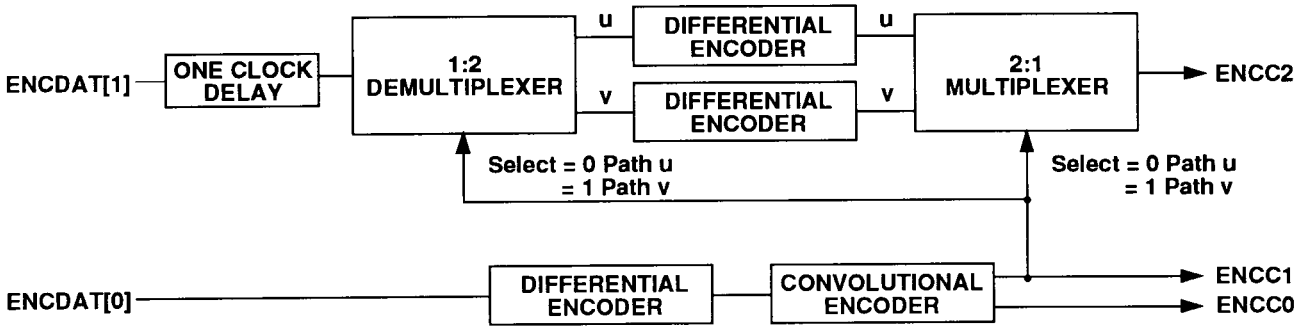


FIGURE 9. PHASE AMBIGUITY RESOLUTION ENCODER FOR 8-PSK MODULATION

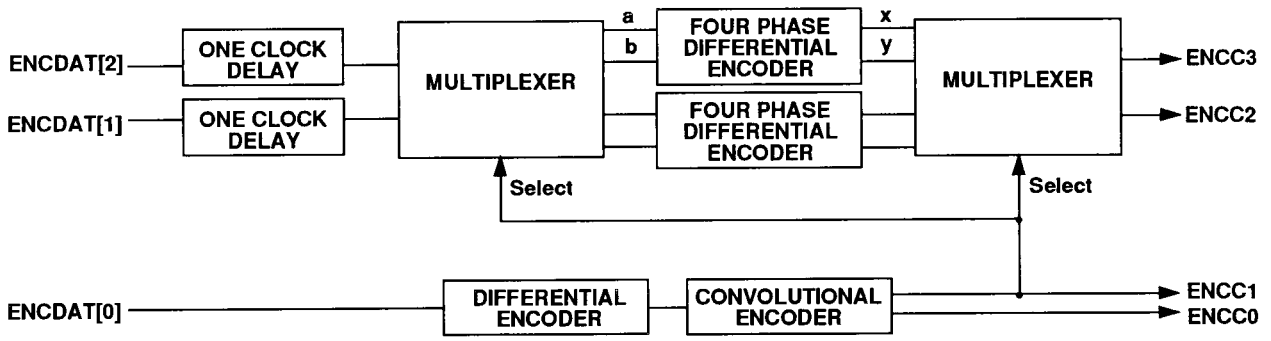


FIGURE 10. PHASE AMBIGUITY RESOLUTION ENCODER FOR 16-PSK MODULATION

TABLE 1. FOUR-PHASE DIFFERENTIAL ENCODER STATE TABLE

Present Input		Last Input		Output	
a(n)	b(n)	a(n-1)	b(n-1)	x(n)	y(n)
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	0	1	1
0	0	0	1	0	1
0	1	0	1	1	1
1	0	0	1	0	0
1	1	0	1	1	0
0	0	1	0	1	0
0	1	1	0	0	0
1	0	1	0	1	1
1	1	1	0	0	1
0	0	1	1	1	1
0	1	1	1	1	0
1	0	1	1	0	1
1	1	1	1	0	0

for 8-PSK modulation and 22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, and 337.5° for 16-PSK modulation produce erroneous outputs from the decoder and are detected by the normalization circuit used in the PTCM, since the normalization rate would be abnormally high in these cases.

The Q1875 PTCM Decoder can automatically synchronize to incoming data streams with these phase shifts. The synchronization technique is a two-step process. First, the decoder quality state is constantly monitored using the "state metric normalization rate" circuit previously described. The user programs an "in-sync/out-of-sync" threshold for this internal circuit. The success or failure of this test for each test period is indicated on the decoder's output pins 53 (INSYNC) and 52 (OUTOFSYNC). This synchronization monitor function is operational whenever the decoder is processing data.

The second step of the automatic synchronization process attempts to correct an indicated out-of-sync condition by rotating the branch metrics and sector number just prior to the actual decoding process. For 8-PSK modulation, the branch metrics and sector number are rotated by 45°; for 16-PSK modulation, they are rotated by 22.5°. This corresponds to converting the branch metrics and sector number to an adjacent sector corresponding to a phase at which the PTCM decoder is capable of recovering data (using the phase ambiguity resolver). The OUTOFSYNC output pin (pin 52) is typically connected to a D flip-flop divider (figure 12). Wiring the Q output of the flip-flop to the SYNCCHNG input pin (pin 14) on the decoder provides a feedback path between the synchronization monitor and the branch metric rotation logic. When the SYNCCHNG is high, the branch metric rotation logic rotates the incoming branch metrics and sector number. When the SYNCCHNG is low, no action is performed. The synchronization monitor runs continuously to determine whether the offsetting action taken by the branch metric rotation logic has corrected the out-of-sync condition.

Reset Circuit Operation

The Q1875 encoding and decoding functions have individual reset inputs. A reset operation should be performed when the decoder is initially configured

and whenever a change occurs in the mode of operation. The reset operation uses either the external input pins DECRESET (pin 13) and ENCRESET (pin 37) or the reset bits in control registers of the processor interface. The operation of external input pins and processor-controlled bits is identical.

When an encoder or decoder reset is asserted, either by setting the input pin to logic high or setting the processor interface bit to "1," the reset is latched synchronously into the decoder. Both input clocks of the encoder and/or decoder must be operational during reset. The reset operation is edge-triggered, and the actual reset occurs only during the first clock period after the reset line is asserted. Continuing to hold the reset line or bit to the logic high or "1" condition does not cause a continuous reset.

A reset affects the internal state of the ambiguity resolver and synchronization circuits. Resetting the ambiguity resolver sets all states to logic "0." Resetting the decoder does not set the internal states of the path memory to a fixed value.

Device Throughput Delay

When operating with either rate ⅔ 8-PSK coding or rate ¾ 16-PSK coding, the throughput delay of the encoder is 10½ periods of the ENCINCLK clock, which is the same frequency as the ENCOUTCLK input signal. The throughput delay of the decoder is 182½ periods of the DECINCLK clock, which is the same frequency as the DECOUTCLK signal. These throughput delay values are the same for operation in both direct and peripheral modes.

Direct vs. Peripheral Data Mode Operation

The Q1875 PTCM Decoder interfaces with data via dedicated signal pins or via the processor interface. The Direct Data mode interfaces with all data via the dedicated pins and is most commonly used with synchronous data channels. The Peripheral Data mode interfaces with all data signals via processor interface registers. This mode is used when the decoder is functioning as an error control peripheral to the processor system.

When operating in Peripheral Data mode, the functions of the following signals are provided by writing to port addresses: ENCDAT[0, 1, 2] (pins 33, 35, and 34), ENCINCLK (pin 36), ENCOUTCLK (pin 44), ENCRESET (pin 37), BM00 (pins 29, 28, 27), BM01 (pins 18, 17, and 16), BM10 (pins 26, 22, and 19), BM11 (pins 32, 31, 30), SECTOR[0-3] (pins 10, 9, 8, and 7), DECINCLK (pin 11), DECOUTCLK (pin 23), and DECRESET (pin 13). In this mode, all above-mentioned pins should be connected to logic "0." Direct or Peripheral Data mode is selected by setting bit 3 in both Encoder Control Register 2 and Decoder Control Register 2 of the processor interface (0 = Direct, 1 = Peripheral).

In Peripheral Data mode, each data bit handled by either the encoder or the decoder requires four processing steps. First, input data to the encoder or decoder is written to the appropriate register using the processor interface (tables 8 through 11). Second, processor-controlled activation of ENCINCLK or DECINCLK is performed by writing to the appropriate processor interface address. Then, processor-controlled activation of ENCOUTCLK or DECOUTCLK is done by writing to the appropriate processor interface address. Finally, the output data is read from the appropriate register. This cycle repeats for each bit processed by the decoder.

MODES OF OPERATION

The Q1875 PTCM Decoder can operate in either rate ⅔ 8-PSK modulation or rate ¾ 16-PSK modulation. For both modes, branch metrics and a sector number for each received symbol need to be supplied from an external lookup table. The code rate of the on-chip encoder function can differ from that of the decoder function.

In addition to the basic code rate selection, the Q1875 device supports various, user-selected, operational functions and modes. Selecting the mode of operation uses the control registers of the processor interface as described below. The following paragraphs describe the functions performed and the design considerations associated with each mode.

Code Rate ⅔ 8-PSK Mode Operation

When using code rate ⅔ 8-PSK modulation, 3 encoded bits (ENCC0, ENCC1, and ENCC2) are generated by the encoder for every 2 information bits (ENCDAT[0] and ENCDAT[1]). The encoder outputs ENCC0, ENCC1, and ENCC2 are clocked out at the same

frequency that the ENCDAT[0] and ENCDAT[1] inputs are clocked in.

At the receiver, the received symbol phase must be converted to branch metrics and a sector number for use by the Q1875 PTCM Decoder (table 2). Specifically, the decoder inputs four 3-bit branch metrics (B00[2-0], B01[2-0], B11[2-0], and B10[2-0]) and a 3-bit sector number (SECTOR[2-0]) for each received symbol. The decoder outputs DECDAT[0] and DECDAT[1] are clocked out at the same frequency that the branch metrics and sector number inputs are clocked in.

Code Rate ¾ 16-PSK Mode Operation

Operating with code rate ¾ 16-PSK modulation, 4 encoded bits (ENCC0, ENCC1, ENCC2, and ENCC3) are generated by the encoder for every 3 information

TABLE 2. 8-PSK MODULATION PHASE TO BRANCH METRIC CONVERSION

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$0.0 \le \varphi < 2.8$	0	4	7	4	0
$2.8 \le \varphi < 8.4$	0	3	7	4	0
$8.4 \le \varphi < 14.1$	0	2	6	4	0
$14.1 \le \varphi < 19.7$	0	1	5	4	0
$19.7 \le \varphi < 25.3$	0	0	4	4	0
$25.3 \le \varphi < 30.9$	1	0	4	5	0
$30.9 \le \varphi < 36.6$	2	0	4	6	0
$36.6 \le \varphi < 42.2$	3	0	4	7	0
$42.2 \le \varphi < 45.0$	4	0	4	7	0
$45.0 \le \varphi < 47.8$	4	0	4	7	1
$47.8 \le \varphi < 53.4$	4	0	3	7	1
$53.4 \le \varphi < 59.1$	4	0	2	6	1
$59.1 \le \varphi < 64.7$	4	0	1	5	1
$64.7 \le \varphi < 70.3$	4	0	0	4	1
$70.3 \le \varphi < 75.9$	5	1	0	4	1
$75.9 \le \varphi < 81.6$	6	2	0	4	1
$81.6 \le \varphi < 87.2$	7	3	0	4	1
$87.2 \le \varphi < 90.0$	7	4	0	4	1
$90.0 \le \varphi < 92.8$	7	4	0	4	2
$92.8 \le \varphi < 98.4$	7	4	0	3	2
$98.4 \le \varphi < 104.1$	6	4	0	2	2
$104.1 \le \varphi < 109.7$	5	4	0	1	2
$109.7 \le \varphi < 115.3$	4	4	0	0	2
$115.3 \le \varphi < 120.9$	4	5	1	0	2
$120.9 \le \varphi < 126.6$	4	6	2	0	2
$126.6 \le \varphi < 132.2$	4	7	3	0	2
$132.2 \le \varphi < 135.0$	4	7	4	0	2
$135.0 \le \varphi < 137.8$	4	7	4	0	3
$137.8 \le \varphi < 143.4$	3	7	4	0	3
$143.4 \le \varphi < 149.1$	2	6	4	0	3
$149.1 \le \varphi < 154.7$	1	5	4	0	3
$154.7 \le \varphi < 160.3$	0	4	4	0	3
$160.3 \le \varphi < 165.9$	0	4	5	1	3
$165.9 \le \varphi < 171.6$	0	4	6	2	3
$171.6 \le \varphi < 177.2$	0	4	7	3	3
$177.2 \le \varphi < 180.0$	0	4	7	4	3

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$180.0 \le \varphi < 182.8$	0	4	7	4	4
$182.8 \le \varphi < 188.4$	0	3	7	4	4
$188.4 \le \varphi < 194.1$	0	2	6	4	4
$194.1 \le \varphi < 199.7$	0	1	5	4	4
$199.7 \le \varphi < 205.3$	0	0	4	4	4
$205.3 \le \varphi < 210.9$	1	0	4	5	4
$210.9 \le \varphi < 216.6$	2	0	4	6	4
$216.6 \le \varphi < 222.2$	3	0	4	7	4
$222.2 \le \varphi < 225.0$	4	0	4	7	4
$225.0 \le \varphi < 227.8$	4	0	4	7	5
$227.8 \le \varphi < 233.4$	4	0	3	7	5
$233.4 \le \varphi < 239.1$	4	0	2	6	5
$239.1 \le \varphi < 244.7$	4	0	1	5	5
$244.7 \le \varphi < 250.3$	4	0	0	4	5
$250.3 \le \varphi < 255.9$	5	1	0	4	5
$255.9 \le \varphi < 261.6$	6	2	0	4	5
$261.6 \le \varphi < 267.2$	7	3	0	4	5
$267.2 \le \varphi < 270.0$	7	4	0	4	5
$270.0 \le \varphi < 272.8$	7	4	0	4	6
$272.8 \le \varphi < 278.4$	7	4	0	3	6
$278.4 \le \varphi < 284.1$	6	4	0	2	6
$284.1 \le \varphi < 289.7$	5	4	0	1	6
$289.7 \le \varphi < 295.3$	4	4	0	0	6
$295.3 \le \varphi < 300.9$	4	5	1	0	6
$300.9 \le \varphi < 306.6$	4	6	2	0	6
$306.6 \le \varphi < 312.2$	4	7	3	0	6
$312.2 \le \varphi < 315.0$	4	7	4	0	6
$315.0 \le \varphi < 317.8$	4	7	4	0	7
$317.8 \le \varphi < 323.4$	3	7	4	0	7
$323.4 \le \varphi < 329.1$	2	6	4	0	7
$329.1 \le \varphi < 334.7$	1	5	4	0	7
$334.7 \le \varphi < 340.3$	0	4	4	0	7
$340.3 \le \varphi < 345.9$	0	4	5	1	7
$345.9 \le \varphi < 351.6$	0	4	6	2	7
$351.6 \le \varphi < 357.2$	0	4	7	3	7
$357.2 \le \varphi < 360.0$	0	4	7	4	7

bits (ENCDAT[0], ENCDAT[1], and ENCDAT[2]). Encoder outputs ENCC0, ENCC1, ENCC2, and ENCC3 are clocked out of the encoder at the same frequency that inputs ENCDAT[0], ENCDAT[1], and ENCDAT[2] are clocked in.

The received phase is converted to branch metrics and a sector number for use by the Q1875 PTCM Decoder (table 3). Specifically, the decoder inputs four 3-bit branch metrics (B00[2-0], B01[2-0], B11[2-0], and B10[2-0]) and one 4-bit sector number (SECTOR[3-0]) for each received phase. The decoder outputs DECDAT[0], DECDAT[1], and DECDAT[2] are clocked out at the same frequency that the branch metrics and sector number inputs are clocked in.

TABLE 3. 16-PSK MODULATION PHASE TO BRANCH METRIC CONVERSION

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$0.0 \le \varphi < 1.4$	0	4	7	4	0
$1.4 \le \varphi < 4.2$	0	3	7	4	0
$4.2 \le \varphi < 7.0$	0	2	6	4	0
$7.0 \le \varphi < 9.8$	0	1	5	4	0
$9.8 \le \varphi < 12.7$	0	0	4	4	0
$12.7 \le \varphi < 15.5$	1	0	4	5	0
$15.5 \le \varphi < 18.3$	2	0	4	6	0
$18.3 \le \varphi < 21.1$	3	0	4	7	0
$21.1 \le \varphi < 22.5$	4	0	4	7	0
$22.5 \le \varphi < 23.9$	4	0	4	7	1
$23.9 \le \varphi < 26.7$	4	0	3	7	1
$26.7 \le \varphi < 29.5$	4	0	2	6	1
$29.5 \le \varphi < 32.3$	4	0	1	5	1
$32.3 \le \varphi < 35.2$	4	0	0	4	1
$35.2 \le \varphi < 38.0$	5	1	0	4	1
$38.0 \le \varphi < 40.8$	6	2	0	4	1
$40.8 \le \varphi < 43.6$	7	3	0	4	1
$43.6 \le \varphi < 45.0$	7	4	0	4	1
$45.0 \le \varphi < 46.4$	7	4	0	4	2
$46.4 \le \varphi < 49.2$	7	4	0	3	2
$49.2 \le \varphi < 52.0$	6	4	0	2	2
$52.0 \le \varphi < 54.8$	5	4	0	1	2
$54.8 \le \varphi < 57.7$	4	4	0	0	2
$57.7 \le \varphi < 60.5$	4	5	1	0	2
$60.5 \le \varphi < 63.3$	4	6	2	0	2
$63.3 \le \varphi < 66.1$	4	7	3	0	2
$66.1 \le \varphi < 67.5$	4	7	4	0	2
$67.5 \le \varphi < 68.9$	4	7	4	0	3
$68.9 \le \varphi < 71.7$	3	7	4	0	3
$71.7 \le \varphi < 74.5$	2	6	4	0	3
$74.5 \le \varphi < 77.3$	1	5	4	0	3
$77.3 \le \varphi < 80.2$	0	4	4	0	3
$80.2 \le \varphi < 83.0$	0	4	5	1	3
$83.0 \le \varphi < 85.8$	0	4	6	2	3
$85.8 \le \varphi < 88.6$	0	4	7	3	3
$88.6 \le \varphi < 90.0$	0	4	7	4	3

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$90.0 \le \varphi < 91.4$	0	4	7	4	4
$91.4 \le \varphi < 94.2$	0	3	7	4	4
$94.2 \le \varphi < 97.0$	0	2	6	4	4
$97.0 \le \varphi < 99.8$	0	1	5	4	4
$99.8 \le \varphi < 102.7$	0	0	4	4	4
$102.7 \le \varphi < 105.5$	1	0	4	5	4
$105.5 \le \varphi < 108.3$	2	0	4	6	4
$108.3 \le \varphi < 111.1$	3	0	4	7	4
$111.1 \le \varphi < 112.5$	4	0	4	7	4
$112.5 \le \varphi < 113.9$	4	0	4	7	5
$113.9 \le \varphi < 116.7$	4	0	3	7	5
$116.7 \le \varphi < 119.5$	4	0	2	6	5
$119.5 \le \varphi < 122.3$	4	0	1	5	5
$122.3 \le \varphi < 125.2$	4	0	0	4	5
$125.2 \le \varphi < 128.0$	5	1	0	4	5
$128.0 \le \varphi < 130.8$	6	2	0	4	5
$130.8 \le \varphi < 133.6$	7	3	0	4	5
$133.6 \le \varphi < 135.0$	7	4	0	4	5
$135.0 \le \varphi < 136.4$	7	4	0	4	6
$136.4 \le \varphi < 139.2$	7	4	0	3	6
$139.2 \le \varphi < 142.0$	6	4	0	2	6
$142.0 \le \varphi < 144.8$	5	4	0	1	6
$144.8 \le \varphi < 147.7$	4	4	0	0	6
$147.7 \le \varphi < 150.5$	4	5	1	0	6
$150.5 \le \varphi < 153.3$	4	6	2	0	6
$153.3 \le \varphi < 156.1$	4	7	3	0	6
$156.1 \le \varphi < 157.5$	4	7	4	0	6
$157.5 \le \varphi < 158.9$	4	7	4	0	7
$158.9 \le \varphi < 161.7$	3	7	4	0	7
$161.7 \le \varphi < 164.5$	2	6	4	0	7
$164.5 \le \varphi < 167.3$	1	5	4	0	7
$167.3 \le \varphi < 170.2$	0	4	4	0	7
$170.2 \le \varphi < 173.0$	0	4	5	1	7
$173.0 \le \varphi < 175.8$	0	4	6	2	7
$175.8 \le \varphi < 178.6$	0	4	7	3	7
$178.6 \le \varphi < 180.0$	0	4	7	4	7

Standard k=7 Viterbi Decoder Operation

The Q1875 PTCM Decoder is backwards-compatible with the Q1650/Q0256 family of Viterbi decoders. Refer to the Q1650 and Q0256 technical data sheets when using the Q1875 device in the Q1650/Q0256 convolutional encoder/Viterbi decoder mode.

CONFIGURATION EXAMPLES

Rate 2/3 8-PSK Modulation Example

For the TCM encoder (figure 11), the input data stream is processed by a serial-to-parallel converter

TABLE 3. 16-PSK MODULATION PHASE TO BRANCH METRIC CONVERSION (CONTINUED)

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
180.0 ≤ φ < 181.4	0	4	7	4	8
181.4 ≤ φ < 184.2	0	3	7	4	8
184.2 ≤ φ < 187.0	0	2	6	4	8
187.0 ≤ φ < 189.8	0	1	5	4	8
189.8 ≤ φ < 192.7	0	0	4	4	8
192.7 ≤ φ < 195.5	1	0	4	5	8
195.5 ≤ φ < 198.3	2	0	4	6	8
198.3 ≤ φ < 201.1	3	0	4	7	8
201.1 ≤ φ < 202.5	4	0	4	7	8
202.5 ≤ φ < 203.9	4	0	4	7	9
203.9 ≤ φ < 206.7	4	0	3	7	9
206.7 ≤ φ < 209.5	4	0	2	6	9
209.5 ≤ φ < 212.3	4	0	1	5	9
212.3 ≤ φ < 215.2	4	0	0	4	9
215.2 ≤ φ < 218.0	5	1	0	4	9
218.0 ≤ φ < 220.8	6	2	0	4	9
220.8 ≤ φ < 223.6	7	3	0	4	9
223.6 ≤ φ < 225.0	7	4	0	4	9
225.0 ≤ φ < 226.4	7	4	0	4	10
226.4 ≤ φ < 229.2	7	4	0	3	10
229.2 ≤ φ < 232.0	6	4	0	2	10
232.0 ≤ φ < 234.8	5	4	0	1	10
234.8 ≤ φ < 237.7	4	4	0	0	10
237.7 ≤ φ < 240.5	4	5	1	0	10
240.5 ≤ φ < 243.3	4	6	2	0	10
243.3 ≤ φ < 246.1	4	7	3	0	10
246.1 ≤ φ < 247.5	4	7	4	0	10
247.5 ≤ φ < 248.9	4	7	4	0	11
248.9 ≤ φ < 251.7	3	7	4	0	11
251.7 ≤ φ < 254.5	2	6	4	0	11
254.5 ≤ φ < 257.3	1	5	4	0	11
257.3 ≤ φ < 260.2	0	4	4	0	11
260.2 ≤ φ < 263.0	0	4	5	1	11
263.0 ≤ φ < 265.8	0	4	6	2	11
265.8 ≤ φ < 268.6	0	4	7	3	11
268.6 ≤ φ < 270.0	0	4	7	4	11

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
270.0 ≤ φ < 271.4	0	4	7	4	12
271.4 ≤ φ < 274.2	0	3	7	4	12
274.2 ≤ φ < 277.0	0	2	6	4	12
277.0 ≤ φ < 279.8	0	1	5	4	12
279.8 ≤ φ < 282.7	0	0	4	4	12
282.7 ≤ φ < 285.5	1	0	4	5	12
285.5 ≤ φ < 288.3	2	0	4	6	12
288.3 ≤ φ < 291.1	3	0	4	7	12
291.1 ≤ φ < 292.5	4	0	4	7	12
292.5 ≤ φ < 293.9	4	0	4	7	13
293.9 ≤ φ < 296.7	4	0	3	7	13
296.7 ≤ φ < 299.5	4	0	2	6	13
299.5 ≤ φ < 302.3	4	0	1	5	13
302.3 ≤ φ < 305.2	4	0	0	4	13
305.2 ≤ φ < 308.0	5	1	0	4	13
308.0 ≤ φ < 310.8	6	2	0	4	13
310.8 ≤ φ < 313.6	7	3	0	4	13
313.6 ≤ φ < 315.0	7	4	0	4	13
315.0 ≤ φ < 316.4	7	4	0	4	14
316.4 ≤ φ < 319.2	7	4	0	3	14
319.2 ≤ φ < 322.0	6	4	0	2	14
322.0 ≤ φ < 324.8	5	4	0	1	14
324.8 ≤ φ < 327.7	4	4	0	0	14
327.7 ≤ φ < 330.5	4	5	1	0	14
330.5 ≤ φ < 333.3	4	6	2	0	14
333.3 ≤ φ < 336.1	4	7	3	0	14
336.1 ≤ φ < 337.5	4	7	4	0	14
337.5 ≤ φ < 338.9	4	7	4	0	15
338.9 ≤ φ < 341.7	3	7	4	0	15
341.7 ≤ φ < 344.5	2	6	4	0	15
344.5 ≤ φ < 347.3	1	5	4	0	15
347.3 ≤ φ < 350.2	0	4	4	0	15
350.2 ≤ φ < 353.0	0	4	5	1	15
353.0 ≤ φ < 355.8	0	4	6	2	15
355.8 ≤ φ < 358.6	0	4	7	3	15
358.6 ≤ φ < 360.0	0	4	7	4	15

to generate the ENCDAT[0] and ENCDAT[1] input pair. This data pair is clocked into the Q1875 PTCM at one-half the rate of the input data clock. For every 2 input bits (ENCDAT[0] and ENCDAT[1]), the encoder generates 3 output bits (ENCC0, ENCC1, and ENCC2). This 3-bit output is supplied to an external 8-PSK modulator. The mapping from the 3-bit

encoder output to transmitted phase is shown (table 4). Note that for rate 2/3 8-PSK operation, the ENCDAT[2] input is not used and should be grounded.

TABLE 4. MAPPING OF RATE 2/3 8-PSK ENCODER OUTPUT TO TRANSMITTED PHASE

Encoder Output (binary)	Transmitted Phase
000	0°
001	45°
011	90°
010	135°
100	180°
101	225°
111	270°
110	315°

At the receiver (figure 12), the demodulated output is typically sampled and quantized. In this example, each channel is quantized by a 6-bit analog-to-digital converter and used to address two 4Kx8 branch metric lookup ROMs. The conversion from quantized I & Q to branch metrics and sector number can be programmed in the ROMs (table 2). Note that the conversion from I & Q to phase is phase = $\tan^{-1}(I/Q)$.

For each set of branch metrics and sector number clocked into the PTCM decoder, 2 decoded outputs are generated, DECDAT[0] and DECDAT[1]. The decoded outputs are processed by a parallel-to-serial converter that generates the final output decoded data stream. Notice that the parallel-to-serial conversion process requires a clock that is two times the frequency of the symbol clock. For rate 2/3 8-PSK modulation, the input SECTOR[3] is not used and should be grounded (pin 34).

The Q1875 TCM encoder and PTCM decoder are programmed for rate 2/3 8-PSK operation by writing to the processor interface. A register initialization for this example is shown (table 5).

Rate 3/4 16-PSK Modulation Example

For the TCM encoder (figure 13), the input data stream is processed by a serial-to-parallel converter

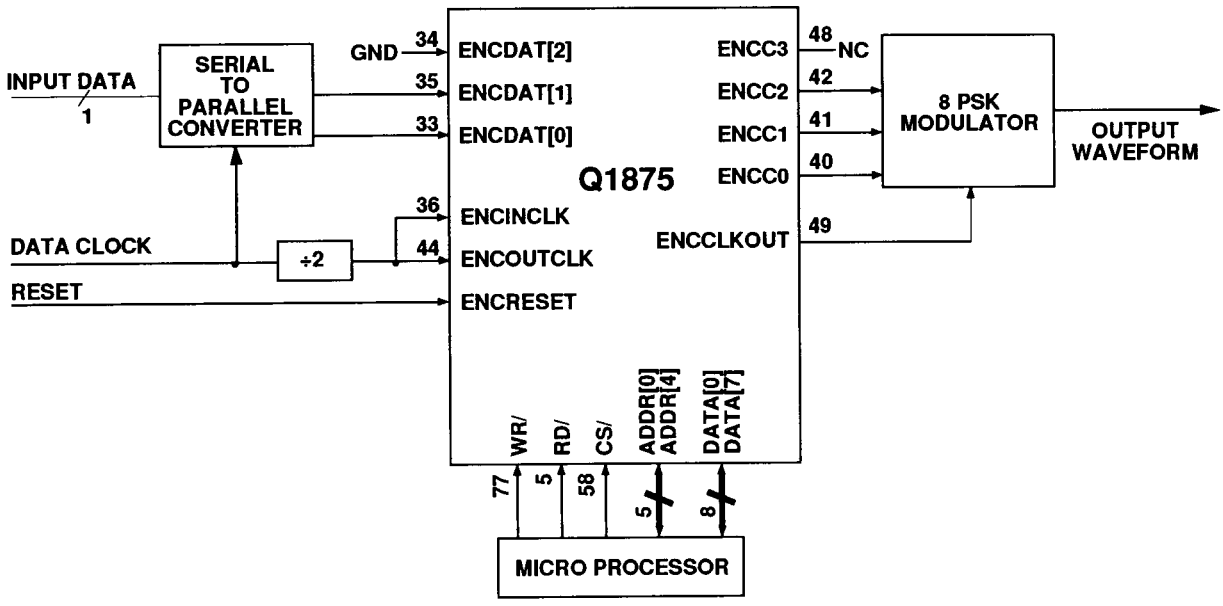


FIGURE 11. RATE 2/3 8-PSK ENCODER CONFIGURATION EXAMPLE

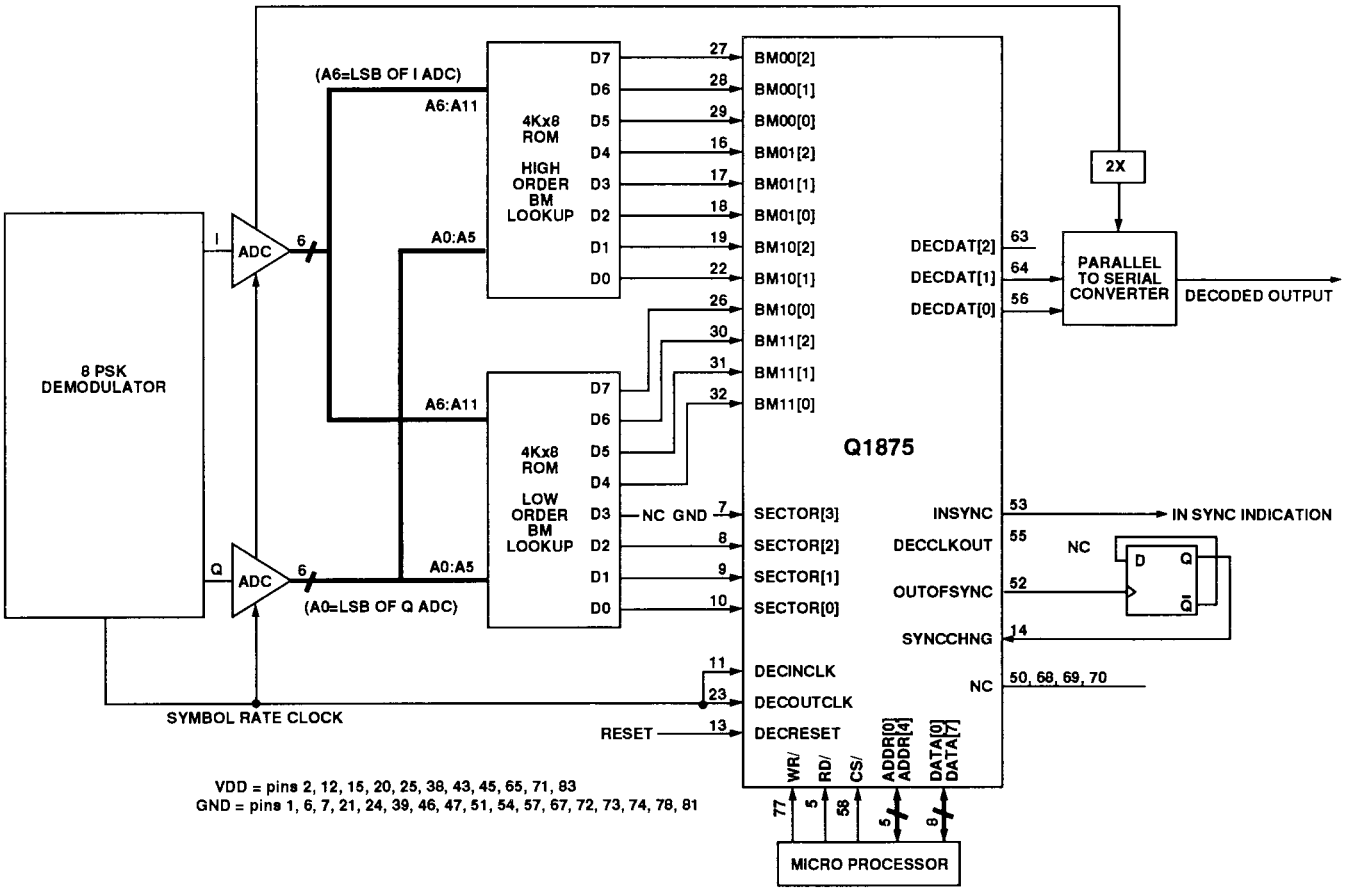


FIGURE 12. RATE 2/3 8-PSK DECODER CONFIGURATION EXAMPLE

to generate the ENCDAT[0], ENCDAT[1], and ENCDAT[2] input group. This data group is clocked into the Q1875 PTCM Decoder at one-third the rate of the input data clock. For every 3 input bits (ENCDAT[0], ENCDAT[1], and ENCDAT[2]), the encoder generates 4 output bits (ENCC0, ENCC1, ENCC2, and ENCC3). This 4-bit output is supplied to an external 16-PSK modulator. The mapping from the 4-bit encoder output to transmitted phase is shown (table 6).

At the receiver (figure 14), the demodulated output is typically sampled and quantized. In this example, each channel is quantized by a 6-bit analog-to-digital (ADC) converter and used to address two 4Kx8 branch metric lookup ROMs. The conversion from quantized I & Q to branch metrics and sector number can be programmed in the ROMs (table 2). Note, that the conversion from I & Q to phase is phase = $\tan^{-1}(I/Q)$.

For each set of branch metrics and sector number clocked into the PTCM decoder, 3 decoded outputs are generated (DECDAT[0], DECDAT[1], and DECDAT[2]). The decoded outputs are processed by a parallel-to-serial converter that generates the final output decoded data stream. Notice that the parallel-to-serial conversion process requires a clock that is three times the frequency of the symbol clock.

The Q1875 TCM encoder and PTCM decoder are programmed for rate 3/4 16-PSK operation by writing to the processor interface. An example register initialization for this example is shown (table 7).

TABLE 5. Q1875 RATE 2/3 INITIALIZATION EXAMPLE

Step	Register Name	Address	Value	Comments
1	Reserved Register	15H	00H	Reserved register must be set to 0 for correct operation.
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	C0H	Must program for correct operation
4	Decoder Control Register 2	03H	91H	Direct data mode, ambiguity decoder on
5	Decoder Control Register 3	04H	01H	Clear reset bit
6	Decoder Control Register 3	04H	05H	Set reset bit (resets decoder)
7	Normalization Test Bit-Count Input Register	08H	FEH	T count - Threshold set for 10%
8	Normalization Test Normalize-Count Input Register	09H	F9H	N count - Threshold set for 10%
9	Normalization Test Value-Enable Register	17H	XXH	A write of any value to this register begins the normalization test.
10	Encoder Control Register 2	07H	90H	Direct data mode, ambiguity resolver on
11	Encoder Control Register 1	06H	84H	Clear reset bit
12	Encoder Control Register 1	06H	86H	Set reset bit (resets encoder)

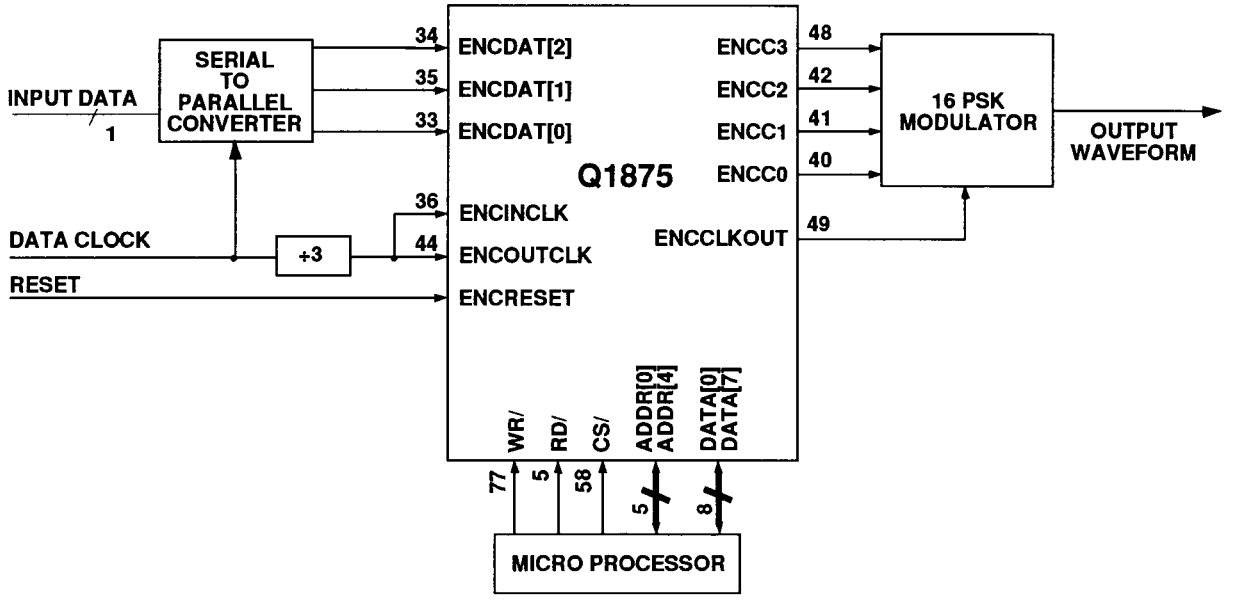


FIGURE 13. RATE 3/4 16-PSK ENCODER CONFIGURATION EXAMPLE

TABLE 6. MAPPING OF RATE 3/4 16-PSK ENCODER OUTPUT TO TRANSMITTED PHASE

Encoder Output (binary)	Transmitted Phase
0000	0°
0001	22.5°
0011	45°
0010	67.5°
0100	90°
0101	112.5°
0111	135°
0110	157.5°
1100	180°
1101	202.5°
1111	225°
1110	247.5°
1000	270°
1001	292.5°
1011	315°
1010	337.5°

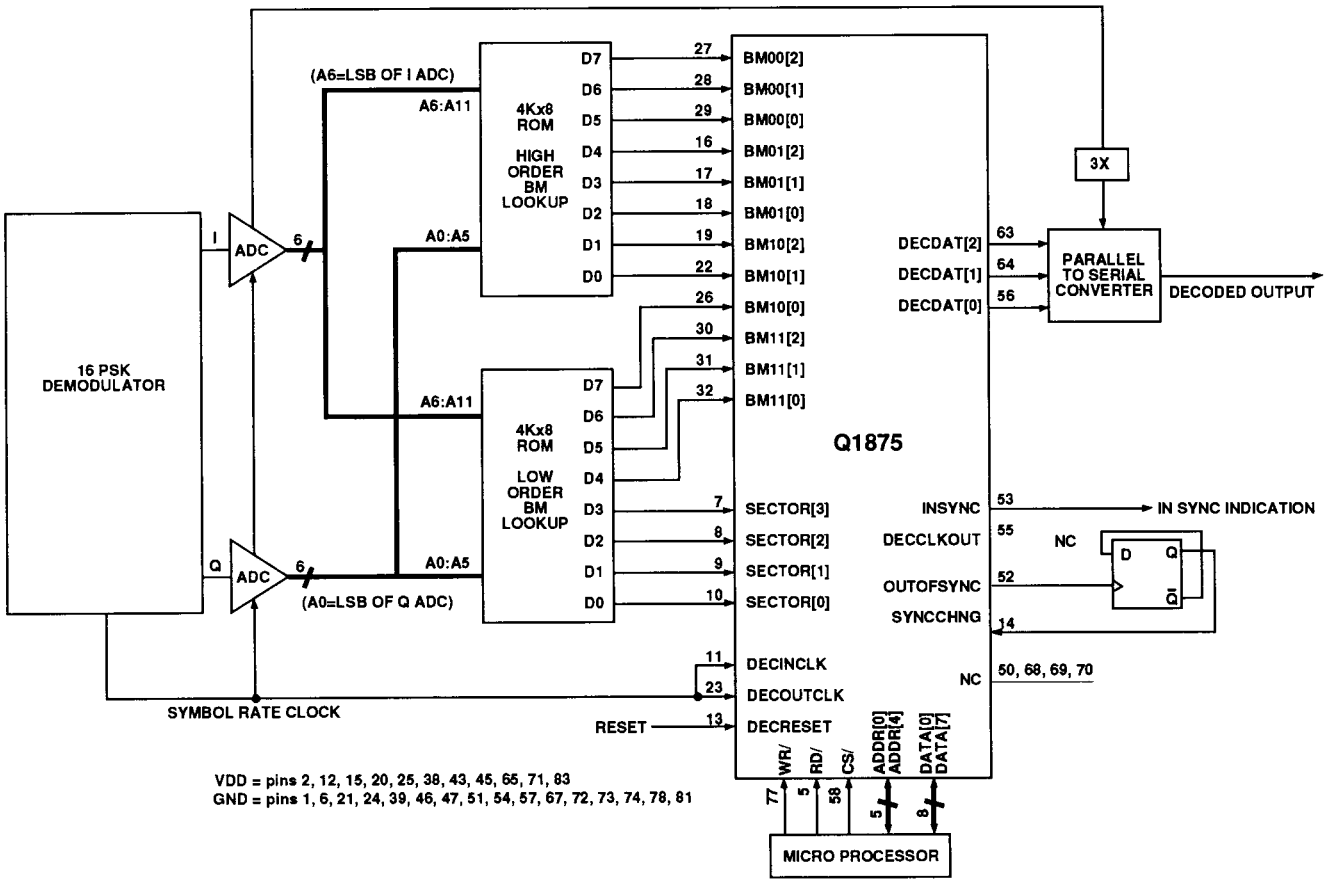


FIGURE 14. RATE 3/4 16-PSK DECODER CONFIGURATION EXAMPLE

TABLE 7. Q1875 RATE 3/4 INITIALIZATION EXAMPLE

Step	Register Name	Address	Value	Comments
1	Reserved Register	15H	00H	Reserved register must be set to 0 for correct operation.
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	C0H	Must program for correct operation
4	Decoder Control Register 2	03H	11H	Direct data mode, ambiguity decoder on
5	Decoder Control Register 3	04H	01H	Clear reset bit
6	Decoder Control Register 3	04H	05H	Set reset bit (resets decoder)
7	Normalization Test Bit-Count Input Register	08H	FEH	T count - Threshold set for 10%
8	Normalization Test Normalize-Count Input Register	09H	F9H	N count - Threshold set for 10%
9	Normalization Test Value-Enable Register	17H	XXH	A write of any value to this register begins the normalization test.
10	Encoder Control Register 2	07H	10H	Direct data mode, ambiguity resolver on
11	Encoder Control Register 1	06H	84H	Clear reset bit
12	Encoder Control Register 1	06H	86H	Set reset bit (resets encoder)

TECHNICAL SPECIFICATIONS

Processor Interface

The on-chip processor interface of the Q1875 PTCM Decoder allows a processor to set the operational mode and monitor the internal status of the device. The interface includes an 8-bit wide data bus, a 5-bit-wide address bus, and read-enable, write-enable, and chip-select lines. This interface will operate with most major microprocessor and signal processor families without wait state logic. It also can be used to write and read data to and from the encoder and decoder functions. In this mode, the Q1875 device operates as a single-chip FEC peripheral to the processor system.

The Q1875 processor interface has 2 read registers and 17 write registers (tables 8 and 9). Not all registers are required in every operational mode (tables 10 and 11).

The memory maps of the read and write registers are shown (tables 8 and 9, respectively) as are the functions of each register and bit (tables 10 and 11, respectively).

TABLE 8. Q1875 READ REGISTERS MEMORY MAP

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
		Decoder Data Output Register							
00	00	Rsvd	Rsvd	DECDAT[2]	DECDAT[1]	Rsvd	Rsvd	Rsvd	DECDAT[0]
		Encoder Data Output Register							
02	02	Rsvd	Rsvd	Rsvd	Rsvd	ENCC3	ENCC2	ENCC1	ENCC0

TABLE 9. Q1875 WRITE REGISTERS MEMORY MAP

ADDRESS DEC	ADDRESS HEX	DATA BITS D7	D6	D5	D4	D3	D2	D1	D0
		Decoder Data Input Register 1							
00	00	BM11[0]	BM01[0]	BM10[0]	BM00[0]	BM11[1]	BM01[1]	BM10[1]	BM00[1]
		Decoder Data Input Register 2							
01	01	BM11[2]	BM01[2]	BM10[2]	BM00[2]	SECTOR3	SECTOR2	SECTOR1	SECTOR0
		Decoder Control Register 1							
02	02	Set to 1	Set to 1	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
		Decoder Control Register 2							
03	03	TRL 8/16	Set to 0	Set to 0	DIFF DEC ENABLE	PERIPR/ DIRECT	Set to 0	Set to 0	Set to 1
		Decoder Control Register 3							
04	04	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	S/W DEC RESET	Set to 0	Set to 1
		Encoder Data Input Register							
05	05	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	ENCDAT[2]	ENCDAT[1]	ENCDAT[0]
		Encoder Control Register 1							
06	06	Set to 1	Set to 0	Set to 0	Set to 0	Set to 0	Set to 1	S/W ENC RESET	Set to 0
		Encoder Control Register 2							
07	07	TRL 8/16	Set to 0	Set to 0	DIFF ENC ENABLE	PERIPR/ DIRECT	Set to 0	Set to 0	Set to 0
		Normalization Test Bit-Count Input Register							
08	08	TCOUNT Bit 7 (MS)	TCOUNT Bit 6	TCOUNT Bit 5	TCOUNT Bit 4	TCOUNT Bit 3	TCOUNT Bit 2	TCOUNT Bit 1	TCOUNT Bit 0 (LS)
		Normalization Test Normalize-Count Input Register							
09	09	NCOUNT Bit 7 (MS)	NCOUNT Bit 6	NCOUNT Bit 5	NCOUNT Bit 4	NCOUNT Bit 3	NCOUNT Bit 2	NCOUNT Bit 1	NCOUNT Bit 0 (LS)
		Processor Decoder Input Clock Register							
14	0E	DECINCLK Bit 7	DECINCLK Bit 6	DECINCLK Bit 5	DECINCLK Bit 4	DECINCLK Bit 3	DECINCLK Bit 2	DECINCLK Bit 1	DECINCLK Bit 0

TABLE 9. Q1875 WRITE REGISTERS MEMORY MAP (CONTINUED)

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
		Processor Decoder Output Clock Register							
15	0F	DECOUT-CLK Bit 7	DECOUT-CLK Bit 6	DECOUT-CLK Bit 5	DECOUT-CLK Bit 4	DECOUT-CLK Bit 3	DECOUT-CLK Bit 2	DECOUT-CLK Bit 1	DECOUT-CLK Bit 0
		Processor Encoder Input Clock Register							
17	11	ENCINCLK Bit 7	ENCINCLK Bit 6	ENCINCLK Bit 5	ENCINCLK Bit 4	ENCINCLK Bit 3	ENCINCLK Bit 2	ENCINCLK Bit 1	ENCINCLK Bit 0
		Processor Encoder Output Clock Register							
18	12	ENCOUT-CLK Bit 7	ENCOUT-CLK Bit 6	ENCOUT-CLK Bit 5	ENCOUT-CLK Bit 4	ENCOUT-CLK Bit 3	ENCOUT-CLK Bit 2	ENCOUT-CLK Bit 1	ENCOUT-CLK Bit 0
		Reserved Register							
21	15	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
		Reserved Register							
22	16	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
		Normalization Test Value-Enable Register							
23	17	NTVE Bit 7	NTVE Bit 6	NTVE Bit 5	NTVE Bit 4	NTVE Bit 3	NTVE Bit 2	NTVE Bit 1	NTVE Bit 0

NOTES
1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to zero or one for proper operation.
3. **Reserved write registers 15h and 16h must be set to 0 for correct operation.**

TABLE 10. Q1875 READ REGISTERS

READ ADDRESS 00H: DECODER DATA OUTPUT REGISTER

BIT	NAME	FUNCTION	Same Function as Input Pin
0	DECDAT[0]	Decoder data output (LSB)	56
1	-	Reserved	-
2	-	Reserved	-
3	-	Reserved	-
4	DECDAT[1]	Decoder data output (CSB)	64
5	DECDAT[2]	Decoder data output (MSB)	63
6-7	–	Reserved	–

READ ADDRESS 02H: ENCODER DATA OUTPUT REGISTER

BIT	NAME	FUNCTION	Same Function as Input Pin
0	ENCC0	Encoder output (LSB)	40
1	ENCC1	Encoder output	41
2	ENCC2	Encoder output	42
3	ENCC3	Encoder output (MSB)	48
4-7	–	Reserved	–

WRITE ADDRESS 00H: DECODER DATA INPUT REGISTER 1

BIT	NAME	CONTROL/INPUT	Same Function as Input Pin
0	BM00[1]	Branch metric 00 (CSB)	28
1	BM10[1]	Branch metric 10 (CSB)	22
2	BM01[1]	Branch metric 01 (CSB)	17
3	BM11[1]	Branch metric 11 (CSB)	31
4	BM00[0]	Branch metric 00 (LSB)	29
5	BM10[0]	Branch metric 10 (LSB)	26
6	BM01[0]	Branch metric 01 (LSB)	18
7	BM11[0]	Branch metric 11 (LSB)	32

WRITE ADDRESS 01H: DECODER DATA INPUT REGISTER 2

BIT	NAME	ACCEPTS	Same Function as Input Pin
0	SECTOR0	Sector number (LSB)	10
1	SECTOR1	Sector number	9
2	SECTOR2	Sector number	8
3	SECTOR3	Sector number (MSB)	7
4	BM00[2]	Branch metric 00 (MSB)	27
5	BM10[2]	Branch metric 10 (MSB)	19
6	BM01[2]	Branch metric 01 (MSB)	16
7	BM11[2]	Branch metric 11 (MSB)	30

TABLE 11. Q1875 WRITE REGISTERS

WRITE ADDRESS 02H: DECODER CONTROL REGISTER 1

BIT	NAME	FUNCTION
0-5	-	Set to 0
6-7	-	Set to 1

WRITE ADDRESS 03H: DECODER CONTROL REGISTER 2

BIT	NAME	FUNCTION
0	-	Set to 1
1-2	-	Set to 0
3	DECODER PERIPHERAL/ DIRECT DATA MODE	1 makes decoder use processor bus interface for data input/output (peripheral mode). See "Processor Bus Interface Pins" in *Q1875 Pin Functions* (table 12). 0 makes decoder use dedicated I/O pins for data input/output (direct data mode). See "Decoder I/O Pins" in *Q1875 Pin Functions* (table 12).
4	DIFF DEC ENA	1 enables the differential decoder and ambiguity resolver decoder; 0 disables the differential decoder and ambiguity resolver decoder. (The setting of this bit does not affect the operation of the differential encoder and ambiguity resolver encoder.)
5	-	Set to 0
6	-	Set to 0
7	8-PSK/16-PSK	1 selects rate $^{2}/_{3}$ 8-PSK operation, 0 selects rate $^{3}/_{4}$ 16-PSK operation.

WRITE ADDRESS 04H: DECODER CONTROL REGISTER 3

0	-	Set to 1
1	-	Set to 0
2	S/W DECODER RESET	A transition from 0 to 1 resets decoder functions (similar to pin 13). Connect pin 13 to logic 0 when using this software-controlled reset. Bit 2 should be set to 0 when using the DECRESET pin.
3-7	–	Set to 0

WRITE ADDRESS 05H: ENCODER DATA INPUT REGISTER

BIT	NAME	FUNCTION
0	ENCDAT[0]	If: Encoder peripheral mode enabled Then: Accepts encoder data (same function as pin 33)
1	ENCDAT[1]	If: Encoder peripheral mode enabled Then: Accepts encoder data (same function as pin 35)
2	ENCDAT[2]	If: Encoder peripheral mode enabled Then: Accepts encoder data (same function as pin 34)
3-6	-	Set to 0
7	-	Set to 1

TABLE 11. Q1875 WRITE REGISTERS (CONTINUED)

WRITE ADDRESS 06H: ENCODER CONTROL REGISTER 1

BIT	NAME	FUNCTION
0	-	Set to 0
1	S/W ENCODER RESET	A transition from 0 to 1 resets decoder functions (similar to pin 37). Connect pin 37 to logic 0 when using this software-controlled reset. Bit 1 should be set to 0 when using the ENCRESET pin.
2	-	Set to 1
3-6	-	Set to 0
7	-	Set to 1

WRITE ADDRESS 07H: ENCODER CONTROL REGISTER 1

BIT	NAME	FUNCTION
0-2	–	Set to 0
3	ENCODER PERIPHERAL/ DIRECT DATA MODE	1 makes encoder use processor bus interface for data input/output (peripheral mode). See "Processor Bus Interface Pins" in *Q1875 Pin Functions* (table 12). 0 makes encoder use I/O pins for data input/output (direct data mode). See "Encoder I/O Pins" in *Q1875 Pin Functions* (table 12).
4	DIFF ENC ENA	1 enables differential encoder and ambiguity resolver encoder; 0 disables differential encoder and ambiguity resolver encoder. (The setting of this bit does not affect the operation of the differential decoder and ambiguity resolver decoder.)
5	-	Set to 0
6	-	Set to 0
7	8-PSK/16-PSK	1 selects rate $^2/_3$ 8-PSK operation, 0 selects rate $^3/_4$ 16-PSK operation.

WRITE ADDRESS 08H: NORMALIZATION TEST BIT-COUNT INPUT REGISTER

BIT	NAME	FUNCTION
0-7	T COUNT (Bit 0 is LSB)	Determines the length of the synchronization monitor test; requires an 8-bit value See *Normalization Rate Monitor Operation* for more information.

WRITE ADDRESS 09H: NORMALIZATION TEST NORMALIZE-COUNT INPUT REGISTER

BIT	NAME	FUNCTION
0-7	N COUNT (Bit 0 is LSB)	Determines the normalization threshold level for the synchronization monitor test; requires an 8-bit value See *Normalization Rate Monitor Operation* for more information.

WRITE ADDRESS 0EH: PROCESSOR DECODER INPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	DECINCLK (software-controlled)	Generates (when given any value) a single DECINCLK clock cycle. Connect pin 11 (DECINCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 0FH: PROCESSOR DECODER OUTPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	DECOUTCLK (software-controlled)	Generates (when given any value) a single DECOUTCLK clock cycle. Connect pin 23 (DECOUTCLK) to logic 0 when using this software-controlled clock.

TABLE 11. Q1875 WRITE REGISTERS (CONTINUED)

WRITE ADDRESS 11H: PROCESSOR ENCODER INPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	ENCINCLK (software-controlled)	Generates (when given any value) a single ENCINCLK clock cycle. Connect pin 36 (ENCINCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 12H: PROCESSOR ENCODER OUTPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	ENCOUTCLK (software-controlled)	Generates (when given any value) a single ENCOUTCLK clock cycle. Connect pin 44 (ENCOUTCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 17H: NORMALIZATION TEST VALUE-ENABLE REGISTER

BIT	NAME	FUNCTION
0-7	Norm Test Values Enable (software-controlled)	Performs two functions (when given any value): 1) Enables the values previously loaded into these registers: Normalization Test Bit-Count Register (write address 08H) Normalization Test Normalize-Count Register (write address 09H) . 2) Restarts the normalization rate test

NOTES
1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to zero or one for proper operation.
3. **Reserved write registers 15h and 16h must be set to 0 for correct operation.**

Pin Descriptions

Following are descriptions of the pin locations (figure 15) and the pin functions (table 12) for the Q1875 PTCM Decoder when operating in PTCM mode.

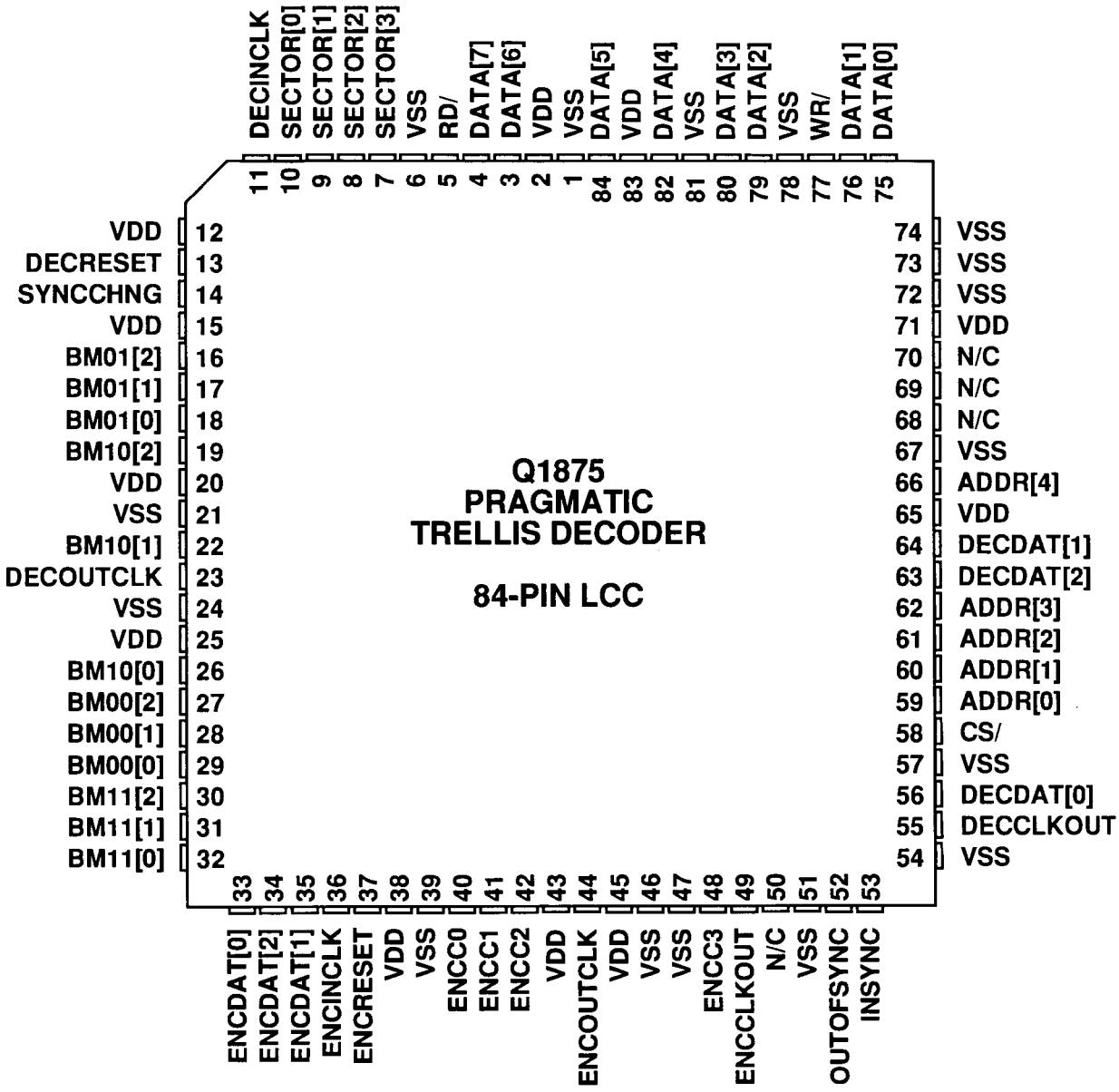


FIGURE 15. Q1875 PINOUT DIAGRAM

TABLE 12. Q1875 PIN FUNCTIONS

	Name	Pins	Type	Function
Encoder I/O Pins	ENCDAT[0]	33	Input	Encoder data input (LSB)
	ENCDAT[1]	35	Input	Encoder data input (CSB)
	ENCDAT[2]	34	Input	Encoder data input (MSB) (Note 1)
	ENCINCLK	36	Input	Encoder data input clock
	ENCOUTCLK	44	Input	Encoder symbol output clock
	ENCCLKOUT	49	Output	Encoder symbol clock output
	ENCC0	40	Output	Encoder output (LSB)
	ENCC1	41	Output	Encoder output
	ENCC2	42	Output	Encoder output
	ENCC3	48	Output	Encoder output (MSB) (Note 2)
	ENCRESET	37	Input	Master encoder reset (active high)
Decoder I/O Pins	BM00[0, 1, 2]	29 (LSB), 28, 27	Input	Branch metric input 00
	BM01[0, 1, 2]	18 (LSB), 17, 16	Input	Branch metric input 01
	BM10[0, 1, 2]	26 (LSB), 22, 19	Input	Branch metric input 10
	BM11[0, 1, 2]	32 (LSB), 31, 30	Input	Branch metric input 11
	SECTOR[0]	10	Input	Sector number (LSB)
	SECTOR[1]	9	Input	Sector number
	SECTOR[2]	8	Input	Sector number
	SECTOR[3]	7	input	Sector number (MSB) (Note 1)
	DECINCLK	11	Input	Decoder symbol input clock
	DECOUTCLK	23	Input	Decoder data output clock
	DECCLKOUT	55	Output	Decoder data clock output
	DECRESET	13	Input	High master resets decoder circuitry
	SYNCCHNG	14	Input	Decoder sync change control (active high)
	OUTOFSYNC	52	Output	Sync monitor test failure (Note 3)
	INSYNC	53	Output	Sync monitor test pass (Note 4)
	DECDAT[0]	56	Output	Decoder data output (LSB)
	DECDAT[1]	64	Output	Decoder data output (CSB)
	DECDAT[2]	63	Output	Decoder data output (MSB) (Note 2)
Processor Bus Interface Pins	DATA[0]–DATA[7]	75, 76,79, 80, 82, 84, 3, 4	I/O	Processor interface data bus (DATA[0] is LSB)
	ADDR[0]–ADDR[4]	59 (LSB) , 60, 61, 62, 66	Input	Processor interface address bus
	WR/	77	Input	Processor interface write strobe (active low)
	RD/	5	Input	Processor interface read strobe (active low)
	CS/	58	Input	Processor interface chip select (active low)
Voltage Supply Pins	VDD (+5V)	2, 12, 15, 20, 25, 38, 43, 45, 65, 71, 83	Power	
	VSS	1, 6, 21, 24, 39, 46, 47, 51, 54, 57, 67, 72, 73, 74, 78, 81	Ground	
	N/C	50, 68, 69, 70	Unused	Make no connection to this pin.

NOTES
1. This input is used only for rate 3/4 16-PSK mode. This input should be set to a logic low when not used.
2. This is valid for rate 3/4 16-PSK mode only.
3. Pin 52 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test fails.
4. Pin 53 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test passes.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	T_S	-55	+85	°C
Operating Temperature (Q1875I-1N)	T_A	-40	+85	°C
Operating Temperature (Q1875C-8N, 30N, 60L)	T_A	0	+70	°C
Junction Temperature	T_J		+160	°C
Voltage on any Input Pin		-0.3	Vdd+0.3	V
Voltage on Vdd and on any Output Pin		-0.3	+7.0	V
DC Input Current	I_{IN}	-10	+10	µA

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

DC Electrical Characteristics

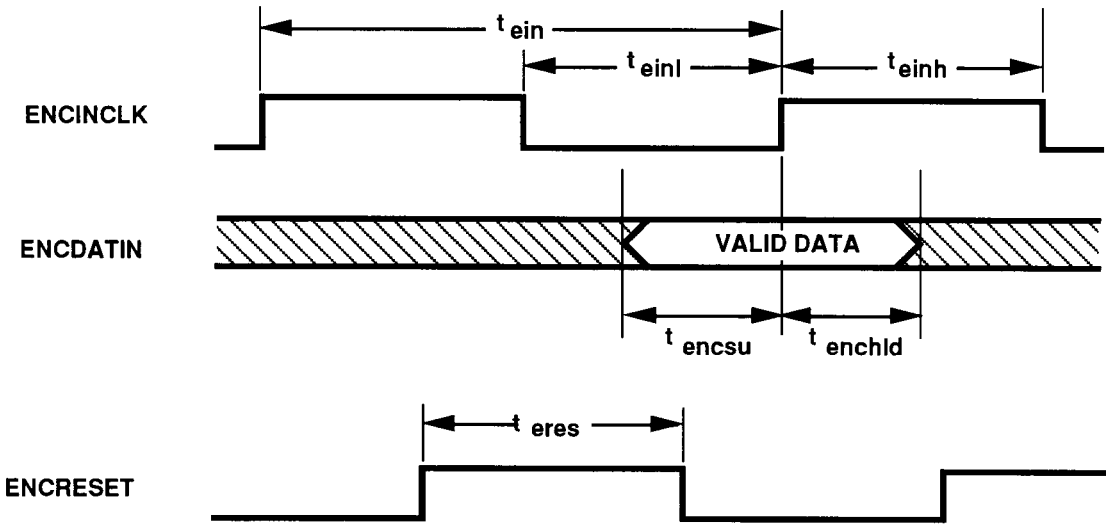
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (Q1875I-1N)	V_{DD}	4.5	5.5	V	
Supply Voltage (Q1875C-8N, 30N, 60L)	V_{DD}	4.75	5.25	V	
High-Level Input Voltage	V_{IH}	2.0	Vdd+0.3	V	
Low-Level Input Voltage	V_{IL}	-0.3	0.8	V	
Input Leakage Current	I_L	–	1.0	µA	
High-Level Output Voltage	V_{OH}	2.4	–	V	I_{OH} = -1.6 mA
Low-Level Output Voltage	V_{OL}	–	0.4	V	I_{OL} = 1.6 mA
Output Short Circuit Current*	I_{OS}	100	300	mA	
Output Capacitance	C_{OUT}		10	pF	
Power Dissipation (Quiescent)	P_D	–	0.1	W	
Power Dissipation (@256 KHz)	P_D	–	0.15	W	
Power Dissipation (@10 MHz)	P_D	–	0.8	W	

* Not more than one output shorted at a time for less than one second

Timing

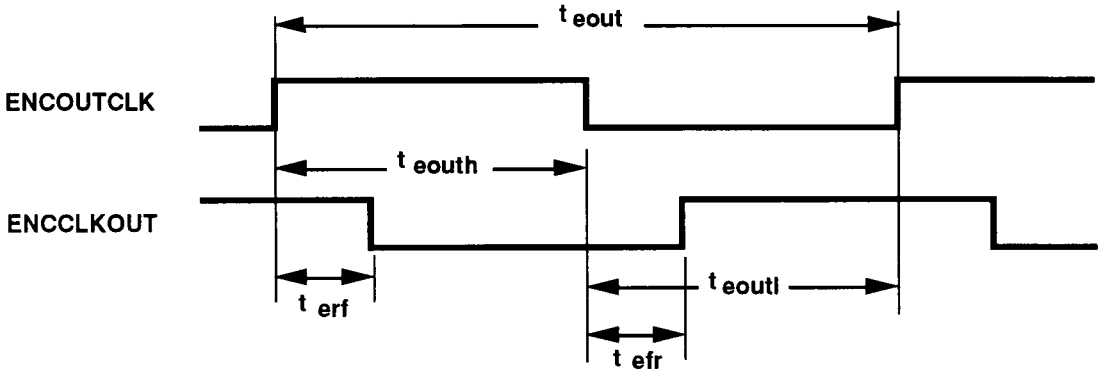
Following are timing specifications for all versions of the Q1875 device. These specifications are valid only for the recommended operating conditions.

Encoder Data Input Timing



		Q1875I-1N		Q1875C-8N		Q1875C-30N		Q1875C-60L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
ENCINCLK	Max Frequency (=1/tein)	–	0.256	–	2.5	–	10	–	20	MHz
tein	ENCINCLK period	3900		400	–	100	–	50	–	ns
tencsu	ENCDATIN setup to ENCINCLK rise	10		10	–	10	–	10	–	ns
tenchld	ENCDATIN hold after ENCINCLK rise	5		5	–	5	–	5	–	ns
teinl	ENCINCLK low period	1560		160	–	40	–	16	–	ns
teinh	ENCINCLK high period	1560		160	–	40	–	16	–	ns
teres	Minimum reset period	7800		800	–	200	–	100	–	ns

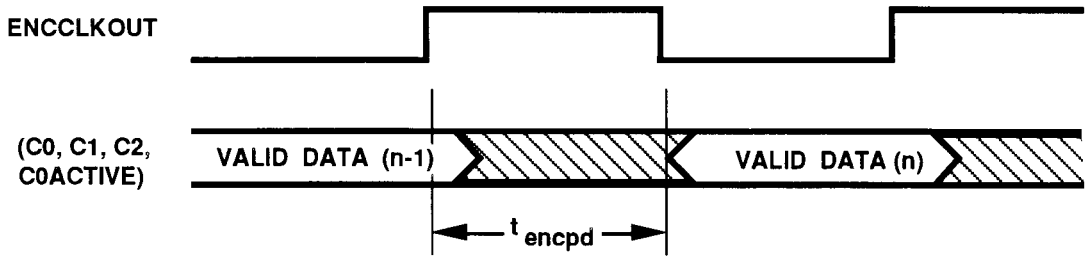
Encoder Clock Timing



		Q1875I-1N		Q1875C-8N		Q1875C-30N		Q1875C-60L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
ENCOUTCLK	Max Frequency (=1/teout)	–	0.256	–	2.5	–	10	–	20	MHz
teout	ENCOUTCLK minimum period	3900	–	400	–	100	–	50	–	ns
teoutl	ENCOUTCLK low period	1560	–	160	–	40	–	16	–	ns
teouth	ENCOUTCLK high period	1560	–	160	–	40	–	16	–	ns
terf *	ENCOUTCLK rise to ENCCLKOUT fall	0	12	0	12	0	12	0	12	ns
tefr *	ENCOUTCLK fall to ENCCLKOUT rise	0	12	0	12	0	12	0	12	ns

* Assumes a 25 pF load on the output pin

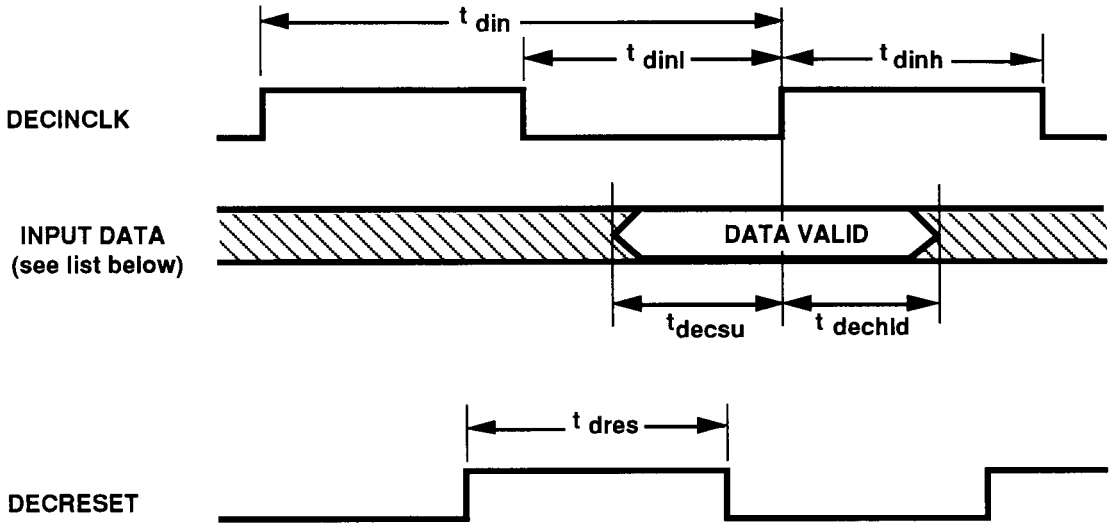
Encoder Data Output Timing



		Q1875I-1N		Q1875C-8N		Q1875C-30N		Q1875C-60L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{encpd}*	Data valid after clock output rising	1	18	1	18	1	18	1	18	ns

*Assumes a 25 pF load on the output pin

Decoder Data Input Timing

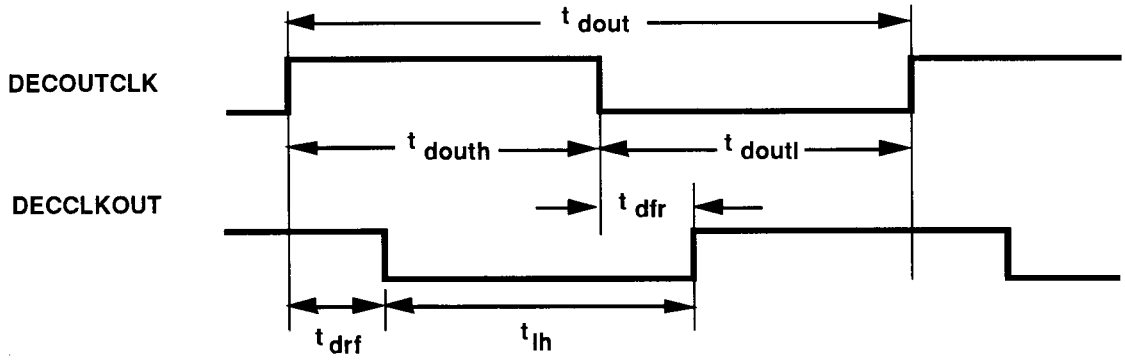


Input data includes:

BM00[2]	BM00[1]	BM00[0]	SECTOR[0]	SYNCCHNG
BM01[2]	BM01[1]	BM01[0]	SECTOR[1]	
BM10[2]	BM10[1]	BM10[0]	SECTOR[2]	
BM11[2]	BM11[1]	BM11[0]	SECTOR[3]	

		Q1875I-1N		Q1875C-8N		Q1875C-30N		Q1875C-60L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
DECINCLK	Max Frequency (=1/tdin)	–	0.256	–	2.5	–	10	–	20	MHz
tdin	Minimum period	3900	–	400	–	100	–	50	–	ns
tdecsu	Data setup to DECINCLK rise	10	–	10	–	10	–	10	–	ns
tdechld	Data hold after DECINCLK rise	5	–	5	–	5	–	5	–	ns
tdinl	DECINCLK low period	1560	–	160	–	40	–	16	–	ns
tdinh	DECINCLK high period	1560	–	160	–	40	–	16	–	ns
tdres	Minimum reset period	7800	–	800	–	200	–	100	–	ns

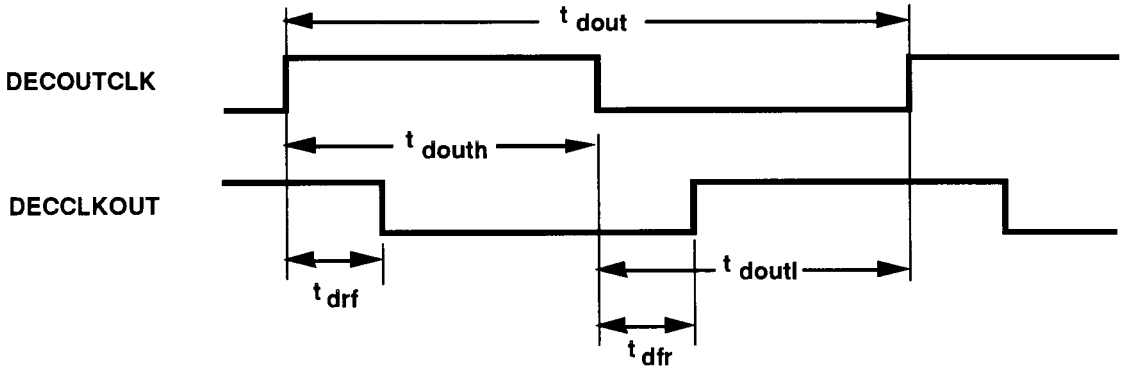
Decoder Clock Timing (Q1875I-1N and Q1875C-8N)



		Q1875I-1N		Q1875C-8N		
Signal	Description	Min	Max	Min	Max	Units
DECOUTCLK	Max Frequency (=1/tdout)	–	0.256	–	2.5	MHz
tdout	DECOUTCLK minimum period	3900		400	–	ns
tdoutl	DECOUTCLK low period	1560		160	–	ns
tdouth	DECOUTCLK high period	1560		160	–	ns
tdrf	DECOUTCLK rise to DECCLKOUT fall*	0	35	0	35	ns
tlh	DECCLKOUT fall to DECCLKOUT rise*	10	–	10	–	ns
tdfr**	DECOUTCLK fall to DECCLKOUT rise*	–	20	–	20	ns

* Assumes a 25 pF load on the output pin
** The rising edge of DECCLKOUT may rise prior to the falling edge of DECOUTCLK.

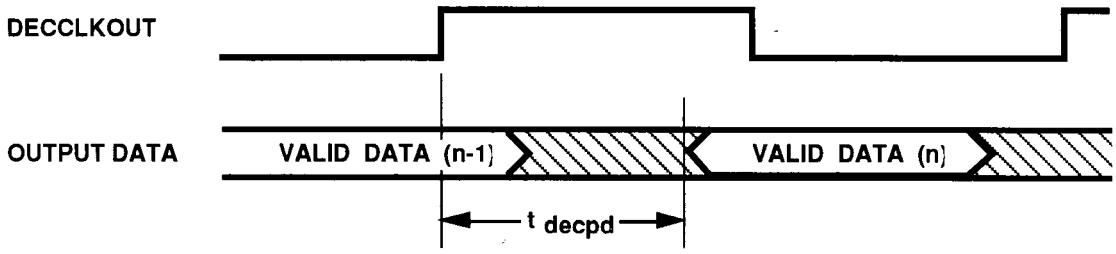
Decoder Clock Timing (Q1875C-30N and Q1875C-60L)



		Q1875C-30N		Q1875C-60L		
Signal	Description	Min	Max	Min	Max	Units
DECOUTCLK	Max Frequency (=1/tdout)	–	10	–	25	MHz
tdout	DECOUTCLK minimum period	100	–	40	–	ns
tdoutl	DECOUTCLK low period	40	–	16	–	ns
tdouth	DECOUTCLK high period	40	–	16	–	ns
tdrf	DECOUTCLK rise to DECCLKOUT fall*	0	20	0	20	ns
tdfr	DECOUTCLK fall to DECCLKOUT rise*	0	20	0	20	ns

*Assumes a 25 pF load on the output pin

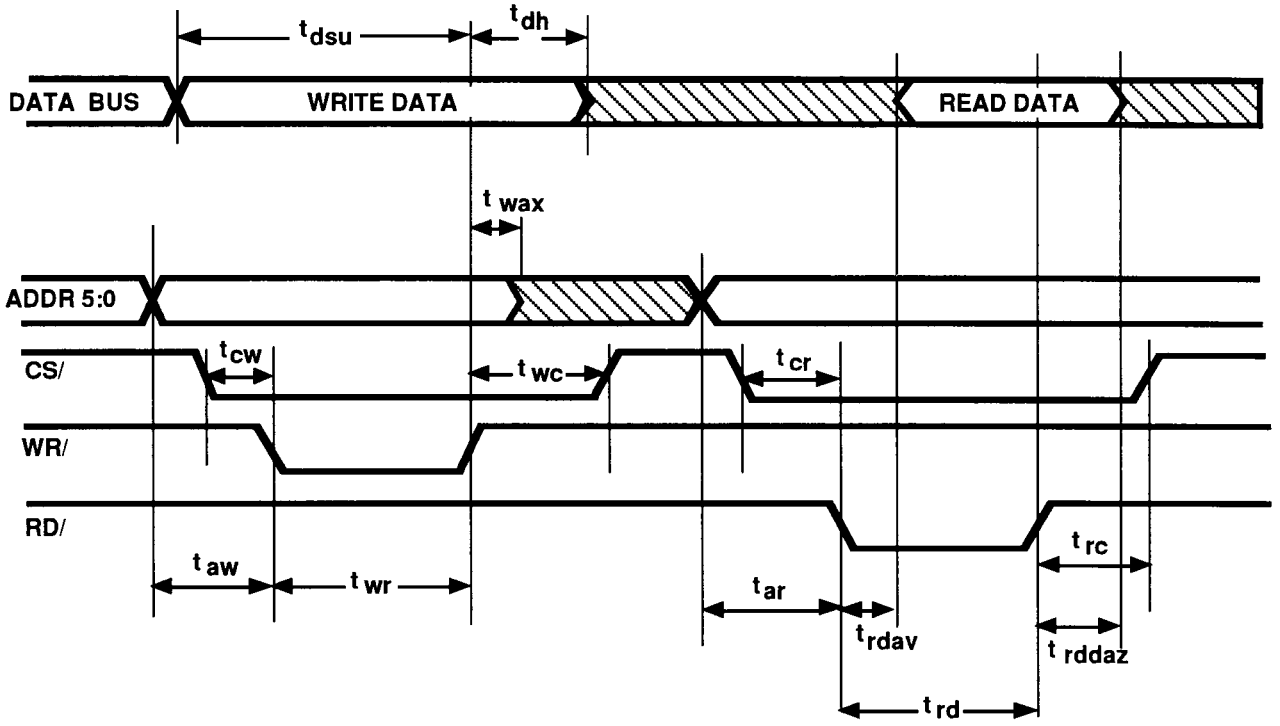
Decoder Data Output Timing



		Q1875I-1N		Q1875C-8N		Q1875C-30N		Q1875C-60L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{decpd}	Data valid after output clock rising	-	40	-	40	1	18	1	18	ns

NOTES
1. Value assumes a 25 pF load on the output pin.
2. Output data includes DECDAT[0], DECDAT[1], DECDAT[2], INSYNC, and OUTOFSYNC.

Processor Interface Timing



		Q1875I-1N, C-8N, -30N, -60L		
Write Signal	Description	Min	Max	Units
t_{dsu}	Data setup to WR/ rising	20	–	ns
t_{dh}	Data hold after WR/ rising	5	–	ns
t_{cw}	CS/ falling to WR/ falling	15	–	ns
t_{wax}	Address hold after WR/ rising	5	–	ns
t_{wc}	CS/ hold after WR/ rising	5	–	ns
t_{aw}	Address valid to WR/ falling	20	–	ns
t_{wr}	WR/ period	80	–	ns
t_{ar}	Address valid to RD/ falling	20	–	ns
t_{rd}	RD/ period	80	–	ns
t_{cr}	CS/ falling to RD/ falling	15	–	ns
t_{rc}	CS/ hold after RD/ rising	5	–	ns
t_{rdav}	RD/ falling to DATA valid	60	–	ns
t_{rddaz}	Data hold after RD/ rising	0	–	ns

PLCC Packaging (Q1875I-1N, Q1875C-8N, and Q1875C-30N)

The Q1875I-1N, Q1875C-8N, and Q1875C-30N devices are packaged in an 84-pin plastic leaded chip carrier (PLCC) (figure 16). A suggested socket is AMP P/N 821573-1 (through-hole board mounted) or P/N 822151-5 (surface mounted). Dimensions are given in inches (mm).

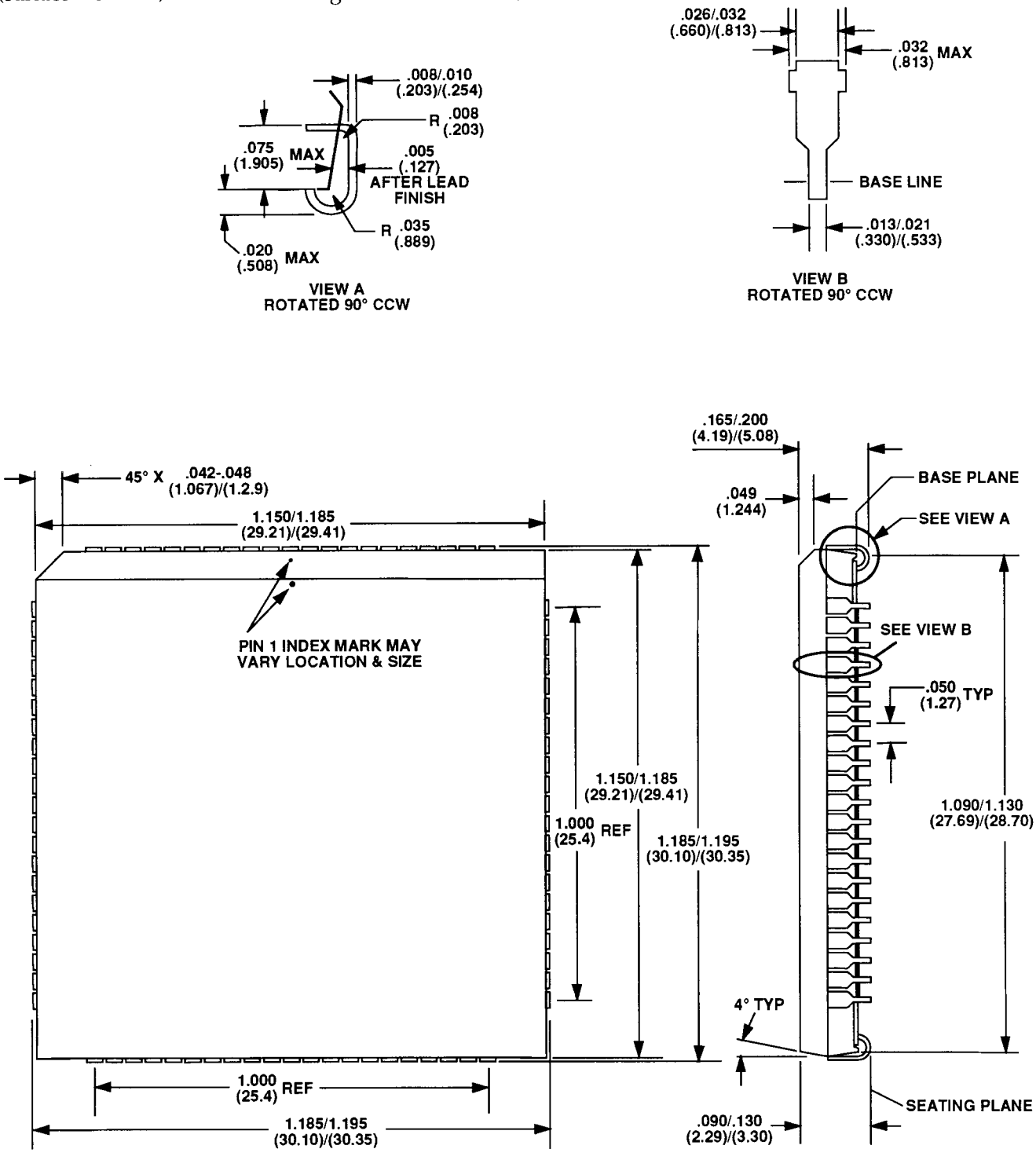


FIGURE 16. PLCC PACKAGING

CLDCC Packaging (Q1875C-60L)

The Q1875C-60L device is packaged in an 84-pin ceramic leaded chip carrier (CLDCC) (figure 17). A suggested socket is AMP P/N 643066-2 (through-hole board mounted) or P/N 643151-2 (surfaced mounted). Dimensions are given in inches (mm).

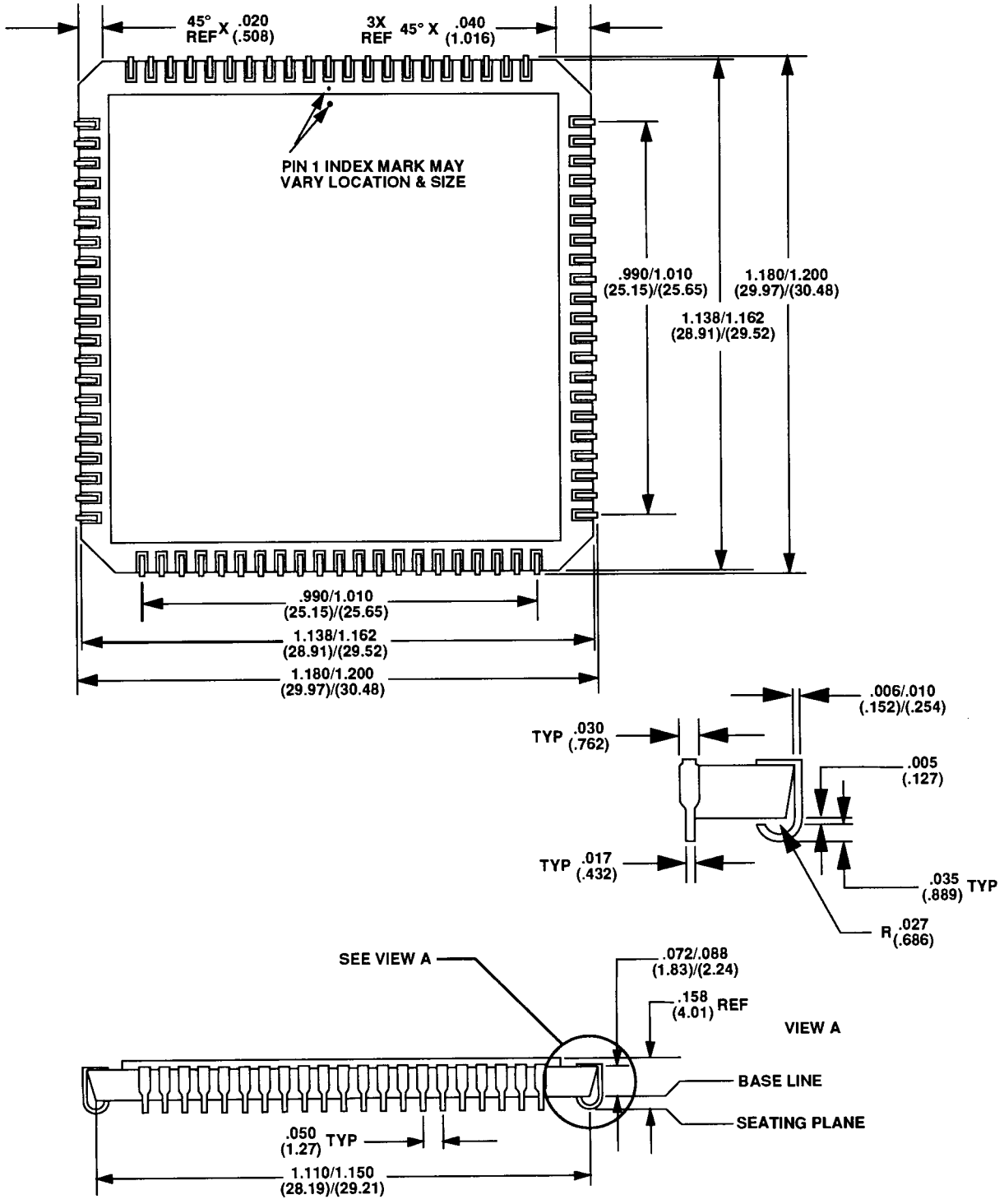


FIGURE 17. CLDCC PACKAGING

REFERENCES

Viterbi Decoding Theory

Bartee, T.C., 1986. *Data Communications, Networks, and Systems.* Indianapolis, Ind.: Howard W. Sams & Co.

Clark, G.C., Jr. and J. B. Cain, 1981. *Error Correction Coding for Digital Communications.* New York: Plenum Press.

Forney, G.D., Jr. "The Viterbi Algorithm," *IEEE Transactions on Information Theory,* vol. IT-15: 177-179.

Viterbi, A.J., 1971. "Convolutional Codes and Their Performance in Communication Systems," *IEEE Transactions on Communication Technology,* vol. COM-19: 751-772.

Trellis-Coded Modulation

Ungerboeck, G., 1987a. "Trellis-Coded Modulation with Redundant Signal Sets-Part I: Introduction," *IEEE Communications Magazine* , vol. 25: 5-11.

Ungerboeck, G., 1987b. "Trellis-Coded Modulation with Redundant Signal Sets-Part II: State of the Art," *IEEE Communications Magazine* , vol. 25: 12-21.

Ungerboeck, G., 1982. "Channel Coding with Multilevel/phase Signals," *IEEE Transactions on Information Theory,* vol. IT-28: 55-67.

U.S. Patent and Trademark Office. QUALCOMM Incorporated. *Viterbi Decoder Bit Efficient Chainback Memory Method and Decoder Incorporation.* (Patent pending).

Viterbi, A.J., J.K. Wolf, and E. Zehavi, 1988. "Trellis-Coded MPSK Modulation for Highly Efficient Military Satellite Applications," *MILCOM88.* New York: The Institute of Electrical and Electronics Engineers, Inc.

Viterbi, A. J., J. K. Wolf, E. Zehavi, and R. Padovani, 1989. "A Pragmatic Approach to Trellis-Coded Modulation," *IEEE Communications Magazine* vol. 27: 11-19.

Wolf, J. K. and G. Ungerboeck, 1986. "Trellis Coding for Partial-Response Channels," *IEEE Transactions on Communications,* vol. COM-34: 765-773.

Zehavi, Ephraim and Gideon Kaplan, 1991. "Phase Noise Effects on *M*-ary PSK Trellis Codes," *IEEE Transactions on Communications,* vol. 39: 373-379.

Data Scrambling Algorithm

CCITT Recommendation *Data Transmission at 48 Kilobits per Second Using 60-108 KHZ group Band Circuits,* Fascicle VIII.1, Rec. V.35, Appx. I

Phase Ambiguity Resolver

U.S. Patent and Trademark Office. QUALCOMM Incorporated. *Method and Apparatus for Resolving Phase Ambiguities in Trellis-Coded Modulated Data.* (U.S. and foreign patents pending).

Related Technical Data Sheets

QUALCOMM, Incorporated, 1991. *Q1650 k=7 Multi-Code Rate Viterbi Decoder Technical Data Sheet.*

QUALCOMM, Incorporated, 1991. *Q0256 k=7 Multi-Code Rate Viterbi Decoder Technical Data Sheet.*

GLOSSARY

AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keyed
CLDCC	Ceramic Leaded Chip Carrier
CMOS	Complementary Metallic Oxide Semiconductor
dB	Decibel
DBS	Direct Broadcast System
FEC	Forward Error Correction
k	Constraint Length
LCC	Leaded Chip Carrier (either PLCC or CLDCC)
Mbps	Million Bits Per Second; refers to the encoder data input rate and the decoder data output rate.
PLCC	Plastic Leaded Chip Carrier
PTCM	Pragmatic Trellis-Coded Modulation
ROM	Read-Only Memory
QPSK	Quadrature Phase Shift Keyed
TCM	Trellis-Coded Modulation
VSAT	Very Small Aperture Terminal

ORDERING INFORMATION

Maximum Data Rate (8-PSK)	Maximum Data Rate (16-PSK)	Plastic Package (PLCC)	Ceramic Package (CLDCC)	Special Packages and Military Versions
512 Kbps	768 Kbps	Q1875I-1N	N/A	Contact QUALCOMM
5 Mbps	7.5 Mbps	Q1875C-8N	N/A	Contact QUALCOMM
20 Mbps	30 Mbps	Q1875C-30N	N/A	Contact QUALCOMM
40 Mbps	60 Mbps	N/A	Q1875C-60L	Contact QUALCOMM

For more information or to place an order, contact your local QUALCOMM Engineering Representative or contact QUALCOMM directly:

QUALCOMM Incorporated
VLSI Products Division
10555 Sorrento Valley Road
San Diego, CA 92121-1617 USA

VLSI Products Division: (619) 597-5005
Main Switchboard: (619) 587-1121
FAX: (619) 452-9096