

MOS INTEGRATED CIRCUIT

μ PD42S17405L, 4217405L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM

4 M-WORD BY 4-BIT, HYPER PAGE MODE (EDO)

Description

The μ PD42S17405L, 4217405L are 4,194,304 words by 4 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μ PD42S17405L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

The μ PD42S17405L, 4217405L are packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 4 bits organization
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μ PD42S17405L-A60, 4217405L-A60	360 mW	60 ns	104 ns	25 ns
μ PD42S17405L-A70, 4217405L-A70	324 mW	70 ns	124 ns	30 ns

- μ PD42S17405L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S17405L	2,048 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	0.54 mW (CMOS level input)
μ PD4217405L	2,048 cycles/32 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	1.8 mW (CMOS level input)

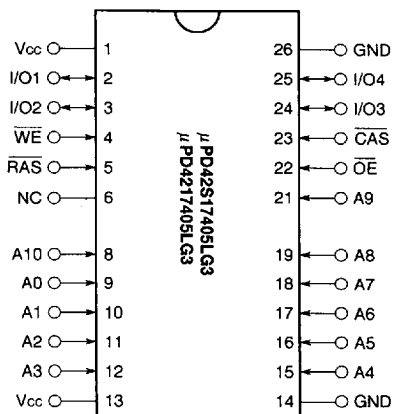
The information in this document is subject to change without notice.

Ordering Information

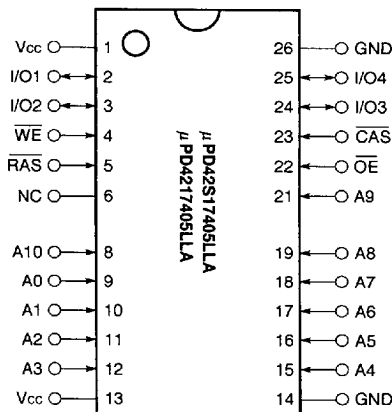
Part number	Access time (MAX.)	Package	Refresh
μPD42S17405LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
μPD42S17405LG3-A70	70 ns		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S17405LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S17405LLA-A70	70 ns		
μPD4217405LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4217405LG3-A70	70 ns		
μPD4217405LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD4217405LLA-A70	70 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

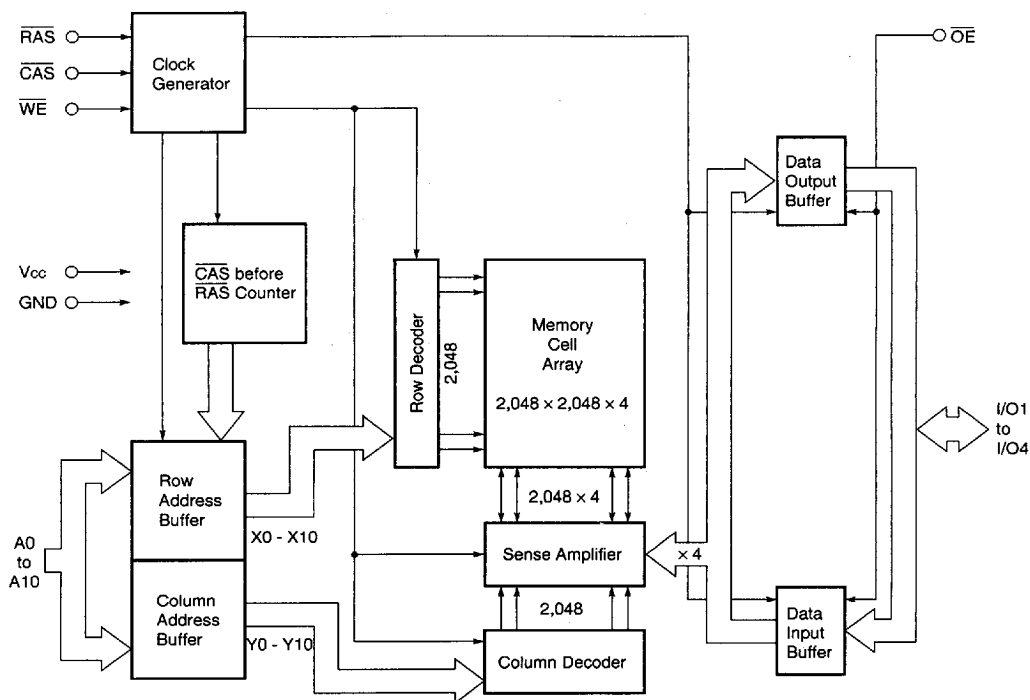


26-pin Plastic SOJ (300 mil)



A0 to A10 : Address Inputs
 I/O1 to I/O4: Data Inputs/Outputs
 RAS : Row Address Strobe
 CAS : Column Address Strobe
 WE : Write Enable
 OE : Output Enable
 Vcc : Power Supply
 GND : Ground
 NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S17405L, 4217405L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A10 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 11-bit and lower 11-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

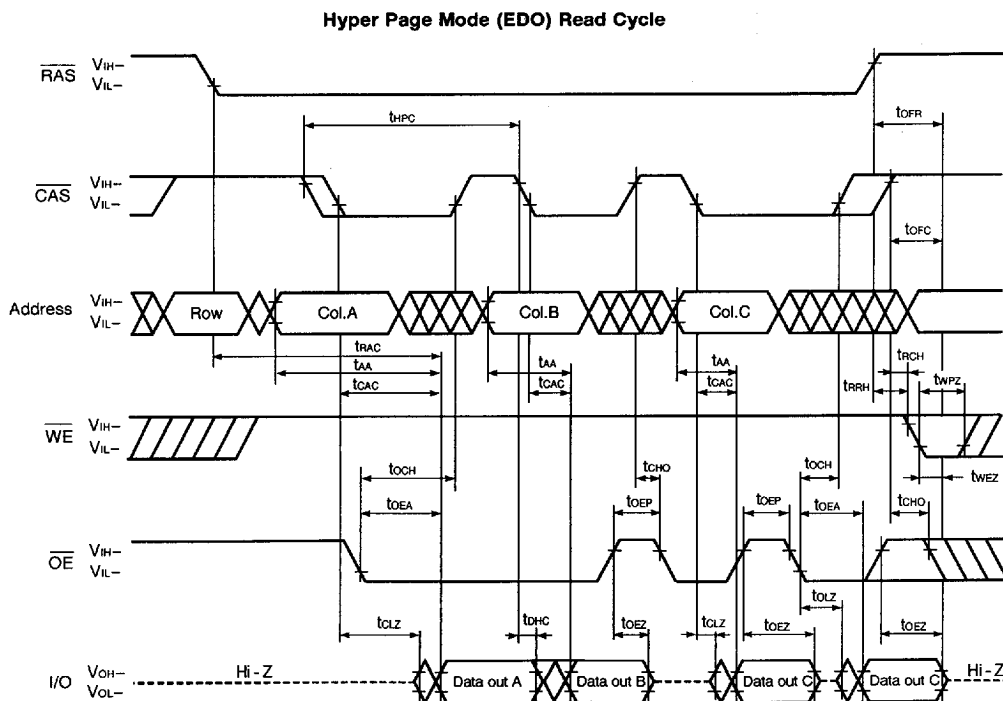
2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

In the hyper page mode (EDO), due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.



Cautions when using the hyper page mode (EDO)

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)
 $\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active
 t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.
 t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.
 - (3) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
 - (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 - (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than $100 \mu s$ ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	$^{\circ}C$
Storage temperature	T_{stg}		-55 to +125	$^{\circ}C$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	$^{\circ}C$

Capacitance ($T_A = 25^{\circ}C$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

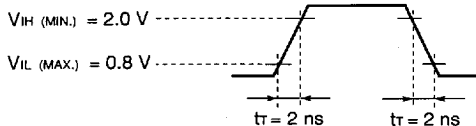
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC(MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 60$ ns	100	mA	1, 2, 3
				$t_{RAC} = 70$ ns	90		
Standby current	μPD42S17405L	I _{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, $I_O = 0$ mA		0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_O = 0$ mA		0.15		
	μPD4217405L		$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, $I_O = 0$ mA		2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_O = 0$ mA		0.5		
$\overline{RAS}$ only refresh current		I _{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 60$ ns	100	mA	1, 2, 3, 4
				$t_{RAC} = 70$ ns	90		
Operating current (Hyper page mode (EDO))		I _{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC(MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 60$ ns	90	mA	1, 2, 5
				$t_{RAC} = 70$ ns	80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I _{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC(MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 60$ ns	100	mA	1, 2
				$t_{RAC} = 70$ ns	90		
CAS before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17405L)		I _{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: $t_{RC} = 62.5$ μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} WE, OE: V_{IH} $I_O = 0$ mA	$t_{RAS} \leq 1$ μs	200	μA	1, 2
CAS before $\overline{RAS}$ self refresh current (only for the μPD42S17405L)		I _{CC7}	$\overline{RAS}$, $\overline{CAS}$: $t_{RASS} = 5$ ms $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ 0 V $\leq V_{IL} \leq 0.2$ V $I_O = 0$ mA		150	μA	2
Input leakage current		I _{I(L)}	$V_I = 0$ to 3.6 V All other pins not under test = 0 V	-5	+5	μA	
Output leakage current		I _{O(L)}	$V_O = 0$ to 3.6 V Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage		V _{OH}	$I_O = -2.0$ mA	2.4		V	
Low level output voltage		V _{OL}	$I_O = +2.0$ mA		0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

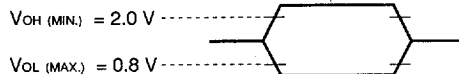
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

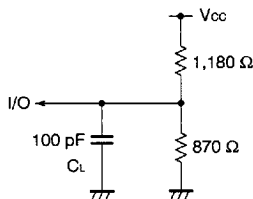
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	trAC = 60 ns		trAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		trc	104	—	124	—	ns	
RAS precharge time		trp	40	—	50	—	ns	
CAS precharge time		tcpn	10	—	10	—	ns	
RAS pulse width		trAS	60	10,000	70	10,000	ns	1
CAS pulse width		tcAS	10	10,000	12	10,000	ns	
RAS hold time		trSH	15	—	20	—	ns	
CAS hold time		tcSH	45	—	50	—	ns	
RAS to CAS delay time		trCD	14	45	14	52	ns	2
RAS to column address delay time		trAD	12	30	12	35	ns	2
CAS to RAS precharge time		tcrp	5	—	5	—	ns	3
Row address setup time		tASR	0	—	0	—	ns	
Row address hold time		trAH	10	—	10	—	ns	
Column address setup time		tASC	0	—	0	—	ns	
Column address hold time		tCAH	10	—	12	—	ns	
OE lead time referenced to RAS		toES	0	—	0	—	ns	
CAS to data setup time		tcLZ	0	—	0	—	ns	
OE to data setup time		toLZ	0	—	0	—	ns	
OE to data delay time		toED	13	—	15	—	ns	
Transition time (rise and fall)		tt	1	50	1	50	ns	
Refresh time	μPD42S17405L	tREF	—	128	—	128	ms	4
	μPD4217405L		—	32	—	32		

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- Notes** 1. In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $t_{\text{RAS}}(\text{MAX.})$ is 100 μs .
 If $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.
 2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

3. $t_{\text{CRP}}(\text{MIN.})$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
 4. This specification is applied only to the μ PD42S17405L.

Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	1
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	1
Access time from column address	t_{AA}	—	30	—	35	ns	1
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	t_{RAL}	30	—	35	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	t_{CHO}	5	—	5	—	ns	

- Notes** 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

2. Either $t_{\text{RCH}}(\text{MIN.})$ or $t_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
 3. $t_{\text{OEZ}}(\text{MAX.})$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t _{WCH}	10	—	10	—	ns	1
$\overline{WE}$ pulse width	t _{WP}	10	—	10	—	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t _{RWL}	15	—	20	—	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t _{CWL}	10	—	12	—	ns	
$\overline{WE}$ setup time	t _{WCS}	0	—	0	—	ns	2
$\overline{OE}$ hold time	t _{OEH}	0	—	0	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	3
Data-in hold time	t _{DH}	10	—	10	—	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t _{RWC}	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t _{RWD}	77	—	89	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t _{CWD}	32	—	37	—	ns	1
Column address to $\overline{WE}$ delay time	t _{AWD}	47	—	54	—	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t _{HPC}	25	—	30	—	ns	1
RAS pulse width	t _{RASP}	60	125,000	70	125,000	ns	
CAS pulse width	t _{HCAS}	10	10,000	12	10,000	ns	
CAS precharge time	t _{CP}	10	—	10	—	ns	
Access time from CAS precharge	t _{ACP}	—	35	—	40	ns	
CAS precharge to WE delay time	t _{CPWD}	52	—	59	—	ns	2
RAS hold time from CAS precharge	t _{RHCP}	35	—	40	—	ns	
Read modify write cycle time	t _{HPRWC}	66	—	75	—	ns	
Data output hold time	t _{DHC}	5	—	5	—	ns	
OE to CAS hold time	t _{OCH}	5	—	5	—	ns	4
OE precharge time	t _{OEP}	5	—	5	—	ns	
Output buffer turn-off delay from WE	t _{WEZ}	0	13	0	15	ns	3,4
WE pulse width	t _{WPZ}	10	—	10	—	ns	4
Output buffer turn-off delay from RAS	t _{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from CAS	t _{OFC}	0	13	0	15	ns	3,4

Notes 1. t_{HPC} (MIN.) is applied to CAS access.

2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CPWD} ≥ t_{CPWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
3. t_{OFC} (MAX.), t_{OFR} (MAX.) and t_{WEZ} (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.
4. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.
 - (1) Both RAS and CAS are inactive (at the end of the read cycle)
 WE: inactive, OE: active
 t_{OFC} is effective when RAS is inactivated before CAS is inactivated.
 t_{OFR} is effective when CAS is inactivated before RAS is inactivated.
 - (2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)
 WE, OE: inactive t_{OEZ} is effective.
 - (3) Both RAS and CAS are inactive or RAS is active and CAS is inactive (at the end of read cycle)
 WE, OE: active and either t_{RAH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.
 - (4) WE: inactive (in read cycle)
 CAS: inactive, OE: active t_{CHO} is effective.
 CAS, OE: active t_{OCH} is effective.

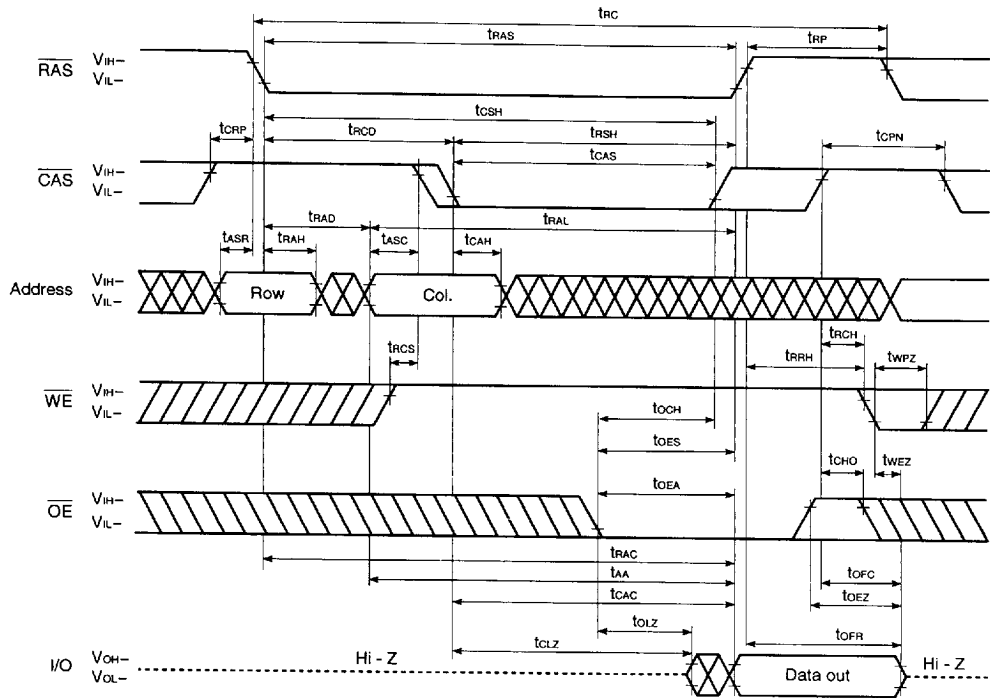
Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t _{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t _{CHR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RASS}	100	—	100	—	μs	1
$\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RPS}	110	—	130	—	ns	1
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{CHS}	—50	—	—50	—	ns	1
$\overline{\text{WE}}$ setup time	t _{WSR}	10	—	10	—	ns	
$\overline{\text{WE}}$ hold time	t _{WHR}	15	—	15	—	ns	

Note 1. This specification is applied only to the μPD42S17405L.

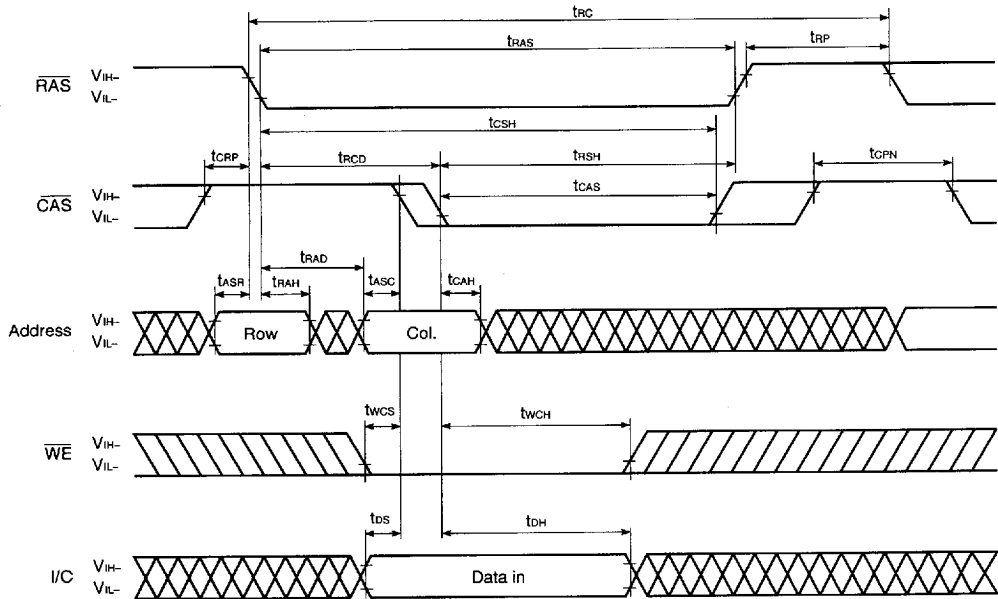
6427525 0091132 81T

Read Cycle



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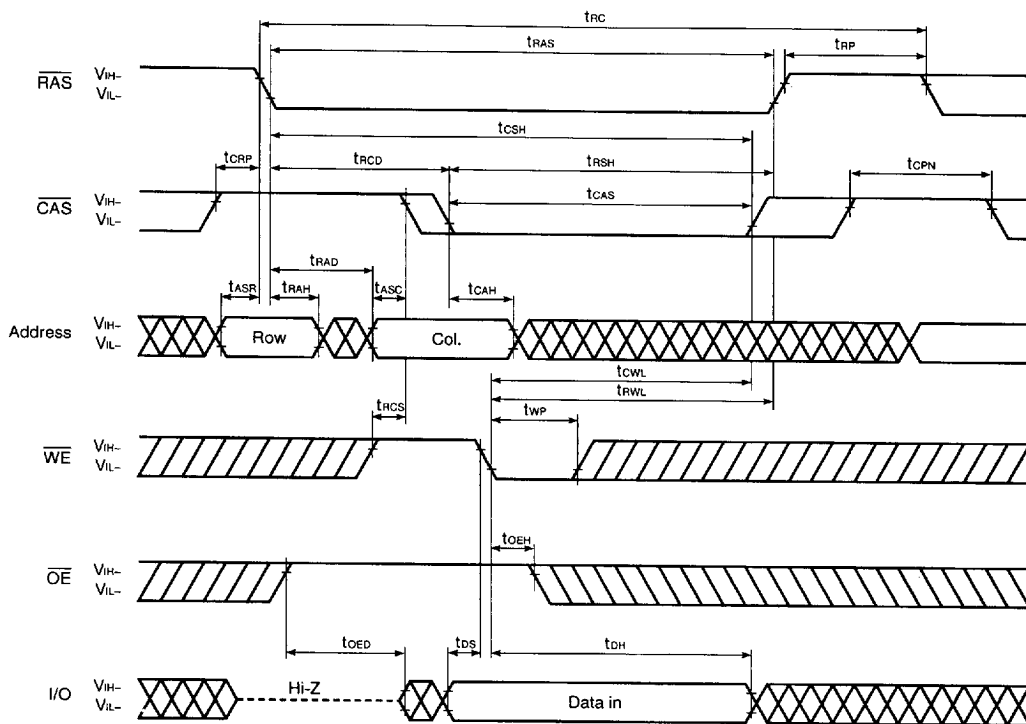
Early Write Cycle



Remark $\overline{OE}$: Don't care

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Late Write Cycle

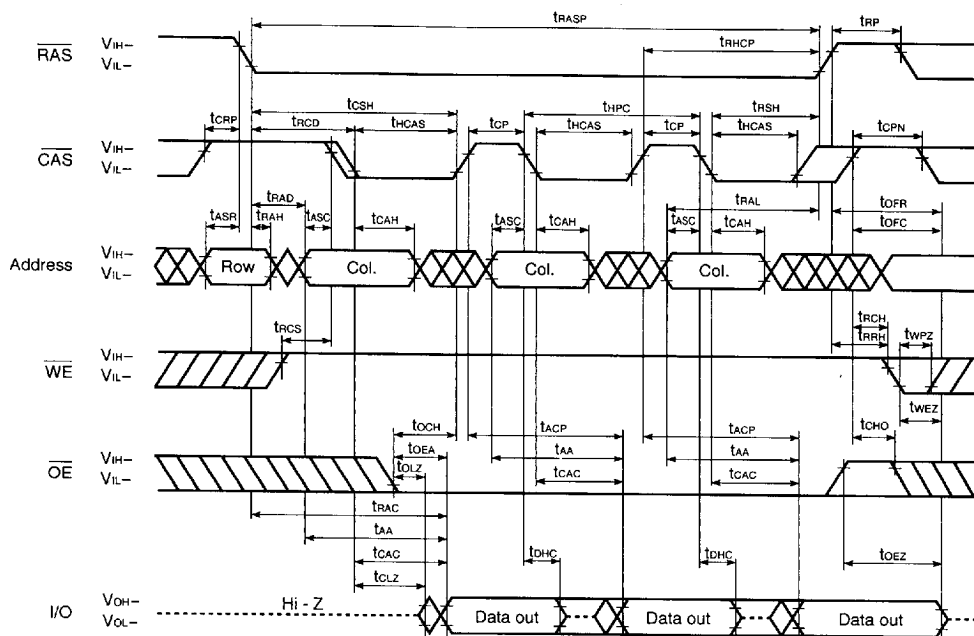


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The timing diagram illustrates the sequence of signals for the 64K1602 LCD module. The signals and their timing parameters are as follows:

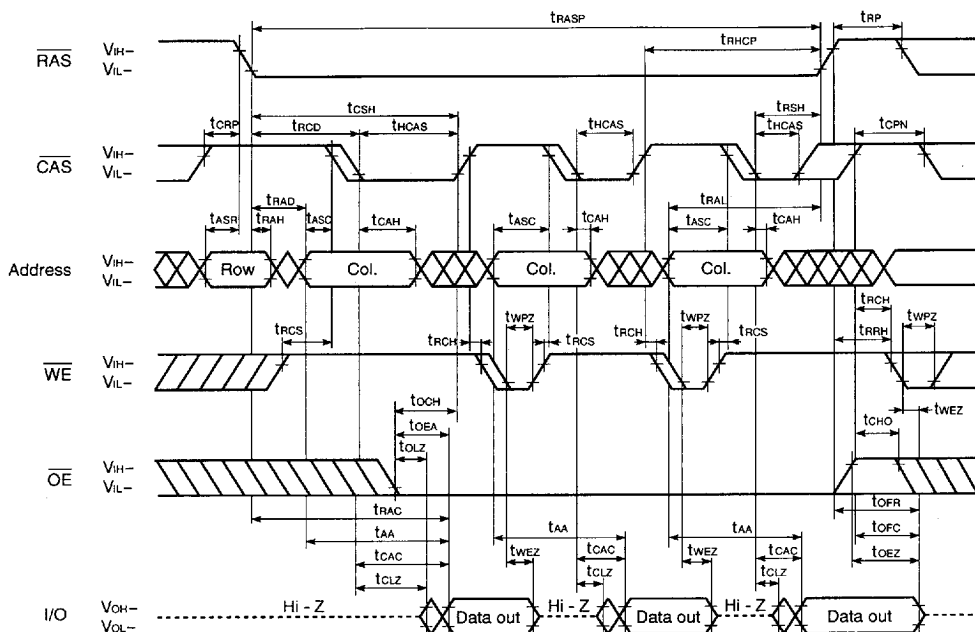
- RAS**: $\overline{\text{RAS}}$ signal with timing parameters t_{RAS} , t_{RWC} , and t_{RP} .
- CAS**: $\overline{\text{CAS}}$ signal with timing parameters t_{CSh} , t_{RCD} , t_{RSH} , t_{CAS} , and t_{CPN} .
- Address**: V_{IH} and V_{IL} signals for Row and Col. with timing parameters t_{RAD} , t_{ASR} , t_{RAH} , t_{ASC} , and t_{CAH} .
- WE**: $\overline{\text{WE}}$ signal with timing parameters t_{RWD} , t_{AWD} , t_{CWD} , t_{CWL} , t_{RWL} , and t_{WP} .
- OE**: $\overline{\text{OE}}$ signal with timing parameters t_{RCS} , t_{OEA} , t_{OEh} , t_{OEL} , t_{AA} , and t_{CAC} .
- I/O**: V_{IH} and V_{IL} signals for Data in and Data out. Data in has timing parameters t_{OED} , t_{DS} , and t_{DH} . Data out has timing parameters t_{OLZ} , t_{CLZ} , and t_{OEZ} .
- Hi-Z**: High-impedance state for Data in and Data out.

Hyper Page Mode (EDO) Read Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{\text{WE}}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

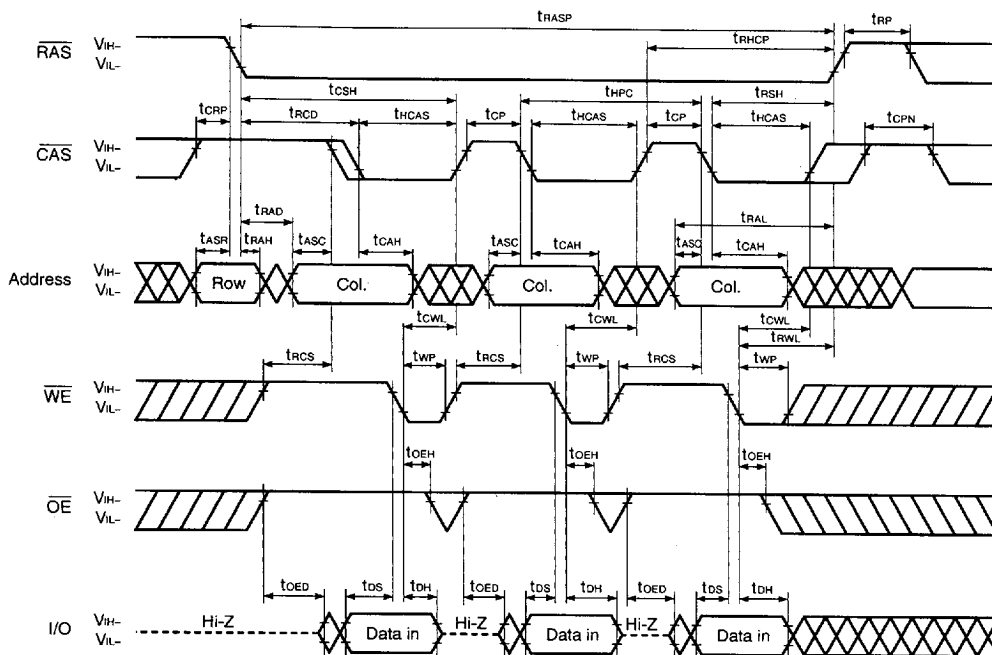
[illegible]

Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

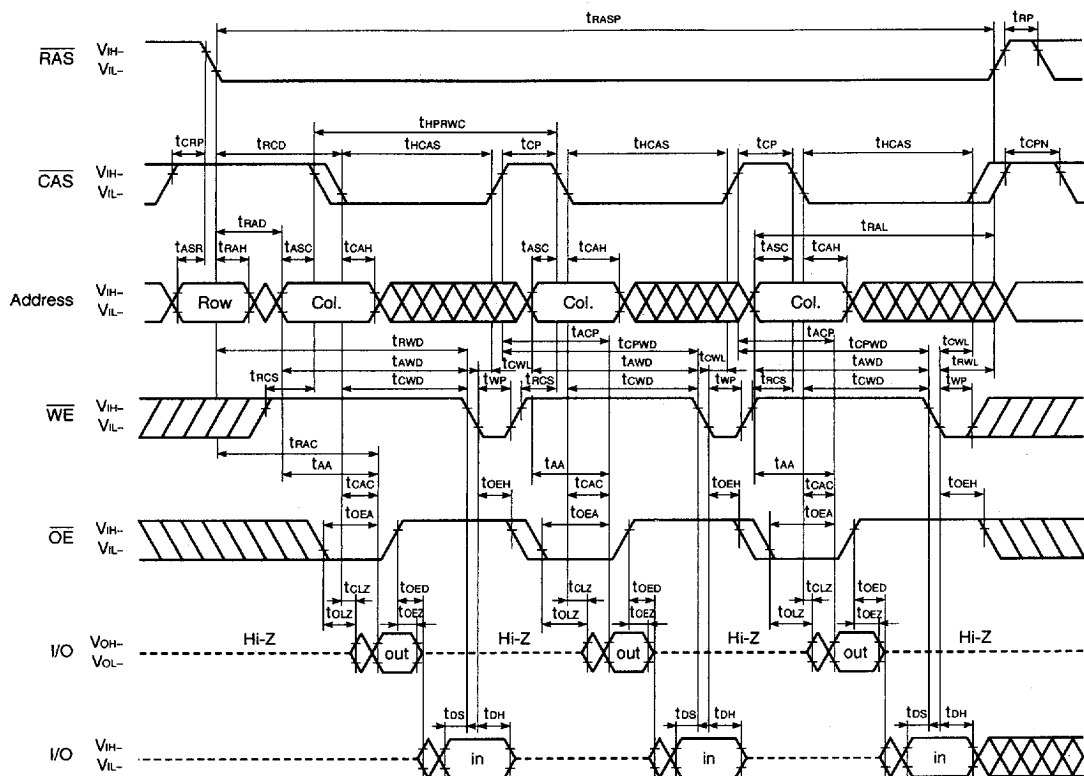
[illegible]

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle

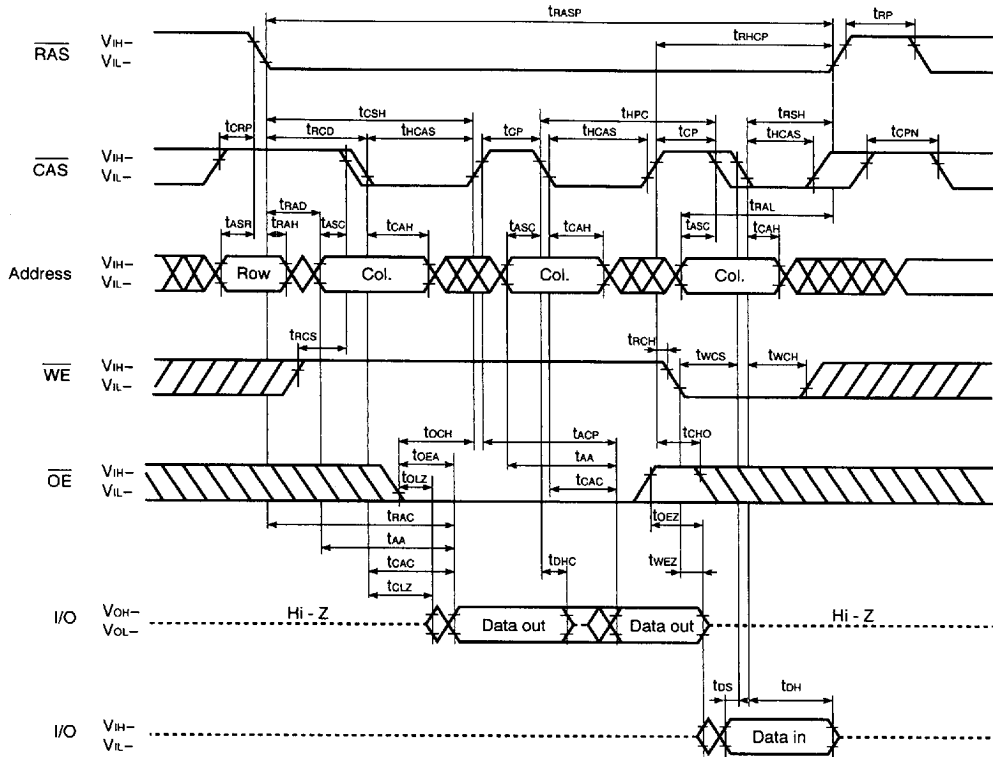


Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.



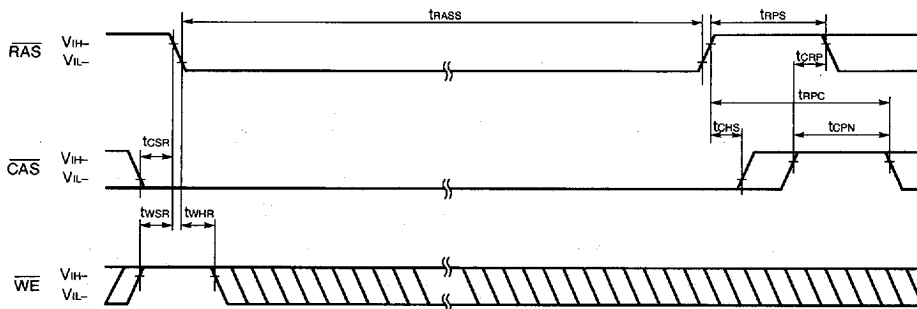
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S17405L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

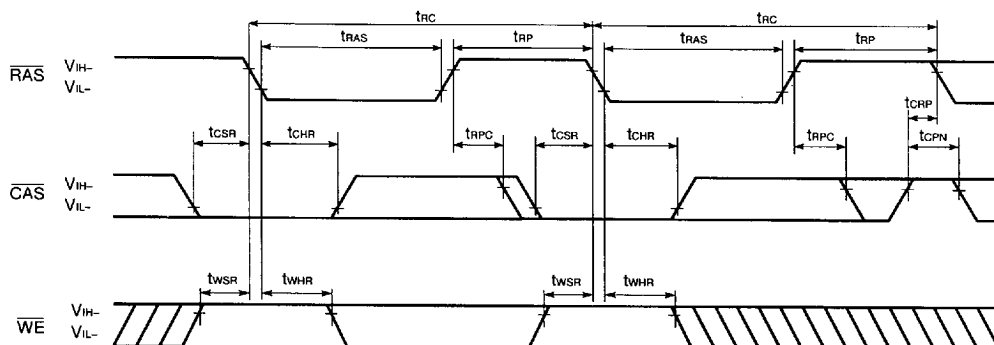
When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 2,048 times within a 32 ms interval just before and after setting CAS before RAS self refresh.

(3) If t_{TRAS} (MIN.) is not satisfied at the beginning of CAS before RAS self refresh cycles (t_{TRAS} < 100 μs), CAS before RAS refresh cycles will be executed one time.

If 10 μs < t_{TRAS} < 100 μs, RAS precharge time for CAS before RAS self refresh (t_{TRPS}) is applied. And refresh cycles (2,048/128 ms) should be met.

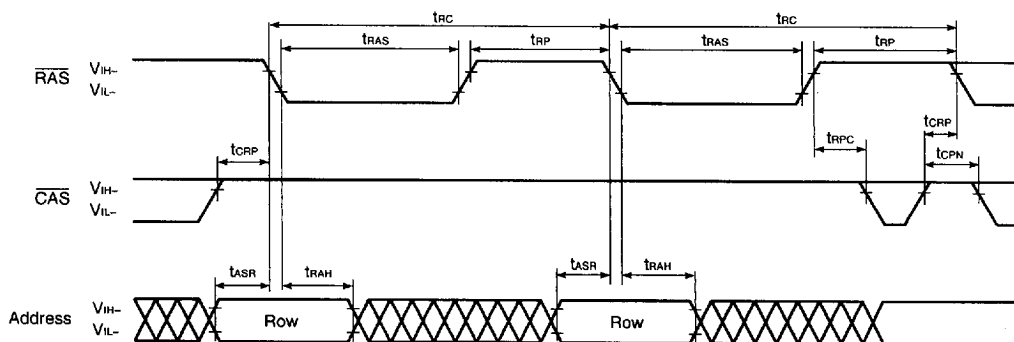
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



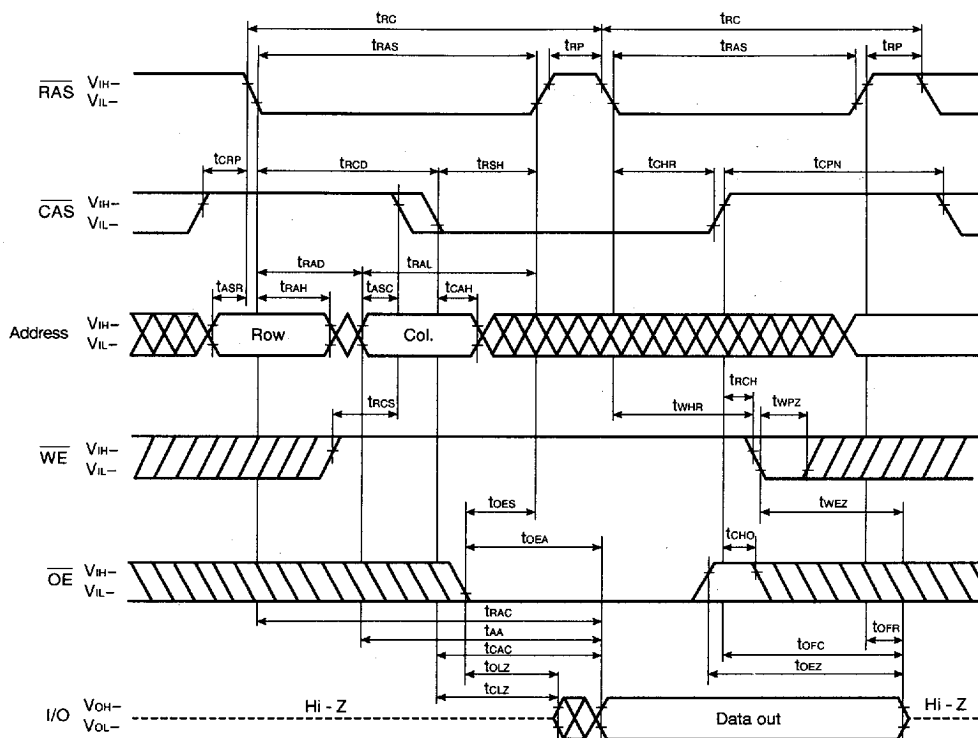
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

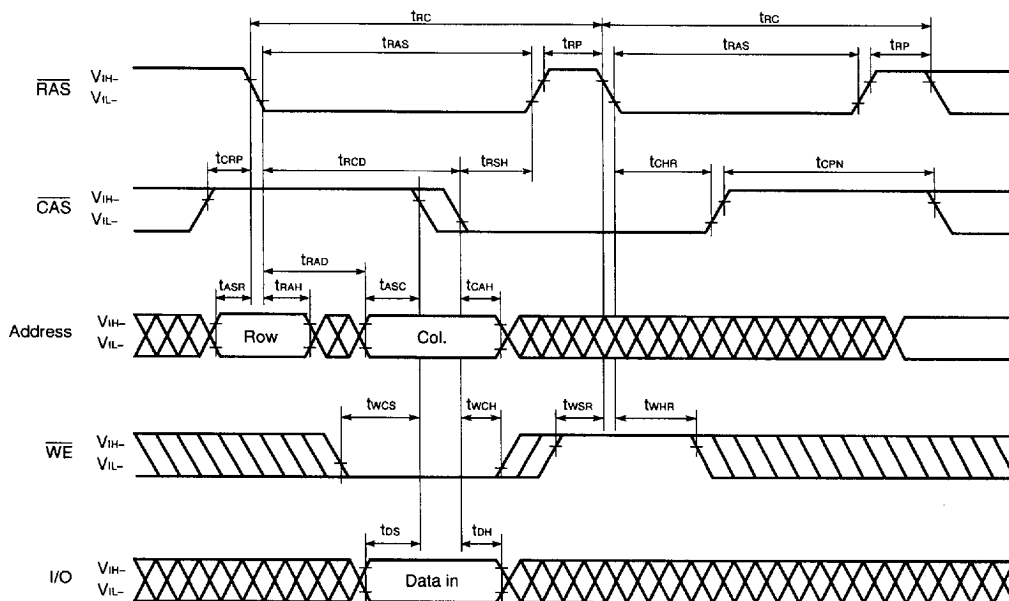


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

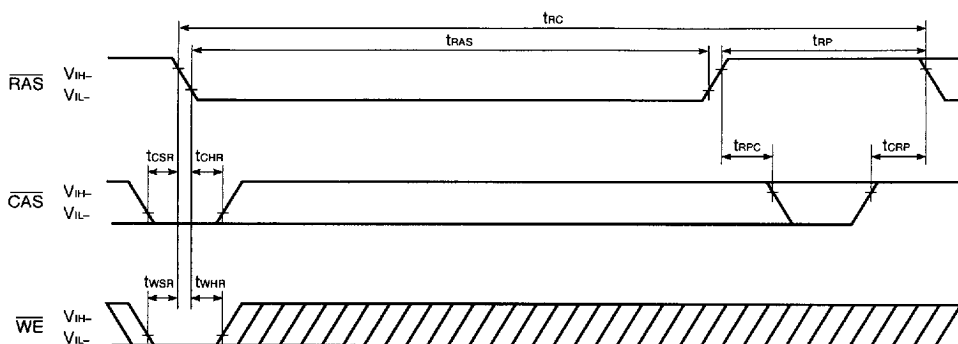


Hidden Refresh Cycle (Write)



Remark $\overline{\text{OE}}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

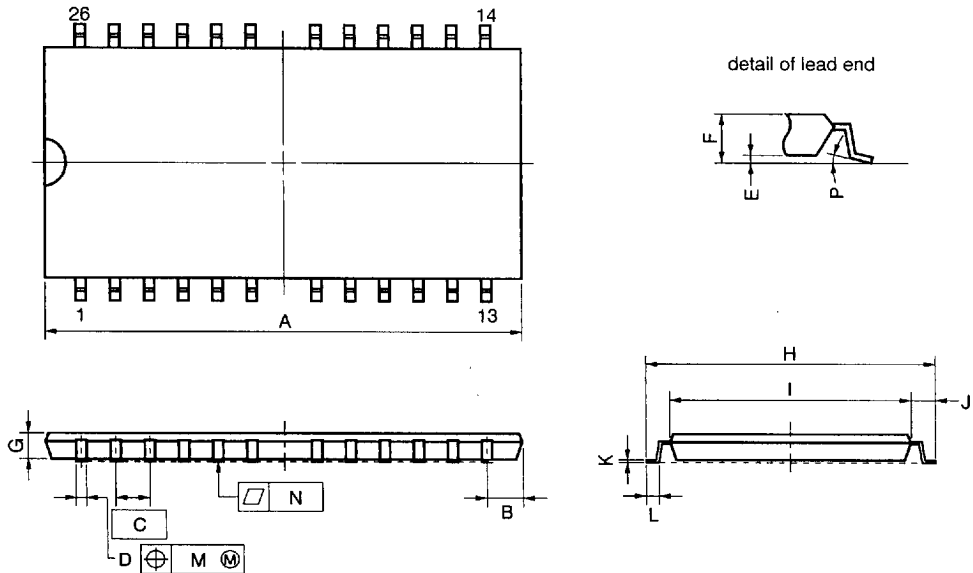
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



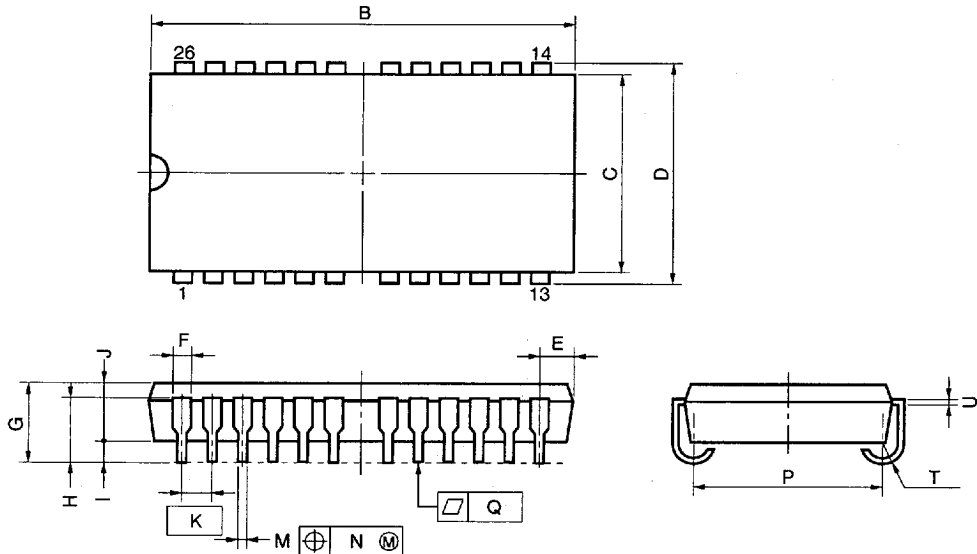
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 ^{+0.09} _{-0.07}	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004
P	3 ⁺⁷ ₋₃	3 ⁺⁷ ₋₃

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	17.3 ^{+0.20} _{-0.25}	0.681 ^{+0.008} _{-0.010}
C	7.62	0.300
D	8.47±0.2	0.333 ^{+0.009} _{-0.008}
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17405L, 4217405L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17405LG3, 4217405LG3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

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μPD42S17405LLA, 4217405LLA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".