UHF power transistor BLT52

FEATURES

- Emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Common emitter class-B operation in portable radio transmitters in the 470 MHz communication band.

DESCRIPTION

NPN silicon planar epitaxial power transistor encapsulated in a ceramic SOT409A SMD package.

PINNING

PIN	DESCRIPTION
1, 4, 5, 8	emitter
2, 3	base
6, 7	collector

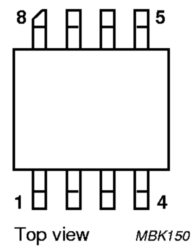


Fig.1 Simplified outline SOT409A.

QUICK REFERENCE DATA

RF performance at $T_{mb} \leq 60$ °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-B	470	7.5	7	≥8 typ. 9.5	≥50 typ. 65
		6	3	≥8 typ. 9.5	≥50 typ. 55

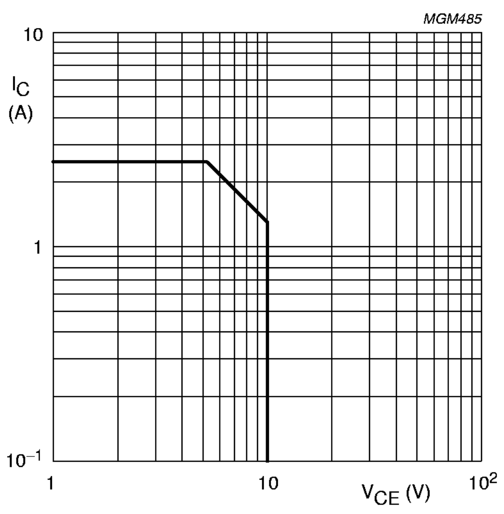
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	10	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	2.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 60$ °C	–	13	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 13 W; $T_{mb} \leq 60$ °C	8	K/W



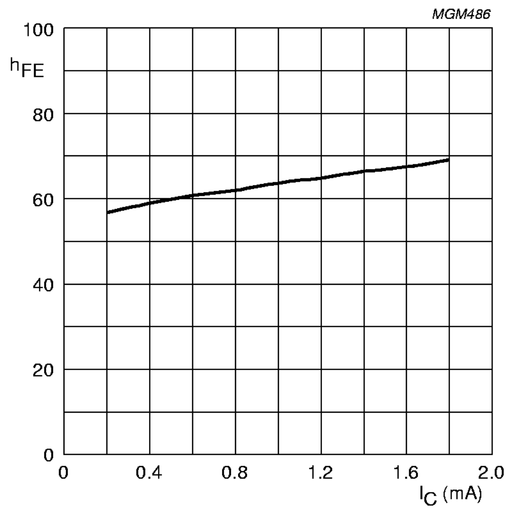
T_{mb} = 60 °C.

Fig.2 DC SOAR.

CHARACTERISTICS

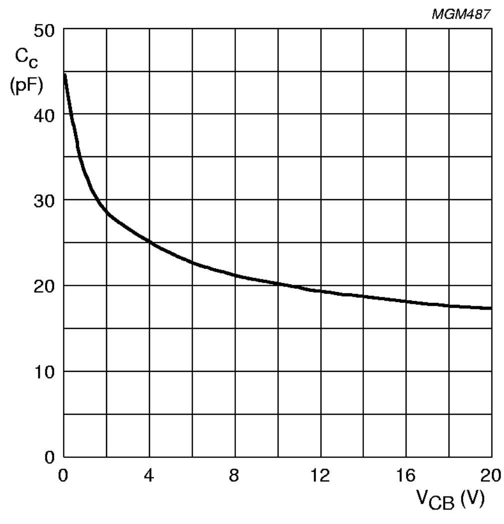
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 20 mA	20	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 40 mA	10	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 4 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 7.5 V	–	–	1	mA
h_{FE}	DC current gain	I_C = 1.2 A; V_{CE} = 5 V	25	–	–	
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = 7.5 V; f = 1 MHz	–	24	–	pF
C_{re}	feedback capacitance	I_C = 0; V_{CE} = 7.5 V; f = 1 MHz	–	17	–	pF



V_{CE} = 5 V; T_j = 25 °C.
Measured under pulse conditions: $t_p \leq 300$ µs; $\delta \leq 0.001$.

Fig.3 DC current gain as a function of collector current; typical values.



$I_E = i_e$ = 0; f = 1 MHz; T_j = 25 °C.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at $T_{mb} \leq 60$ °C in a common emitter test circuit.

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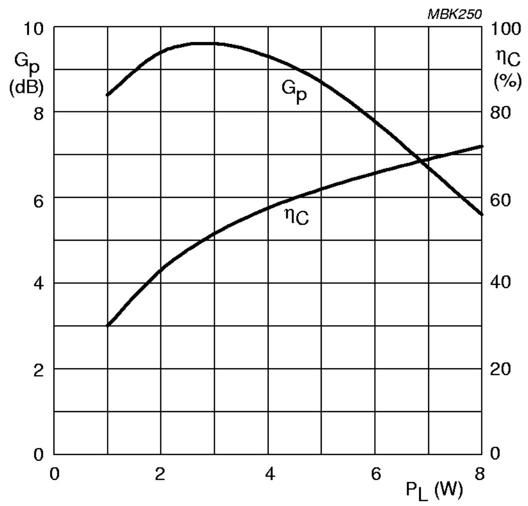
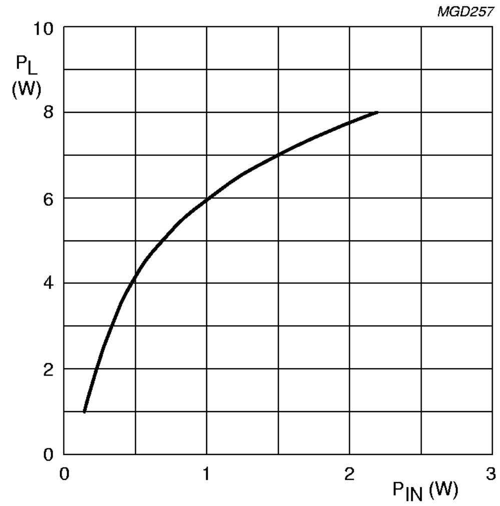
Ruggedness in class-B operation

The BLT52 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: CW, class-B operation; f = 470 MHz; V_{CE} = 9 V and P_L = 7 W; $T_{mb} \leq 60$ °C.



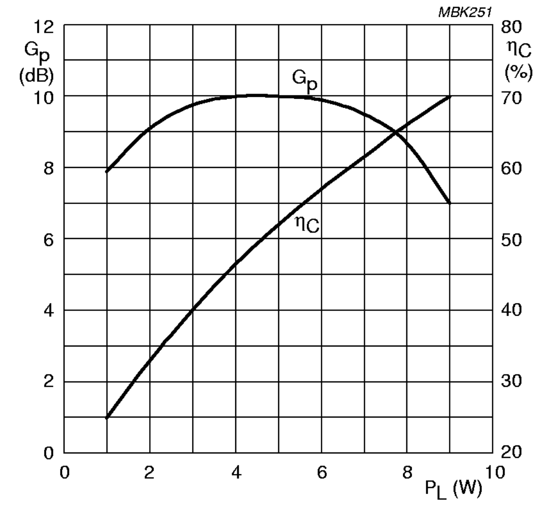
CW, class-B operation; f = 470 MHz; V_{CE} = 6 V; tuned at P_L = 3 W; $T_{mb} \leq 60$ °C.

Fig.5 Power gain and collector efficiency as functions of load power; typical values.



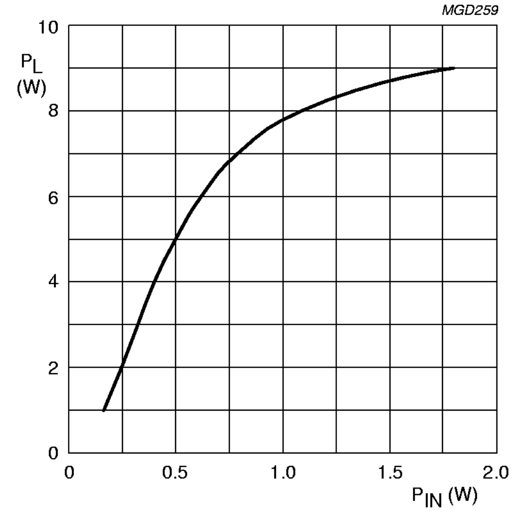
CW, class-B operation; f = 470 MHz; V_{CE} = 6 V; tuned at P_L = 3 W; $T_{mb} \leq 60$ °C.

Fig.6 Load power as a function of input power; typical values.



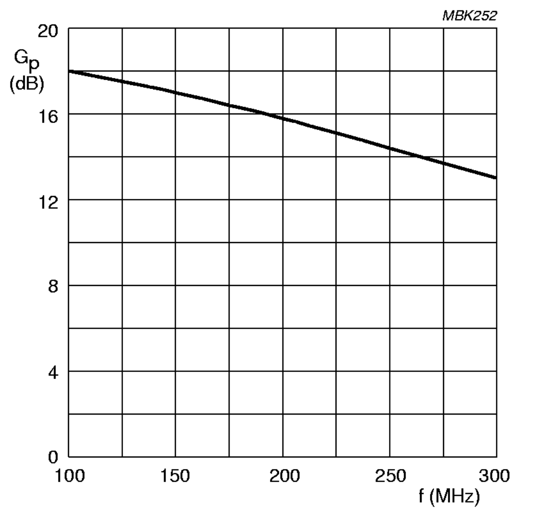
CW, class-B operation; f = 470 MHz; V_{CE} = 7.5 V; tuned at P_L = 7 W; $T_{mb} \leq$ 60 °C.

Fig.7 Power gain and collector efficiency as functions of load power; typical values.



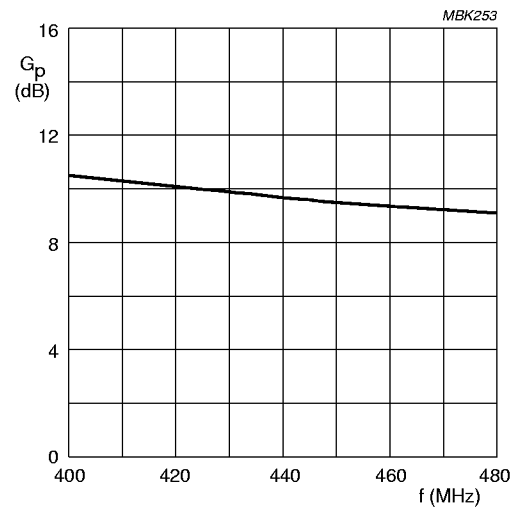
CW, class-B operation; f = 470 MHz; V_{CE} = 7.5 V; tuned at P_L = 7 W; $T_{mb} \leq$ 60 °C.

Fig.8 Load power as a function of input power; typical values.



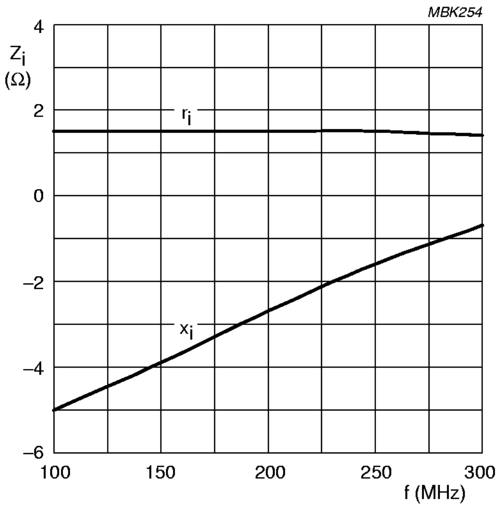
CW, class-B operation; V_{CE} = 7.5 V; P_L = 7 W; $T_{mb} \leq$ 60 °C.

Fig.9 Power gain as a function of frequency; typical values.



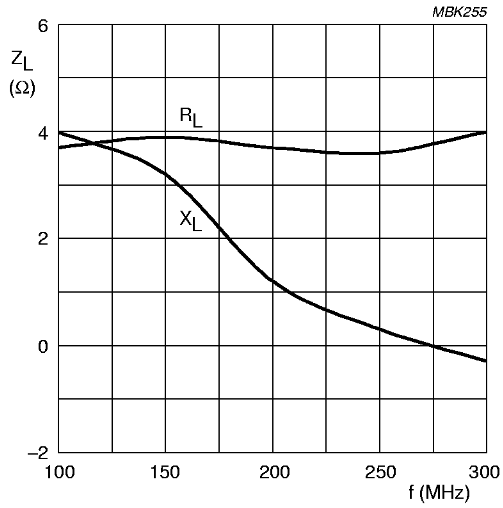
CW, class-B operation; V_{CE} = 7.5 V; P_L = 7 W; $T_{mb} \leq$ 60 °C.

Fig.10 Power gain as a function of frequency; typical values.



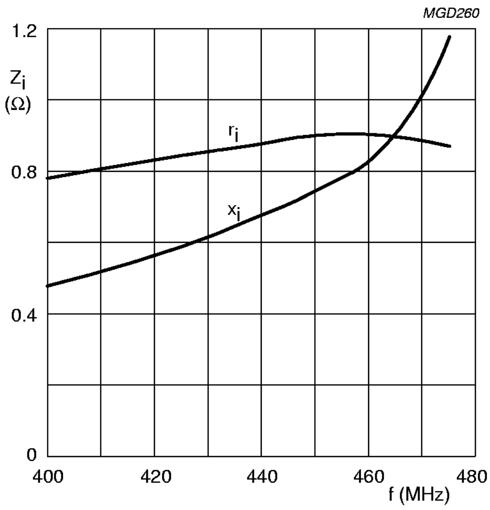
CW, class-B operation; V_{CE} = 7.5 V; P_L = 7 W; T_{mb} ≤ 60 °C.

Fig.11 Input impedance as a function of frequency (series components); typical values.



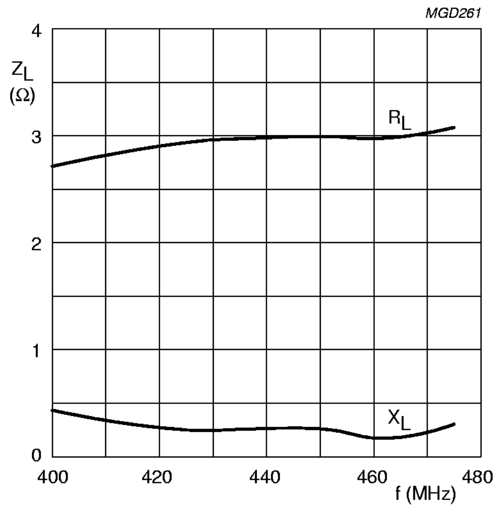
CW, class-B operation; V_{CE} = 7.5 V; P_L = 7 W; T_{mb} ≤ 60 °C.

Fig.12 Load impedance as a function of frequency (series components); typical values.



CW, class-B operation; V_{CE} = 7.5 V; P_L = 7 W; T_{mb} ≤ 60 °C.

Fig.13 Input impedance as a function of frequency (series components); typical values.

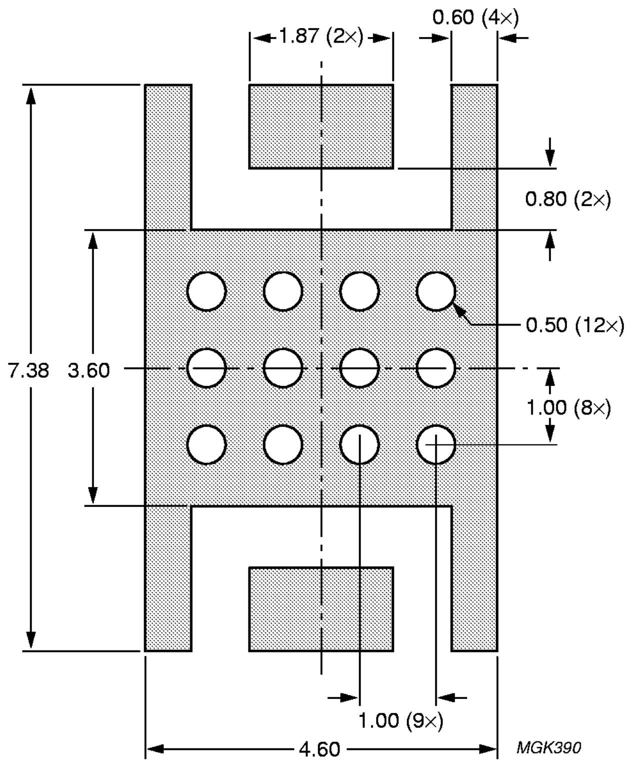


CW, class-B operation; V_{CE} = 7.5 V; P_L = 7 W; T_{mb} ≤ 60 °C.

Fig.14 Load impedance as a function of frequency (series components); typical values.

MOUNTING RECOMMENDATIONS

Both the metallized groundplate and leads contribute to the heatflow. It is recommended that the transistor is mounted on a grounded metallized area of a maximum thickness of 0.8 mm on the printed-circuit board, equipped with at least 12 (0.5 mm diameter) through metallized holes filled with solder.
A thermal resistance $R_{th(mb-h)}$ of 5 K/W can be achieved if heatsink compound is applied when the transistor is mounted on the printed-circuit board.

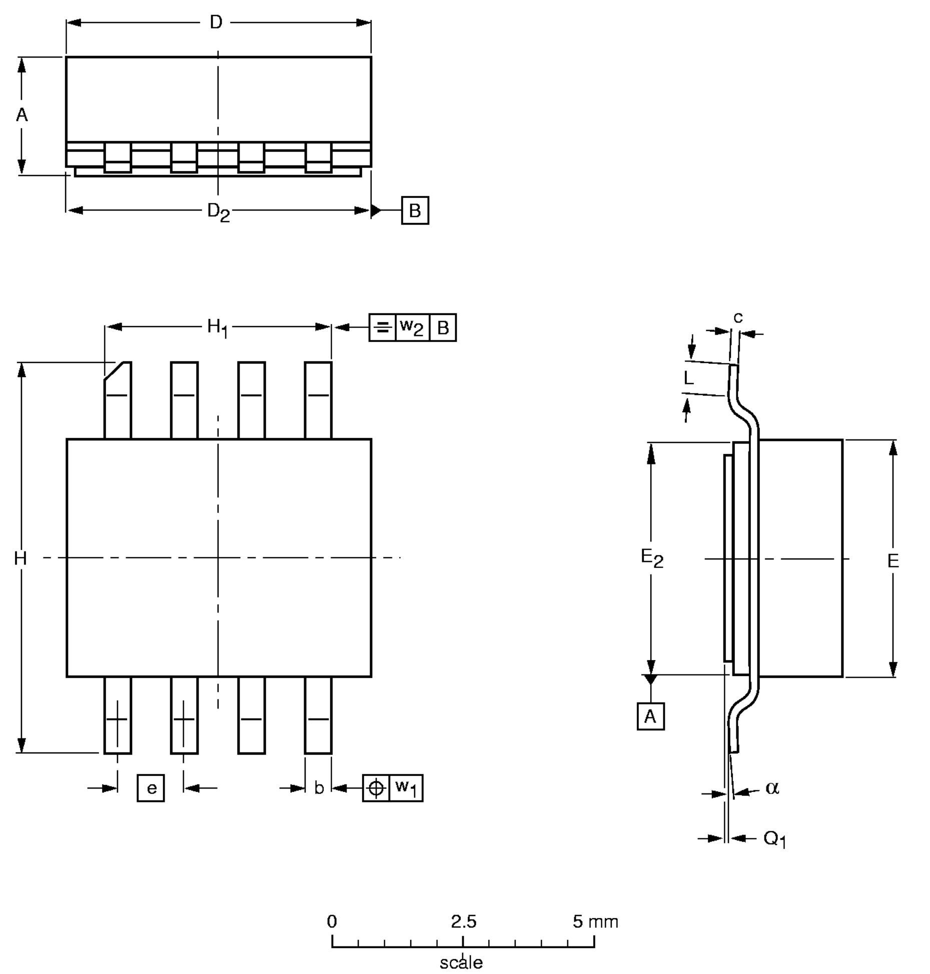


Dimensions in mm.

Fig.15 Reflow soldering footprint for SOT409A.

PACKAGE OUTLINE

Ceramic surface mounted package; 8 leads **SOT409A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						97-06-28