



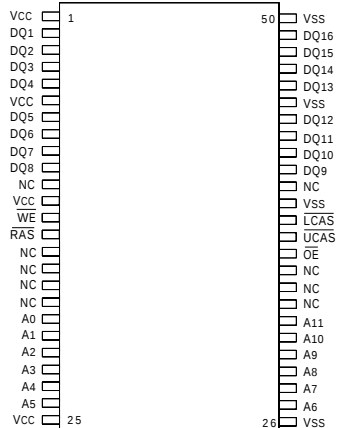
4Mx16 EDO (Extended Data Out) Dynamic RAM 3.3V

FEATURES

- Access Time: 50, 60 and 70ns
- 4 Meg x 16 bit CMOS Dynamic RAM
- Package:
 - 50 pin Plastic TSOP
- Extended Data Out Mode Operation
- Single +3.3V ($\pm 0.3V$) Supply Operation
- 4096 Cycles Refresh
- $\overline{RAS}$ - Only, $\overline{CAS}$ -before- $\overline{RAS}$, and HIDDEN refresh capability
- Low Operating Power Dissipation
- Low Standby Power
- Common I/O
- All Inputs/Outputs TTL Compatible
- Industrial ($-40^{\circ}C$ to $+85^{\circ}C$) and Military ($-55^{\circ}C$ to $+125^{\circ}C$) Temperature Ranges

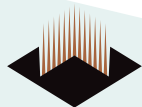
PIN CONFIGURATION

TOP VIEW

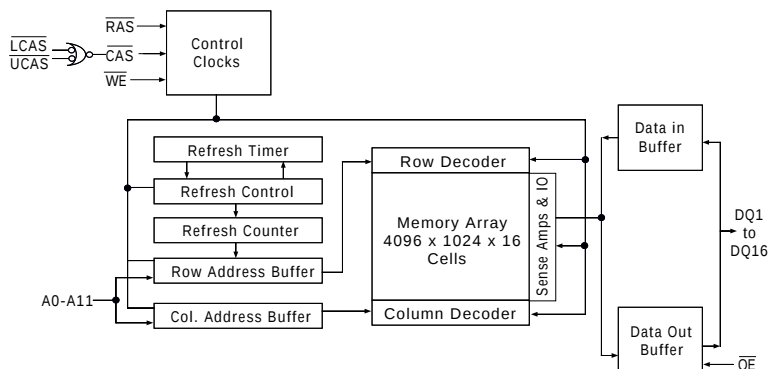


PIN DESCRIPTION

A0-11	Address Inputs
$\overline{LCAS}$ / $\overline{UCAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable
DQ1-16	Data Inputs/Outputs
VCC	Power (+3.3V $\pm 0.3V$)
VSS	Ground
NC	No Connection



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature (Industrial)	-40°C to +85°C
Operating Temperature (Military)	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Power Dissipation	1 Watt
Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS⁽¹⁾

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2	--	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	--	0.8	V

NOTES:

1. All voltage values are with respect to V_{SS}.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Current	I _{cc1}	RAS and UCAS, LCAS, Address cycling @ Trc = min.			180	mA
Standby Current	I _{cc2}	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = \overline{\text{WE}} = V_{\text{IH}}$			4	mA
RAS-only-Refresh Current	I _{cc3}	$\overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{\text{IH}}$, RAS, Addressing cycling @ Trc = min			180	mA
EDO Mode Current	I _{cc4}	$\overline{\text{RAS}} = V_{\text{IL}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ Addressing cycling @ Trc = min.			165	mA
Standby Current	I _{cc5}	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = \overline{\text{WE}} = V_{\text{CC}} - 0.2\text{V}$			2	mA
CAS-before-RAS Refresh Current	I _{cc6}	$\overline{\text{RAS}}$ and $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ cycling @ Trc=min.			180	mA
Input Leakage Current	I _{IL}	$0\text{V} \leq V_{\text{IN}} \leq V_{\text{CC}} + 0.3\text{V}$ All Other Input Pins = 0V	-5		5	μA
Output Leakage Current	I _{OL}	$0\text{V} \leq V_{\text{OUT}} \leq V_{\text{CC}}$	-5		5	μA
Output High Voltage	V _{OH}	I _{OH} = -2.0mA	2.4	—	—	V
Output Low Voltage	V _{OL}	I _{OL} = 2.0mA	—	—	0.4	V

NOTES:

3. I_{cc1(av)}, I_{cc3(av)}, I_{cc4(av)}, and I_{cc6} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4. I_{cc1(av)} and I_{cc4(av)} are dependent on output loading. Specified values are obtained with the output open.

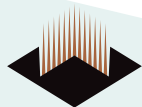
CAPACITANCE

(f = 1.0MHz, T_A = 25°C, V_{CC} = 3.3V)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C _{IN1}	5	pF
Input Capacitance (CAS, WE, RAS)	C _{IN2}	7	pF
Output Capacitance (Q)	C _{DQ}	7	pF

TRUTH TABLE

RAS	LCAS	UCAS	WE	OE	DQ1-8	DQ9-16	STATE
H	X	X	X	X	High Z	High Z	Standby
L	H	H	X	X	High Z	High Z	Refresh
L	L	H	H	L	DQ Out	High Z	Byte Read
L	H	L	H	L	High Z	DQ Out	Byte Read
L	L	L	H	L	DQ Out	DQ Out	Word Read
L	L	H	L	H	DQ In	—	Byte Write
L	H	L	L	H	—	DQ In	Byte Write
L	L	L	L	H	DQ In	DQ In	Word Write
L	L	L	H	H	High Z	High Z	—



TIMING REQUIREMENTS — READ, WRITE, READ-MODIFY-WRITE, REFRESH, AND PAGE MODE CYCLES (V_{CC}=3.3V±0.3V) Notes 1, 2, 5

Parameter	Symbol	50ns		60ns		70ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	90		110		130		ns	
Read-Modify-Write Cycle Time	t _{RWC}	126		150		180		ns	
Access Time from $\overline{\text{CAS}}$	t _{CAC}		13		15		20	ns	3,4,5
Access Time from RAS	t _{RAC}		50		60		70	ns	3,4,10
Access Time From Column Address	t _{AA}		25		30		35	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		0		0		ns	6
Output buffer turn-off delay	t _{OFF}	0	13	0	15	0	20	ns	6,14
Transition Time	t _T	2	50	2	50	2	50	ns	2
RAS Precharge Time	t _{RP}	30		40		50		ns	
$\overline{\text{RAS}}$ Low Pulse Width	t _{TRAS}	50	10,000	60	10,000	70	10,000	ns	
RAS Hold Time after CAS Low	t _{TRSH}	13		15		20		ns	
CAS Hold Time after RAS Low	t _{CSH}	38		45		50		ns	
CAS Low Pulse Width	t _{CAS}	8	10,000	10	10,000	15	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	20	50	ns	4
Column Address Delay from $\overline{\text{RAS}}$ Low	t _{RAD}	9	25	12	30	15	35	ns	10
Delay $\overline{\text{CAS}}$ High to RAS Low	t _{CRP}	5		5		5		ns	
Row Address Set Up Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	9		10		10		ns	
Column Address Set Up Time	t _{ASC}	0		0		0		ns	
Column Address Hold Time	t _{CAH}	8		10		15		ns	
Column Address Hold Time Referenced RAS	t _{AR}	40		45		55		ns	
Column Address to RAS Setup	t _{RAL}	25		30		35		ns	
Read Set Up Time before CAS Low	t _{RCS}	0		0		0		ns	
Read Hold Time after $\overline{\text{CAS}}$ High	t _{RCH}	0		0		0		ns	8
Read Hold Time after RAS High	t _{RRH}	0		0		0		ns	8
Write Hold Time after CAS Low	t _{WCH}	8		10		15		ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{WCR}	40		45		55		ns	
Write Pulse Width	t _{WP}	7		10		15		ns	
$\overline{\text{RAS}}$ Hold Time after Write Low	t _{RWL}	13		15		20		ns	
CAS Hold Time after Write Low	t _{CWL}	8		10		15		ns	
Data Set up Time	t _{DS}	0		0		0		ns	9
Data Hold Time after $\overline{\text{CAS}}$ Low	t _{DH}	8		10		15		ns	9
Data Hold Time Referenced to $\overline{\text{RAS}}$	t _{DHR}	40		45		55		ns	
Refresh Cycle (Industrial)	t _{REF}		32		32		32	ms	
Refresh Cycle (Military)	t _{REF}		16		16		16	ms	
Write Setup Time before $\overline{\text{CAS}}$ Low	t _{WCS}	0		0		0		ns	7
$\overline{\text{CAS}}$ Low to $\overline{\text{WE}}$ Low Delay	t _{CWD}	30		35		45		ns	7
$\overline{\text{RAS}}$ Low to $\overline{\text{WE}}$ Low Delay	t _{RWD}	67		79		94		ns	7
Column Address Setup to CAS High	t _{ACH}	15		15		15		ns	
OE Low to Output Valid	t _{OE}		13		15		20	ns	13
CAS Low to DOUT	t _{COH}	3		3		3		ns	
$\overline{\text{RAS}}$ Low to $\overline{\text{WE}}$ Low	t _{WRH}	10		10		10		ns	
Write High to $\overline{\text{RAS}}$ Low	t _{WRP}	10		10		10		ns	
Address to $\overline{\text{WE}}$ Low Delay	t _{AWD}	48		55		65		ns	7

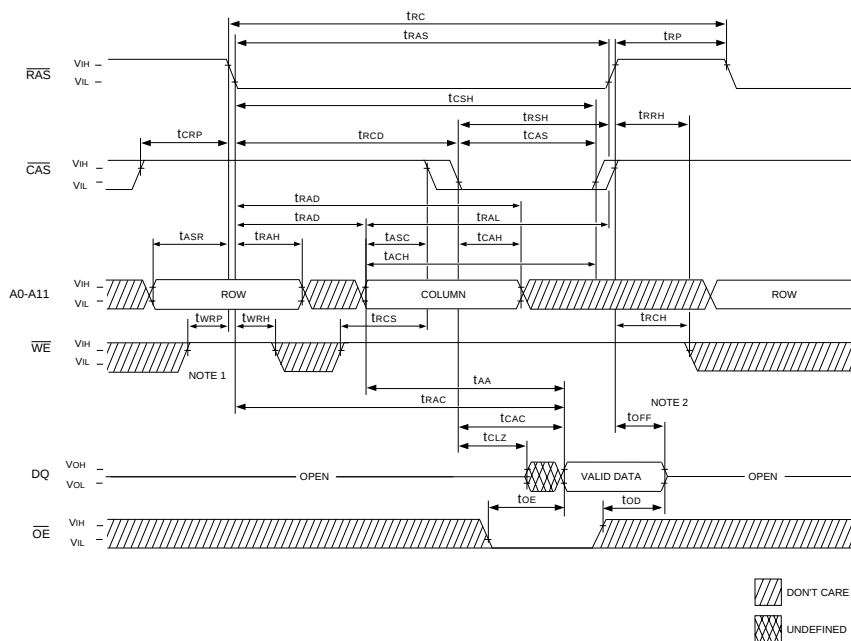


WRITE CYCLE, EARLY AND DELAYED WRITE (VCC=3.3V±0.3V) Notes 1, 2, 5

Parameter	Symbol	50ns		60ns		70ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS Setup for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	tCSR	5		5		5		ns	
CAS Hold for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	tCHR	10		10		15		ns	
Precharge to CAS Active	trPC	5		5		5		ns	
Access Time from CAS Precharge	tCPA		28		35		40	ns	3
EDO Page Cycle Time	tPC	20		25		30		ns	
EDO Page Read-Modify-Write Cycle Time	tPRWC	47		56		71		ns	
CAS precharge time (EDO cycle)	tCP	8		10		10		ns	
RAS pulse width (EDO Cycle)	trASP	50	125K	60	125K	70	125K	ns	
Output Disable Time after $\overline{\text{OE}}$ High	tOD	0	13	0	15	0	20	ns	6
Write Low to Next $\overline{\text{OE}}$ Low	tOEH	8		10		12		ns	
$\overline{\text{OE}}$ Low to $\overline{\text{CAS}}$ High Setup Time	tOES	4		5		5		ns	
$\overline{\text{OE}}$ High Hold From $\overline{\text{CAS}}$ High	tOEHC	5		10		10		ns	
$\overline{\text{OE}}$ High Pulse Width	tOEP	7		10		10		ns	
$\overline{\text{OE}}$ Setup prior to $\overline{\text{RAS}}$ during Hidden Refresh Cycle	tORD	0		0		0		ns	
$\overline{\text{OE}}$ delay from $\overline{\text{WE}}$	tWHZ	0	10	0	13	0	15	ns	
$\overline{\text{WE}}$ pulse to disable at $\overline{\text{CAS}}$ high	tWPZ	10		10		10		ns	

NOTES:

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved, and must be repeated whenever tREF is exceeded.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max) and are assumed to be 3ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the trCD (max) limit insures that trAC (max) can be met. trCD (max) is specified as a reference point only. If trCD is greater than the specified trCD (max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that trCD $\geq$ trCD (max)
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. twCS, trWD, tcWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twCS $\geq$ twCS (min), the cycle is an early write and the data output will remain high impedance for the duration of the cycle. If tcWD $\geq$ tcWD (min), trWD > trWD (min) and tAWD > tAWD (min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either trCH or trRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{WE}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the trAD (max) limit insures that trAC (max) can be met. trAD (max) is specified as a reference point only. If trAD is greater than the specified trAD (max) limit, then access time is controlled by tAA.



NOTES:

1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{WE}$ high for t_{WRP} and t_{WRH} .
2. t_{OFF} is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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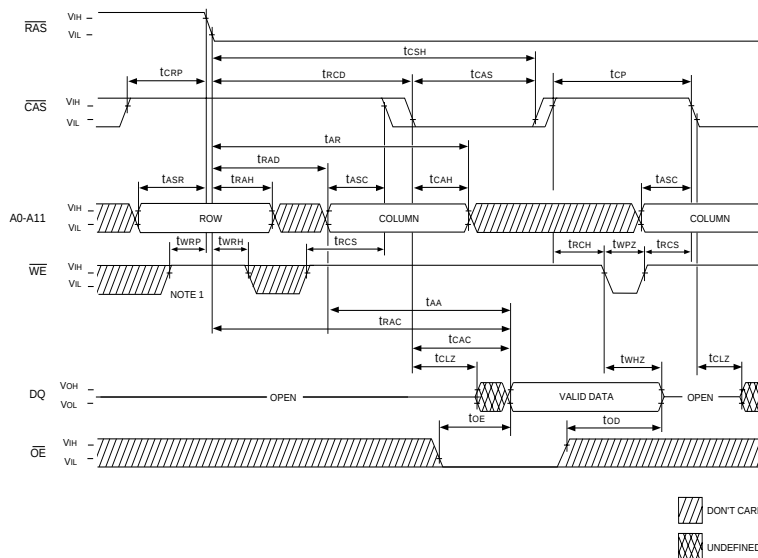


NOTE: 1. TPC is for Late Write Cycles Only

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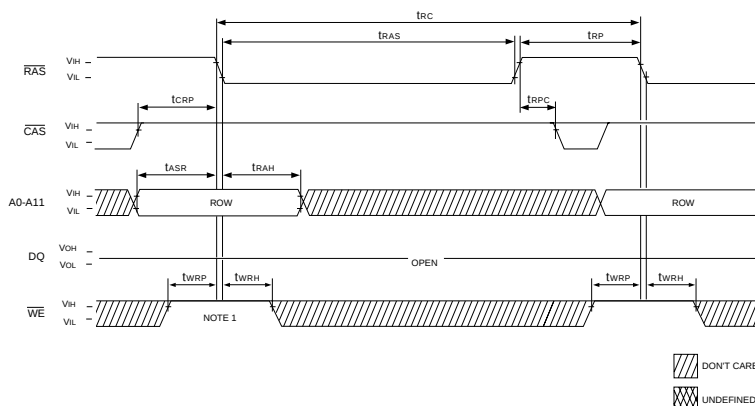


READ CYCLE WITH $\overline{WE}$ CONTROLLED DISABLE



RAS - ONLY REFRESH CYCLE

($\overline{WE}$ and $\overline{OE}$ =Don't Care)



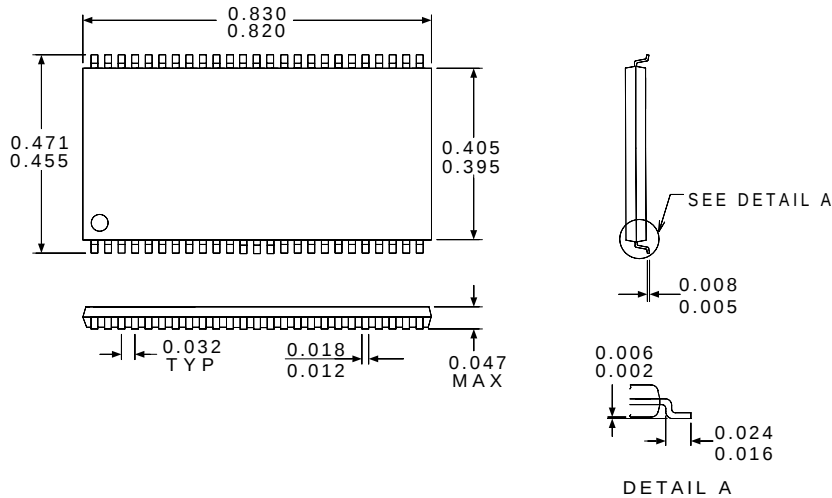


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PACKAGE DESCRIPTION

50 PIN PLASTIC TSOP
PACKAGE NO. 372



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

MILITARY (-55 °C TO +125 °C)

Part No.	Speed (ns)	Package No.
EDI4164MEV50SM	50	372
EDI4164MEV60SM	60	372
EDI4164MEV70SM	70	372

INDUSTRIAL (-40 °C TO +85 °C)

Part No.	Speed (ns)	Package No.
EDI4164MEV50SI	50	372
EDI4164MEV60SI	60	372
EDI4164MEV70SI	70	372