



128Kx8 Monolithic SRAM, SMD 5962-89598

FEATURES

- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- $\overline{CS}$ and $\overline{OE}$ Functions for Bus Control
- 2V Data Retention (EDI88128LPS)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
 - 32 pin Ceramic DIP, 400 mil (Package 102)
 - 32 pin Ceramic DIP, 600 mil (Package 9)
 - 32 lead Ceramic ZIP (Package 100)
 - 32 lead Ceramic SOJ (Package 140)
 - 32 pad Ceramic LCC (Package 141)
 - 32 lead Ceramic Flatpack (Package 142)
- Single +5V ($\pm 10\%$) Supply Operation

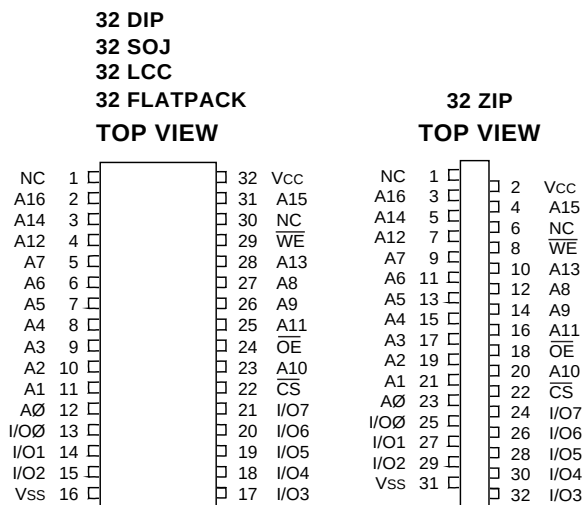
The EDI88128CS is a high speed, high performance, 128Kx8 megabit density Monolithic CMOS Static RAM.

The device has eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

A Low Power version with 2V Data Retention (EDI88128LPS) is also available for battery back-up operation. Military product is available compliant to MIL-PRF-38535.

* 15ns access time is advanced information, contact factory for availability.

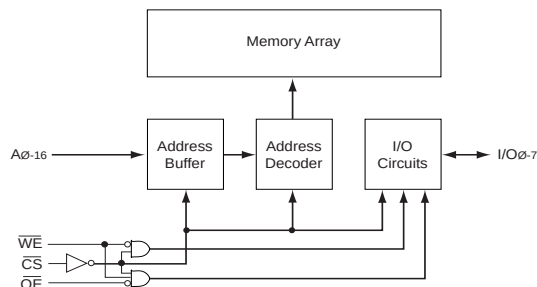
FIG. 1 PIN CONFIGURATION

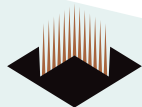


PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
Vcc	Power (+5V $\pm 10\%$)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{OE}$	$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	—	Vcc +0.5	V
Input Low Voltage	VIL	-0.3	—	+0.8	V

CAPACITANCE

(TA = +25°C)

Parameter	Symbol	Condition	Max		Unit
			LCC	CSOJ, ZIP, DIP, Flatpack	
Address Lines	CI	VIN = Vcc or Vss, f = 1.0MHz	6	12	pF
Data Lines	CO	VOU = Vcc or Vss, f = 1.0MHz	8	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(Vcc = 5V, TA = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Leakage Current	ILI	VIN = 0V to Vcc	—	—	±5	μA
Output Leakage Current	ILO	VIO = 0V to Vcc	—	—	±10	μA
Operating Power Supply Current	Icc1	(15-17ns) $\overline{WE}, \overline{CS} = V_{IL}, I/O = 0mA, \text{Min Cycle}$	—	—	300	mA
		(20ns)	—	—	225	mA
		(25-55ns)	—	—	200	mA
Standby (TTL) Power Supply Current	Icc2	(17-55ns) $\overline{CS} \geq V_{IH}, V_{IN} \leq V_{IL}, V_{IN} \geq V_{IH}$	—	—	25	mA
		(15ns)	—	—	60	mA
Full Standby Power Supply Current	Icc3	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	3	10	mA
		CS (17-55ns)	—	—	15	mA
		LPS	—	—	5	mA
Output Low Voltage	VOL	IOL = 8.0mA	—	—	0.4	V
Output High Voltage	VOH	IOH = -4.0mA	2.4	—	—	V

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc - 0.3V



AC CHARACTERISTICS – READ CYCLE (15 to 20ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	15		17		20		ns
Address Access Time	t _{AVQV}	t _{AA}		15		17		20	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		15		17		20	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}		8		8		10	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	0		0		0		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		6		6		8	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		ns
Output Disable to Output in High Z (1)	t _{GHQZ}	t _{OHZ}		6		6		8	ns
Chip Enable to Power Up (1)	t _{ELICCH}	t _{PU}	0		0		0		ns
Chip Enable to Power Down (1)	t _{EHICCL}	t _{PD}		15		17		20	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – READ CYCLE (25 to 55ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	25		35		45		55		ns
Address Access Time	t _{AVQV}	t _{AA}		25		35		45		55	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	3		3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}		12		20		20		20	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	0		0		0		0		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		10		15		20		25	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z (1)	t _{GHQZ}	t _{OHZ}		10		15		20		20	ns
Chip Enable to Power Up (1)	t _{ELICCH}	t _{PU}	0		0		0		0		ns
Chip Enable to Power Down (1)	t _{EHICCL}	t _{PD}		25		35		45		55	ns

1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS

Figure 1

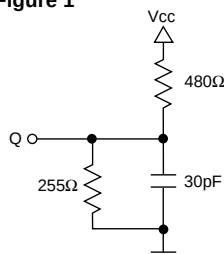
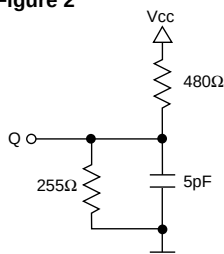
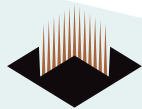


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, C_L = 5pF (Figure 2)



AC CHARACTERISTICS – WRITE CYCLE (12 to 20ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	15		17		20		ns
Chip Enable to End of Write	tELWH	tCW	12		13		15		ns
	tELEH	tCW	12		13		15		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
	tAVEL	tAS	0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	12		13		15		ns
	tAVEH	tAW	12		13		15		ns
Write Pulse Width	tWLWH	tWP	12		13		15		ns
	tWLEH	tWP	12		13		15		ns
Write Recovery Time	tWHAX	tWR	0		0		0		ns
	tEHAX	tWR	0		0		0		ns
Data Hold Time	tWHDX	tDH	0		0		0		ns
	tEHDX	tDH	0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	8	0	8	0	10	ns
Data to Write Time	tDVWH	tDW	7		7		10		ns
	tDVEH	tDW	7		7		10		ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE (25 to 55ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	25		35		45		55		ns
Chip Enable to End of Write	tELWH	tCW	20		25		35		45		ns
	tELEH	tCW	20		25		35		45		ns
Address Setup Time	tAVWL	tAS	0		0		0		0		ns
	tAVEL	tAS	0		0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	20		25		35		45		ns
	tAVEH	tAW	20		25		35		45		ns
Write Pulse Width	tWLWH	tWP	20		30		30		35		ns
	tWLEH	tWP	20		30		30		35		ns
Write Recovery Time	tWHAX	tWR	0		0		5		5		ns
	tEHAX	tWR	0		0		5		5		ns
Data Hold Time	tWHDX	tDH	0		0		0		0		ns
	tEHDX	tDH	0		0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	10	0	13	0	15	0	20	ns
Data to Write Time	tDVWH	tDW	15		20		20		25		ns
	tDVEH	tDW	15		20		20		25		ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.



FIG. 2
TIMING WAVEFORM - READ CYCLE

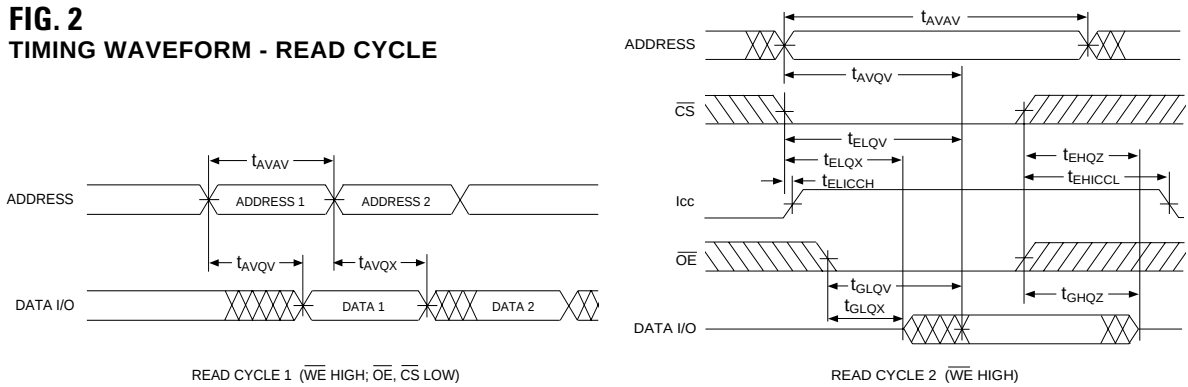


FIG. 3
WRITE CYCLE - $\overline{WE}$ CONTROLLED

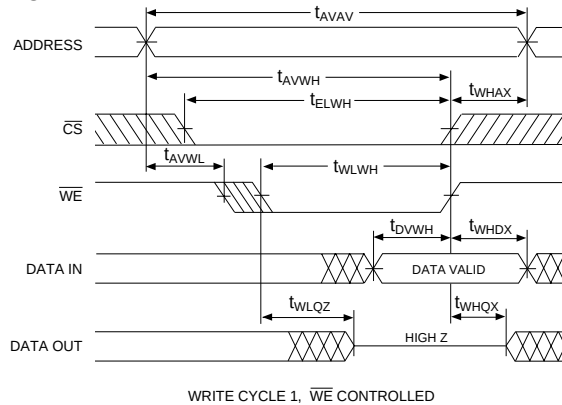
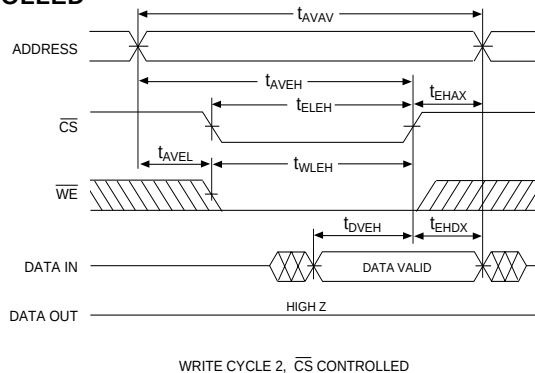
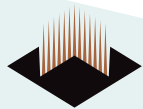


FIG. 4
WRITE CYCLE - $\overline{CS}$ CONTROLLED





DATA RETENTION CHARACTERISTICS (EDI88128LPA ONLY)

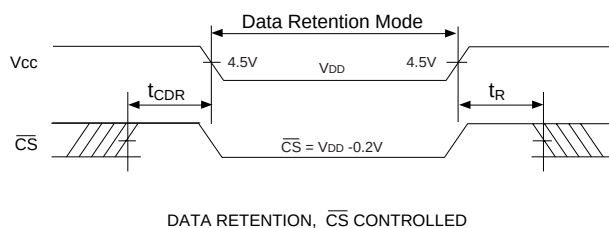
(TA = -55°C to +125°C)

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V _{DD}	V _{DD} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I _{CCDR}	$\overline{CS} \geq V_{DD} - 0.2V$	–	0.5	2	mA
Chip Disable to Data Retention Time (1)	T _{CDR}	V _{IN} ≥ V _{DD} - 0.2V	0	–	–	ns
Operation Recovery Time (1)	T _R	or V _{IN} ≤ 0.2V	T _{AVAV} *	–	–	ns

NOTE:

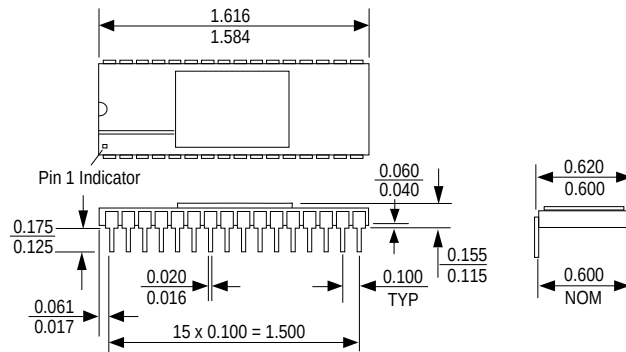
1. Parameter guaranteed by design, but not tested.

* Read Cycle Time

FIG. 5
DATA RETENTION - $\overline{CS}$ CONTROLLED

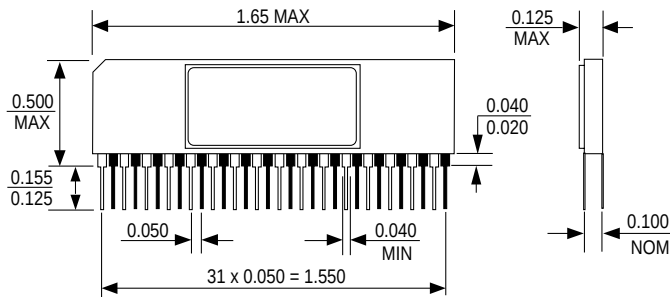


PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600mils wide)



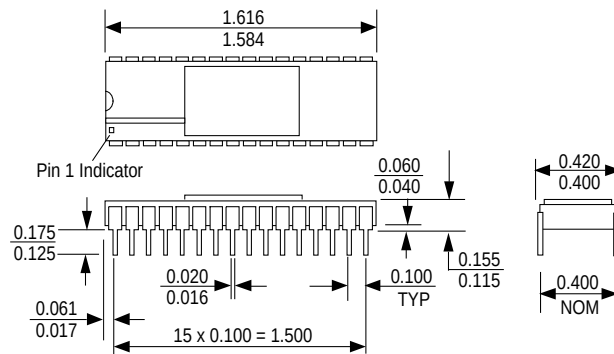
ALL DIMENSIONS ARE IN INCHES

PACKAGE 100: 32 LEAD CERAMIC ZIP



ALL DIMENSIONS ARE IN INCHES

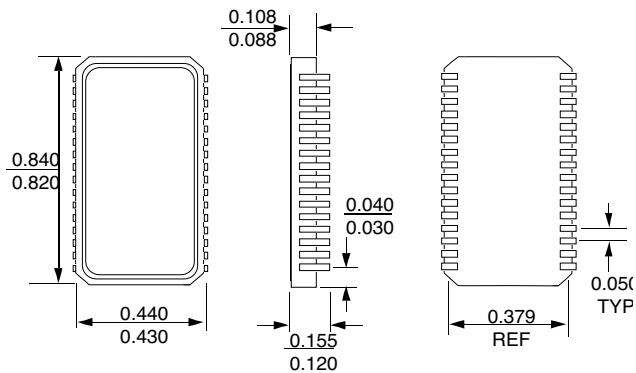
PACKAGE 102: 32 PIN SIDEBRAZED CERAMIC DIP (400mils wide)



ALL DIMENSIONS ARE IN INCHES

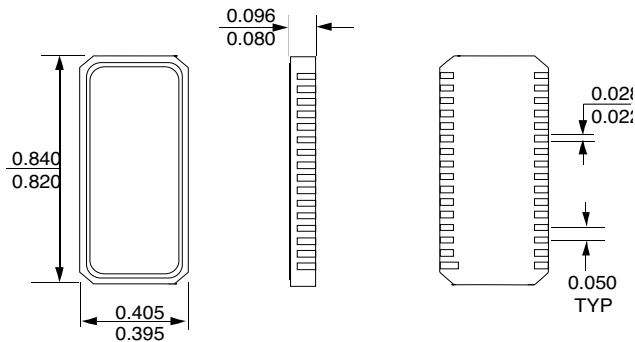


PACKAGE 140: 32 LEAD CERAMIC SOJ



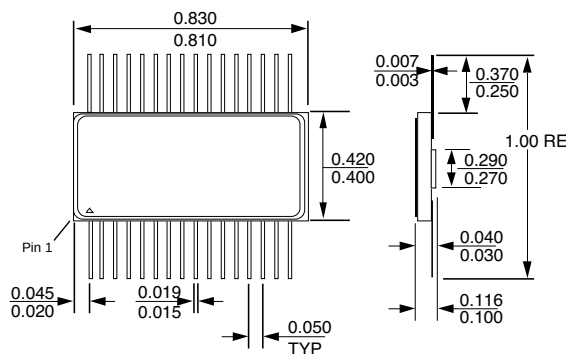
ALL DIMENSIONS ARE IN INCHES

PACKAGE 141: 32 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 142: 32 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 8 128 CS X X X

WHITE ELECTRONIC DESIGNS _____

SRAM _____

ORGANIZATION, 128Kx8 _____

TECHNOLOGY: _____

CS = CMOS Standard Power

LPS = Low Power

ACCESS TIME (ns) _____

PACKAGE TYPE: _____

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

F = 32 lead Ceramic Flatpack (Package 142)

L = 32 pad Ceramic LCC (Package 141)

N = 32 lead Ceramic SOJ (Package 140)

T = 32 lead Sidebrazed DIP, 400 mil (Package 102)

Z = 32 lead Ceramic ZIP (Package 100)

DEVICE GRADE: _____

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C