

•HYUNDAI

HY514370B Series

256K x 16-bit CMOS DRAM with 2 WE & WPB

PRELIMINARY

DESCRIPTION

The HY514370B is the new generation and fast dynamic RAM organized 262,144 x 16-bit configuration employing advanced submicron CMOS process technology and advanced circuit design technique to achieve fast access time. Independent write of upper and lower byte is controlled by 2 separate WE inputs. It gives Write-Per-Bit function useful for graphics applications. Refresh control is provided through RAS-only, CAS-before-RAS, hidden refresh and self refresh modes. The HY514370B conforms to JEDEC pinpoint standards and is available in industry standard 400mil 40pin SOJ and 40/44pin TSOP-II and reverse TSOP-II packages.

FEATURES

- Low power dissipation
 - Max. battery back-up 1.1mW (L-part)
 - Max. CMOS standby 0.825mW (L-part)
 - 5.5mW
 - Max. TTL standby 5.5mW
 - Max. Self refresh 1.1mW (SL-part)
 - Max. operating

Speed	Power
60	605.0mW
70	550.0mW
80	495.0mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access time

Speed	t _{TRC}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	50ns

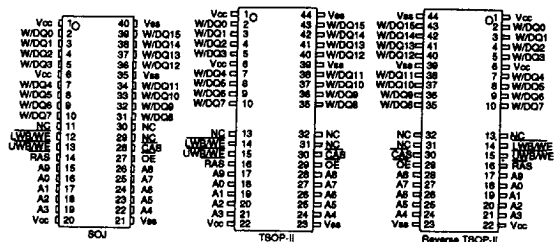
- Fast page mode operation
- 2 WE Inputs for upper and lower byte write control
- Write-Per-Bit Function
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden & Self refresh
- 1024 refresh cycles / 128ms (L-part)
- 1024 refresh cycles / 16ms

PIN DESCRIPTION

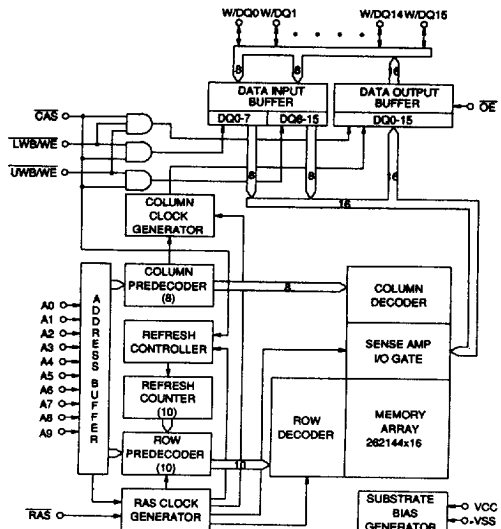
RAS	Row Address Strobe
CAS	Column Address Strobe
LWB/WE, UWB/WE	Write-Per-Bit/Write Enable
OE	Output Enable
A0-A9*	Address Input
W/DQ0-15	Write Mask/Data I/O
Vcc	Power (+5V)
Vss	Ground

* A8 and A9 are applied to row address input only.

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature•Time	260•10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYR.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS≤VIN≤6.5V, All other pins not under test=VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤VOUT≤5.5V, RAS & CAS at VIH		-10	10	μA	
Icc1	Vcc Supply Current, Operating	tRC=tRC (min.)	60 70 80	- - -	110 100 90	mA	1,2,3
Icc2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH, other inputs≥VSS		-	1	mA	
Icc3	Vcc Supply Current, RAS-only refresh	tRC=tRC (min.)	60 70 80	- - -	110 100 90	mA	1,2,3
Icc4	Vcc Supply Current, Fast Page mode	tPC=tPC (min.)	60 70 80	- - -	60 50 45	mA	1,2,3
Icc5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	-	1 0.15	mA	5
Icc6	Vcc Supply Current, CAS-before-RAS refresh	tRC=tRC (min.)	60 70 80	- - -	110 100 90	mA	1,2,3
Icc7	Vcc Supply Current, Battery Back Up (L-part only)	tRC=125μs, tRAS ≤ 1μs CAS=CBR cycling or 0.2V OE & WB/WE=VCC-0.2V, A0-A9=VCC-0.2V or 0.2V W/DQ0-15=0.2V, VCC-0.2V or open		-	200	μA	1,4,5
Icc8	Vcc Supply Current, Self refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as Icc7		-	200	μA	6
VOL	Output Low Voltage	IOL=4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH=-5mA		2.4	-	V	

NOTE :

1. Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
2. Icc1, Icc3, Icc4 and Icc6 are dependent on output loading. Specified values are obtained with the output open.
3. Icc is specified as average current. Icc1, Icc3, Icc6, Address can be changed maximum two times while RAS=VIL. Icc4, Address can be changed maximum once while CAS=VIH.
4. Only tRAS(max.)=1μs is applied to refresh of battery backup but tRAS(max.)=10μs is applied to normal functional operation.
5. Icc5(max.)=0.15mA and Icc7 are applied to L-parts (HY514370BLJC, HY514370BLTC, HY514370BLRC, HY514370BSLJC, HY514370BSLTC and HY514370BSLRC).
6. Icc8 is applied to SL-parts only (HY514370BSLJC, HY514370BSLTC and HY514370BSLRC).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.) NOTE : 1, 2, 3, 13

(TA=+0°C to +70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)										
#	SYMBOL	PARAMETER	HY514370BJC/TC/RC/LJC/LTC/LRC/ SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	80	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from Column Precharge	-	35	-	35	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	17
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6,14
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	16
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	16
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	15,16
34	tRWL	Write Command to RAS Lead Time	20	-	20	-	20	-	ns	15
35	tCWL	Write Command to CAS Lead Time	20	-	20	-	20	-	ns	15,18
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7,14
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (1024cycles)		- 16	-	16	-	16	ms	12
		L-part		- 128	-	128	-	128		11
40	twCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

			HY514370BJC/TC/RC/LJC/LTC/LRC/ SLJC/SLTC/SLRC						UNIT	NOTE	
#	SYMBOL	PARAMETER	-60		-70		-80				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
41	tCWD	CAS to WE Delay Time	45	-	50	-	50	-	ns	8,14	
42	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	8,14	
43	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	8,14	
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns		
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns		
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns		
47	tCPT	CAS Precharge Time (CBR Counter Test)		30	-	35	-	40	-	ns	
48	tROH	RAS Hold Time Reference to OE	0	-	0	-	0	-	ns		
49	tOEA	OE Access Time	-	15	-	20	-	20	ns		
50	tOED	OE to Data Delay	15	-	20	-	20	-	ns		
51	tOEZ	Output Buffer Turn Off Delay Time from OE		0	15	0	20	0	20	ns5	
52	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	15	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	8	
54	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns		
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	5	-	5	-	5	-	ns		
56	tWPH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns		
57	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs		
58	tRPS	RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns		
59	tCHS	CAS Hold Time from RAS (Self Refresh)	-50	-	-50	-	-50	-	ns		
60	tWBS	Write-Per-Bit Set-Up Time	0	-	0	-	0	-	ns		
61	tWBH	Write-Per-Bit Hold Time	10	-	10	-	10	-	ns		
62	tWDS	Write-Per-Bit Selection Set-Up Time	0	-	0	-	0	-	ns		
63	tWDH	Write-Per-Bit Selection Set-Up Time	10	-	10	-	10	-	ns		

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required.
2. If RAS=Vss during power-up, the HY514370B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH=2.4V and VOL=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. tOFF(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to LWE or UWE leading edge in Read-Modify-Write cycles.
8. twCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD $\geq$ tRWD(min.), tCWD $\geq$ tCWD(min.), tAWD $\geq$ tAWD(min.), and tCPWD $\geq$ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=128ms is applied to L-parts (HY514370BLJC, HY514370BLTC, HY514370BLRC, HY514370BSLJC, HY514370BSLTC and HY514370BSLRC).
12. A burst of 1024 CAS-before-RAS refresh cycles must be executed within 16ms (128ms for L-part) after exiting self refresh.
13. When both LWE and UWE go low at the same time, all 16-bits data are written into the device. LWE and UWE must be transited simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of LWE or UWE.
15. These parameters are determined by the later falling edge of LWE or UWE.
16. These parameters are determined by the earlier rising edge of LWE or UWE.
17. These parameters are determined by the later rising edge of LWE or UWE.
18. tcwl must be satisfied by both LWE and UWE for 16-bits access cycles.

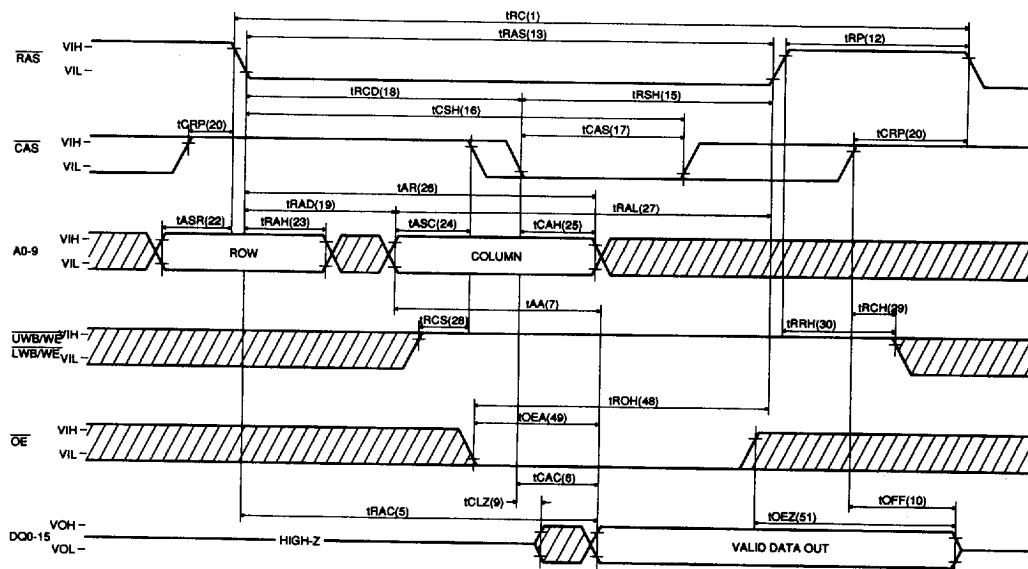
CAPACITANCE

(TA=25°C, VCC=5V $\pm$ 10%, VSS=0V, f=1MHz, unless otherwise noted.)

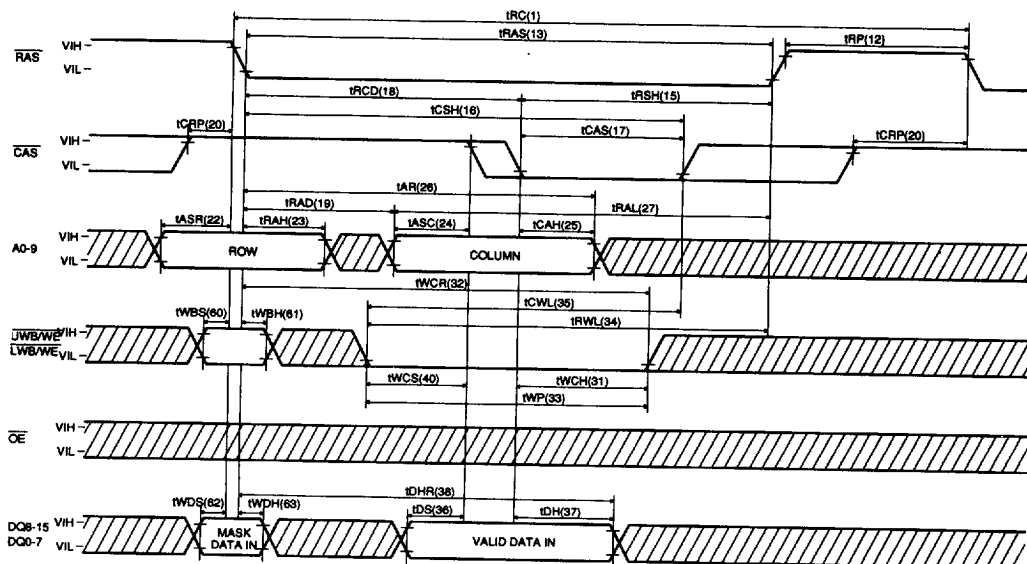
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, LWB/WE, UWB/WE, OE)	-	7	pF
CdQ	Data Input/Output Capacitance (W/DQ0-DQ15)	-	7	pF

TIMING DIAGRAM

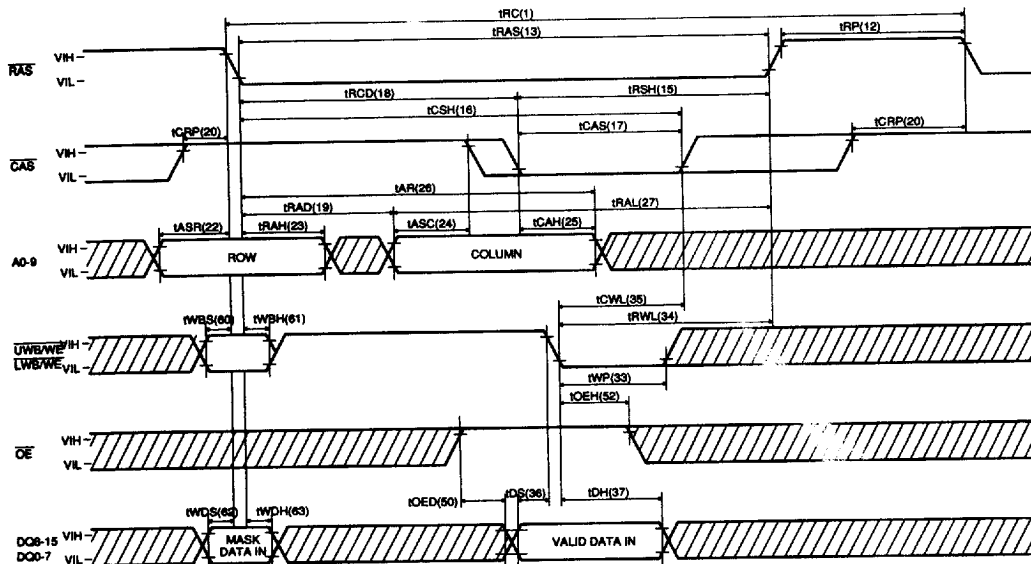
READ CYCLE



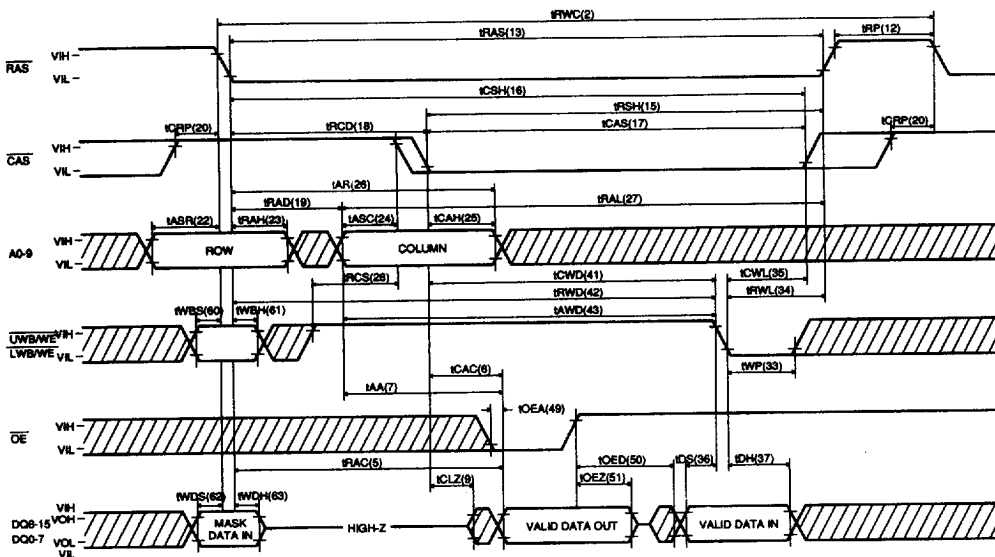
EARLY WRITE CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



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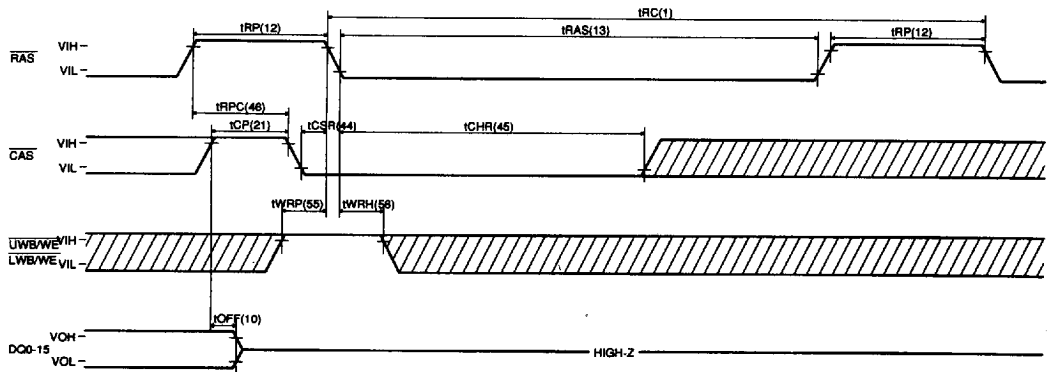
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Timing diagram showing the relationship between RAS, CAS, and AO-S signals. The diagram includes the following parameters:

- $t_{RC}(1)$: Row Address Strobe to Row Address Strobe delay
- $t_{RAS}(19)$: Row Address Strobe pulse width
- $t_{RP}(12)$: Row Address Strobe to Row Address Strobe delay
- $t_{CRP}(20)$: Row Address Strobe to Row Address Strobe delay
- $t_{RPC}(46)$: Row Address Strobe to Row Address Strobe delay
- $t_{ASR}(22)$: Row Address Strobe to Row Address Strobe delay
- $t_{RAH}(23)$: Row Address Strobe to Row Address Strobe delay

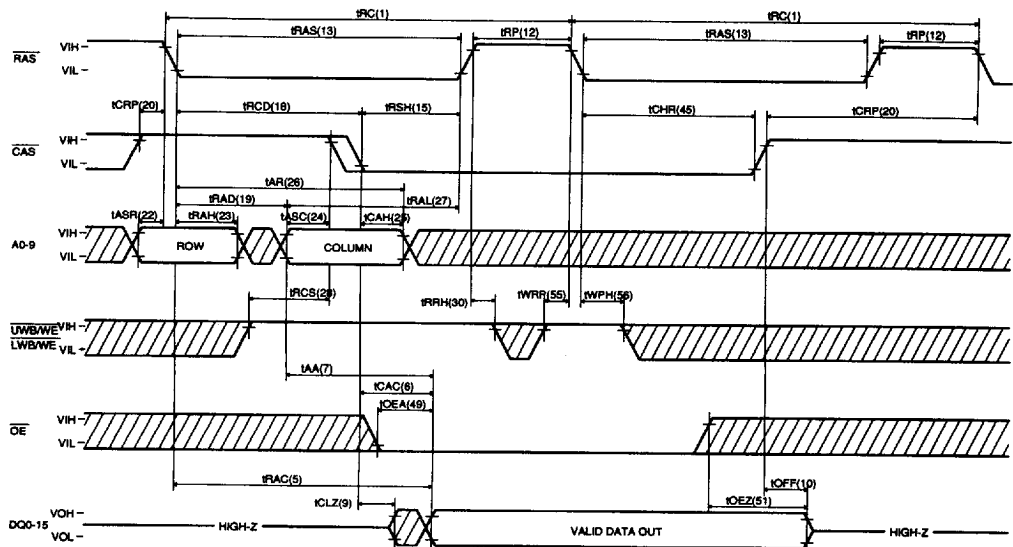
NOTE : OE and WB/WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

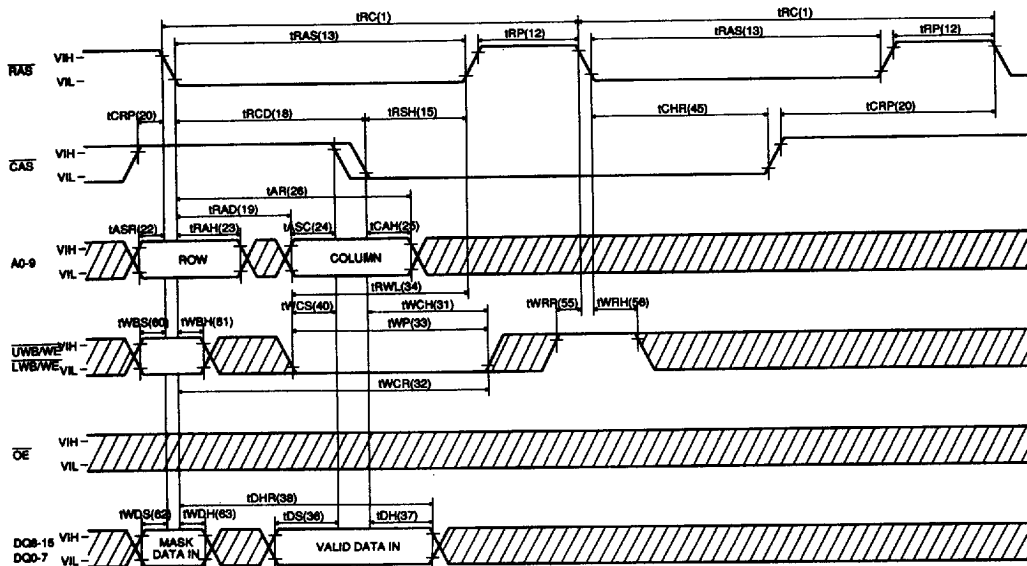


NOTE : A0-8 and OE = "H" or "L"

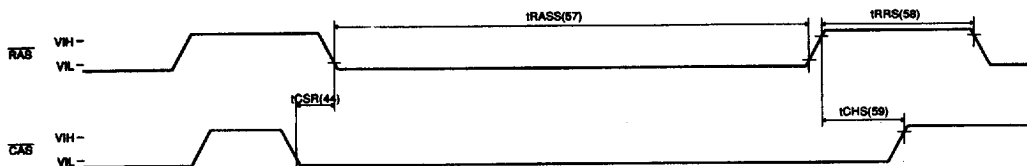
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

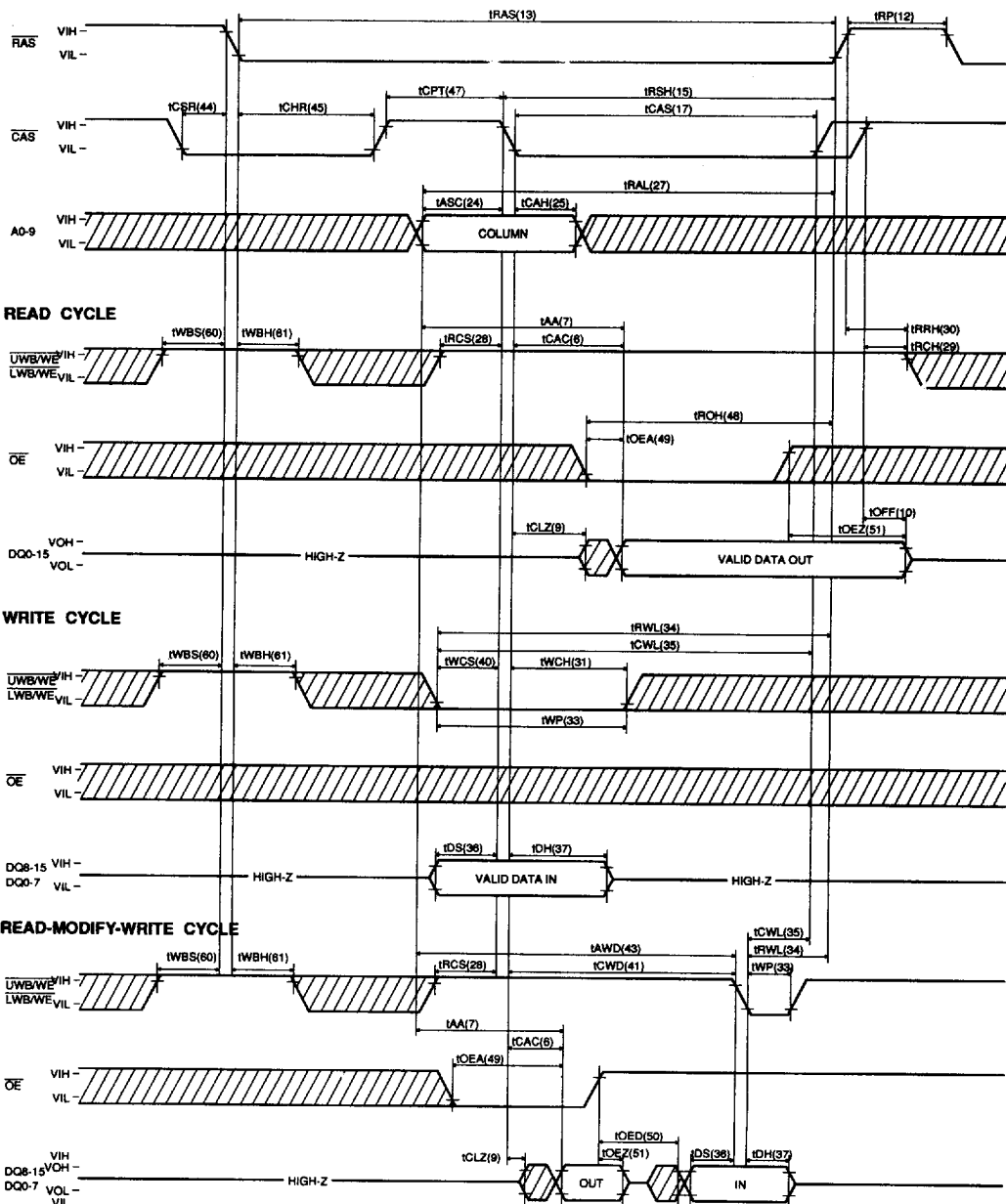


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-8, WB/WE and OE = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



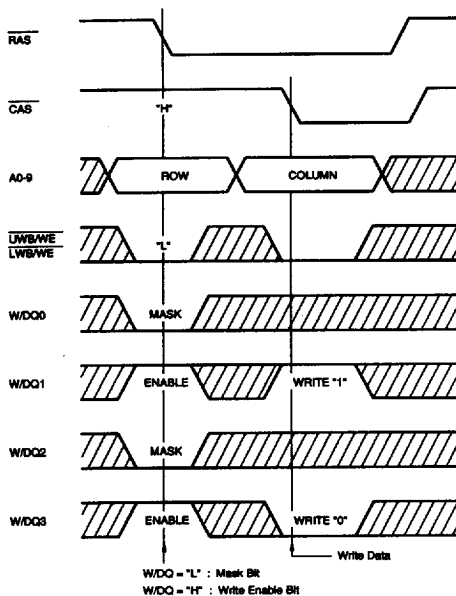
WRITE-PER-BIT FUNCTION

The Write-Per-Bit function selectively controls the internal write enable circuit of the HY514370B. When WB/WE is held "Low" at the falling edge of RAS during a random access operation, the write mask is enabled. At the same time, the mask data on the W/DQ pins is located onto the write mask register (WMR). When a "0" is sensed on any of the W/DQ pins, their corresponding write circuits are disabled and new data will not be written. When "1" is sensed on any of the W/DQ pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the Write-Per-Bit function and an example of the Write-Per-Bit function illustrating its application to displays are shown below.

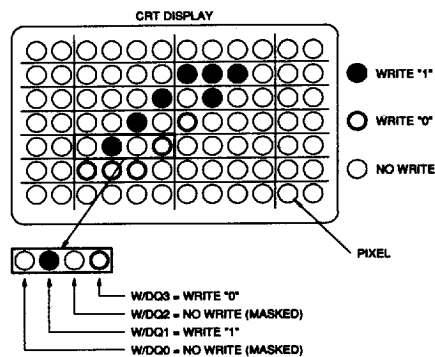
TRUTH TABLE FOR WRITE-PER-BIT FUNCTION

at the falling edge of RAS			Function
CAS	WB/WE	W/DQ0-15	
H	H	Don't Care	Write Enable
H	L	1	Write Enable
		0	Write Mask

WRITE-PER-BIT TIMING DIAGRAM

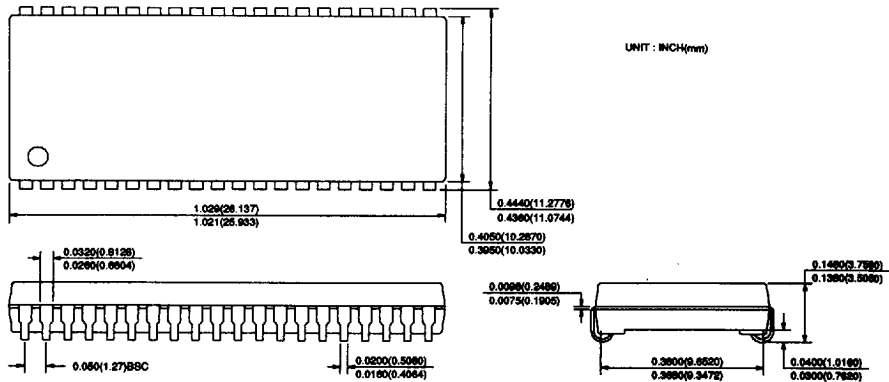


CORRESPONDING BIT MAP

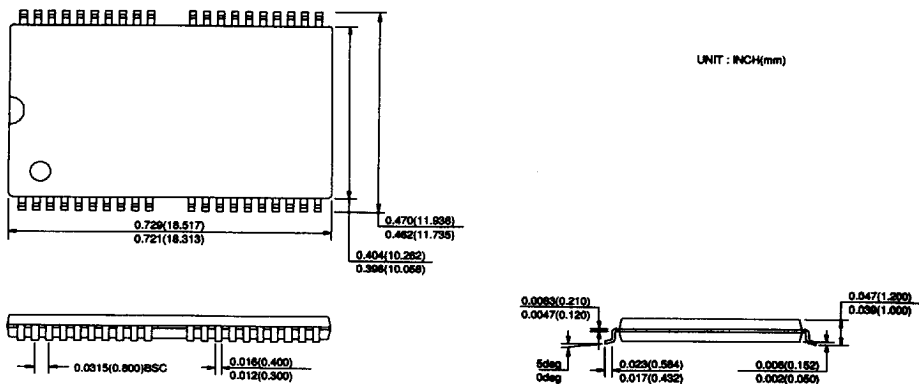


PACKAGE INFORMATION

400 mil 40 pin Small Outline J-form Package (JC)



400 mil 40/44 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY514370BJC	60/70/80		SOJ
HY514370BLJC	60/70/80	L-part	SOJ
HY514370BSLJC	60/70/80	SL-part	SOJ
HY514370BTC	60/70/80		TSOP-II
HY514370BLTC	60/70/80	L-part	TSOP-II
HY514370BSLTC	60/70/80	SL-part	TSOP-II
HY514370BRC	60/70/80		TSOP-II(R)
HY514370BLRC	60/70/80	L-part	TSOP-II(R)
HY514370BSLRC	60/70/80	SL-part	TSOP-II(R)