# 3.3V CMOS QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

**IDT74ALVC125**

## FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC}$ = 3.3V ± 0.3V, Normal Range
- $V_{CC}$ = 2.7V to 3.6V, Extended Range
- $V_{CC}$ = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SOIC, SSOP and TSSOP packages

**Drive Features for ALVC125:**

- High Output Drivers: ±24mA
- Suitable for heavy loads

## DESCRIPTION:

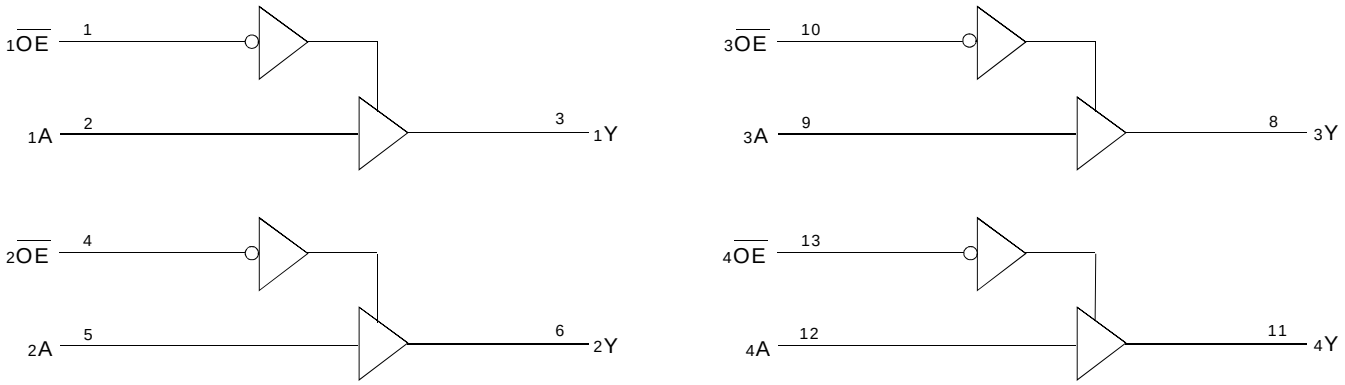
This quadruple bus buffer gate is built using advanced dual metal CMOS technology. The ALVC125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

The ALVC125 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

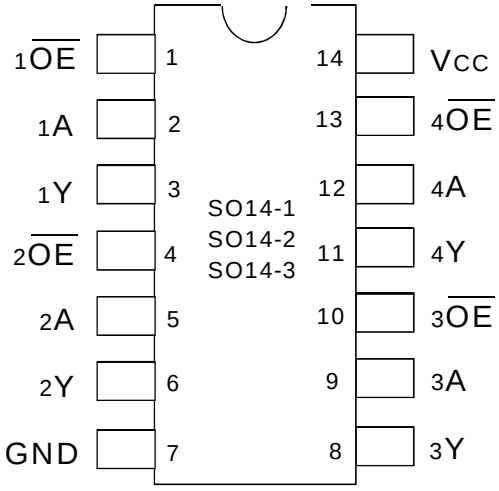
## APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SOIC/ SSOP/ TSSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | – 0.5 to + 4.6 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | – 0.5 to $V_{CC}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | – 65 to + 150 | °C |
| $I_{OUT}$ | DC Output Current | – 50 to + 50 | mA |
| $I_{IK}$ | Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$ | ± 50 | mA |
| $I_{OK}$ | Continuous Clamp Current, $V_O < 0$ | – 50 | mA |
| $I_{CC}$ $I_{SS}$ | Continuous Current through each $V_{CC}$ or GND | ±100 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | 9 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 7 | 9 | pF |

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**NOTE:**
1. As applicable to the device type.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| x$\overline{OE}$ | Output Enable Inputs (Active LOW) |
| xA | Data Inputs |
| xY | 3-State Outputs |

## FUNCTION TABLE (each buffer)(1)

| Inputs | | Output |
|---|---|---|
| x$\overline{OE}$ | xA | xY |
| L | H | H |
| L | L | L |
| H | X | Z |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Operating Condition: $T_A$ = –40°C to +85°C**

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = 3.6V | $V_I$ = $V_{CC}$ | — | — | ± 5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = 3.6V | $V_I$ = GND | — | — | ± 5 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = 3.6V | $V_O$ = $V_{CC}$ | — | — | ± 10 | µA |
| $I_{OZL}$ | (3-State Output pins) | | $V_O$ = GND | — | — | ± 10 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = – 18mA | | — | – 0.7 | – 1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$ $I_{CCH}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V $V_{IN}$ = GND or $V_{CC}$ | | — | 0.1 | 10 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ – 0.6V, other inputs at $V_{CC}$ or GND | | — | — | 750 | µA |

**NOTE:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

# OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions(1) | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3.0V | | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = – 24mA | 2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 24mA | — | 0.55 | |

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**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $T_A = 25^oC$

| Symbol | Parameter | Test Conditions | Vcc = 2.5V ± 0.2V | Vcc = 3.3V ± 0.3V | Unit |
|---|---|---|---|---|---|
| | | | Typical | Typical | |
| $C_{PD}$ | Power Dissipation Capacitance per gate Outputs enabled | $C_L$ = 0pF, f = 10Mhz | 20 | 30 | pF |
| $C_{PD}$ | Power Dissipation Capacitance per gate Outputs disabled | | 3 | 6 | pF |

## SWITCHING CHARACTERISTICS (1)

| Symbol | Parameter | Vcc = 2.5V ± 0.2V | | Vcc = 2.7V | | Vcc = 3.3V ± 0.3V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>xA to xY | 1 | 3.1 | 1 | 3.1 | 1.1 | 3 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>x$\overline{OE}$ to xY | 1.5 | 5.4 | 1.5 | 5.3 | 1.5 | 4.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>x$\overline{OE}$ to xY | 1 | 4.1 | 1.3 | 4.4 | 1.7 | 4.2 | ns |

**NOTE:**
1. See test circuits and waveforms. $T_A$ = – 40°C to + 85°C.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$= 3.3V ± 0.3V | $V_{CC}^{(1)}$ = 2.7V | $V_{CC}^{(2)}$= 2.5V ± 0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |

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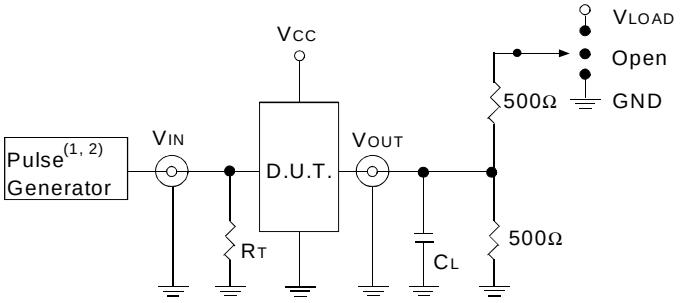
## TEST CIRCUITS FOR ALL OUTPUTS

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**DEFINITIONS:**

$C_L$= Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

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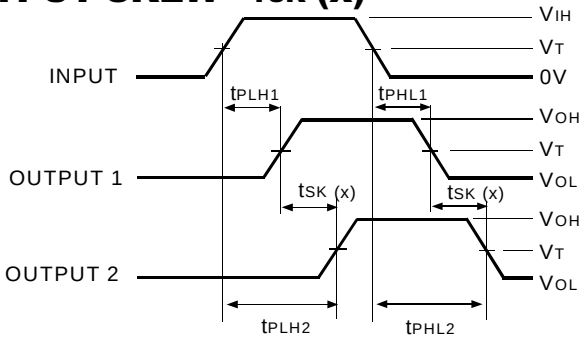
## OUTPUT SKEW - $t_{SK}$ (x)




$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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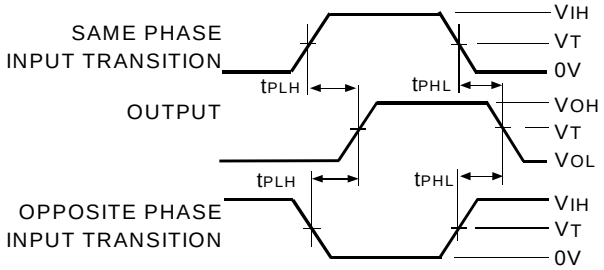
**NOTES:**

1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY

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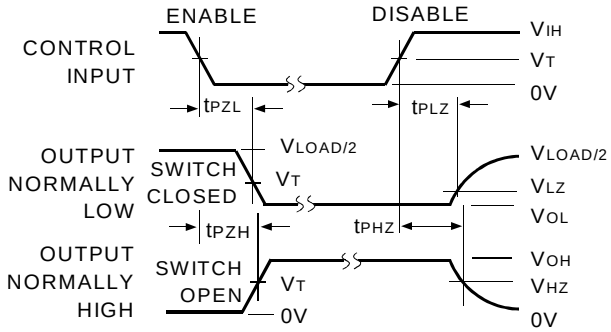
## ENABLE AND DISABLE TIMES

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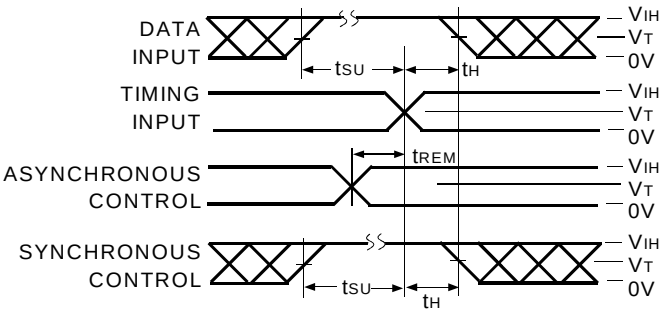
**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

## SET-UP, HOLD, AND RELEASE TIMES

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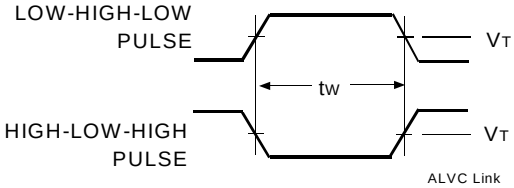
## PULSE WIDTH

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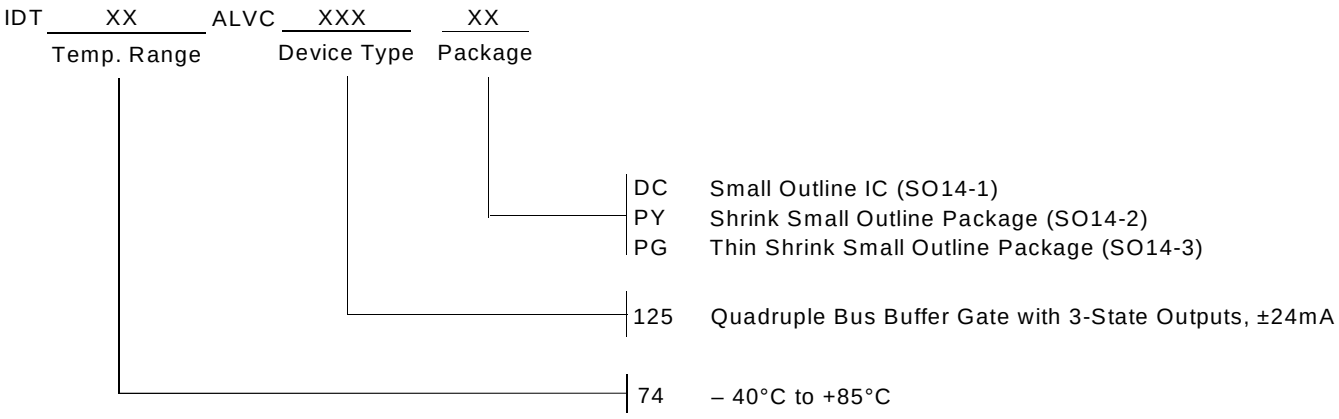
# ORDERING INFORMATION

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