| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| | | | |

| | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | | | |
| REV STATUS OF SHEETS | REV | | | | | | | | | | | | | | | | | | | | | | | | | |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | | | | | | | | | |

| | | |
|---|---|---|
| PMIC N/A | PREPARED BY Joseph A. Kerby | DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 |
| STANDARDIZED MILITARY DRAWING | CHECKED BY Charles E. Besore | MICROCIRCUITS, LINEAR, TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS, MONOLITHIC SILICON |
| THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE | APPROVED BY [signature] | SIZE A / CAGE CODE 67268 / 5962-90628 |
| | DRAWING APPROVAL DATE 91-02-15 | |
| AMSC N/A | REVISION LEVEL | SHEET 1 OF 15 |

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1729-1

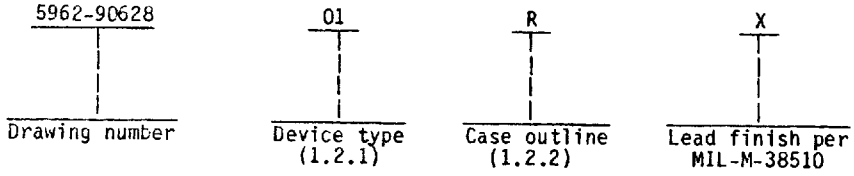
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0001584 911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:




1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 55ALS056 | Trapezoidal-waveform interface bus transceivers |

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| R | D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package |
| S | F-9 (20-lead, .540" x .300" x .100"), flat package |
| 2 | C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package |

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | 6.0 V dc |
| Control input voltage | 5.5 V dc |
| Driver input voltage | 5.5 V dc |
| Driver output voltage | 2.5 V dc |
| Receiver input voltage | 2.5 V dc |
| Receiver output voltage | 5.5 V dc |
| Continuous power dissipation ($P_D$) 1/: | |
| Cases R and 2 | 1375 mW |
| Case S | 1000 mW |
| Storage temperature range | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | 300°C |
| Junction temperature ($T_J$) | 150°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | 4.5 V dc minimum to 5.5 V dc maximum |
| Mimimum high-level input voltage ($V_{IH}$) | 2.0 V dc |
| Maximum low-level input voltage ($V_{IL}$) | 0.8 V dc |
| Bus termination voltage | 1.9 V dc to 2.1 V dc |
| Ambient operating temperature range ($T_A$) | -55°C to +125°C |

1/ For operation above 25°C free-air temperature, derate case outlines R and 2 at the rate of 11 mW/°C and case S at 8 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and truth table. The terminal connections and truth table shall be as specified on figure 1 .

3.2.2 Driver delay waveforms. The driver delay waveforms shall be as specified on figure 2.

3.2.3 Delay waveforms from $T/\overline{R}$ to Bn The delay waveforms from T/R to Bn shallbe as specified on figure 3.

3.2.4 Receiver delay waveforms. The receiver delay waveforms shall be as specified on figure 4.

3.2.5 Delay waveforms from $\overline{CS}$ or $T/\overline{R}$ to An. Delay waveforms from $\overline{CS}$ or $T/\overline{R}$ to An shall be as specified on figure 5.

3.2.6 Receiver noise immunity waveforms. The receiver noise immunity waveforms shall be as specified on figure 6.

TABLE I. Electrical performance characteristics.

| Test | | Symbol | Conditions $-55°C < T_A < +125°C$ unless otherwise specified | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High-level output voltage at An | | $V_{OH}$ | $V_{CC}$ = 4.5 V dc, Bn at 1.2 V dc, $I_{OH}$ = -400 µA, T/$\overline{R}$ at 0.8 V dc, $\overline{CS}$ at 0.8 V dc | 1,2,3 | 2.4 | | V |
| Low-level output voltage | An | $V_{OL}$ | $V_{CC}$ = 4.5 V dc, $I_{OL}$ = 16 mA, Bn at 2 V dc, T/$\overline{R}$ at 0.8 V dc, $\overline{CS}$ at 0.8 V dc | 1,2,3 | | 0.5 | |
| | Bn | | $V_{CC}$ = 4.5 V dc, An at 2 V d, T/$\overline{R}$ at 2 V dc, $\overline{CS}$ at 0.8 V dc | | 0.75 | 1.2 | |
| Input cla p voltage at An, T/$\overline{R}$ and $\overline{CS}$ | | $V_{IC}$ | $V_{CC}$ = 4.5 V dc, $I_I$ = -18 mA | 1,2,3 | | -1.5 | |
| Receiver input threshold at Bn | | $V_T$ | $V_{CC}$ = 5.0 V dc | 1 | 1.45 | 1.65 | |
| | | | | 2,3 | 1.4 | 1.7 | |
| Short circuit output current at An | | $I_{OS}$ | $V_{CC}$ = 5.5 V dc, Bn at 1.2 V dc, An at 0.0 V dc, T/$\overline{R}$ at 0.8 V, $\overline{CS}$ at 0.8 V dc | 1,2,3 | -35 | -125 | µA |
| High-level input current | An, T/$\overline{R}$, and $\overline{CS}$ | $I_{IH}$ | $V_{CC}$ = 5.5 V dc, $V_I$ = $V_{CC}$ | 1,2,3 | | 40 | µA |
| | Bn | | $V_{CC}$ = 5.5 V dc, $V_I$ = 2.0 V dc, An at 0.8 V dc, T/$\overline{R}$ at 0.8 V dc | | | 100 | |
| Low-level input c rrent at An, T/$\overline{R}$, and $\overline{CS}$ | | $I_{IL}$ | $V_{CC}$ = 5.5 V dc, $V_I$ = 0.4 V dc | 1,2,3 | | -400 | |
| Supply current | | $I_{CC}$ | $V_{CC}$ = 5.5 V dc | 1,2,3 | | 85 | mA |
| Functional test 1/ | | | See 4.3.1c. | 7,8 | | | |

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Driver** | | | | | | |
| Propagation delay time, from An to Bn | $t_{PLH1}$ | $\overline{CS}$ at 0.8 V dc, T/$\overline{R}$ at 2.0 V dc, $V_L$ = 2.0 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, See figure 2 | 9 | | 10 | ns |
| | | | 10,11 | | 40 | |
| | $t_{PHL1}$ | | 9 | | 12 | |
| | | | 10,11 | | 15 | |
| Propagation delay time, from $\overline{CS}$ to Bn | $t_{PLH2}$ | An and T/$\overline{R}$ at 2.0 V dc, $V_L$ = 2.0 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, See figure 2 | 9 | | 18 | |
| | | | 10,11 | | 30 | |
| | $t_{PHL2}$ | | 9 | | 20 | |
| | | | 10,11 | | 22 | |
| Propagation delay time, from T/$\overline{R}$ to Bn | $t_{PLH3}$ | $V_L$ = 2.0 V dc, $\overline{CS}$ at 0.8 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, See figure 3 | 9 | | 18 | |
| | | | 10,11 | | 37 | |
| | $t_{PHL3}$ | | 9 | | 18 | |
| | | | 10,11 | | 21 | |
| Transition time, from An to Bn | $t_{TLH}$ | $\overline{CS}$ at 0.8 V dc, T/$\overline{R}$ at 2.0 V dc, $V_L$ = 2.0 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, See figure 2 | 9 | | 8 | |
| | | | 10,11 | | 33 | |
| | $t_{THL}$ | | 9 | | 10 | |
| | | | 10,11 | | 13 | |
| **Receiver** | | | | | | |
| Propagation delay time, from Bn to An | $t_{PLH4}$ | $\overline{CS}$ at 0.8 V dc, T/$\overline{R}$ at 0.8 V dc, $V_L$ = 5.0 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, See figure 4 S1 closed | 9 | | 20 | ns |
| | | | 10,11 | | 22 | |
| | $t_{PHL4}$ | | 9 | | 18 | |
| | | | 10,11 | | 20 | |
| Output disable time, from $\overline{CS}$ to An | $t_{PLZ1}$ | Bn at 2.0 V dc, $V_L$ = 5.0 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, | 9 | | 20 | |
| | | | 10,11 | | 22 | |
| Output enable time, from $\overline{CS}$ to An | $t_{PZL1}$ | T/$\overline{R}$ at 0.8 V dc, See figure 5 S1 closed | 9 | | 13 | |
| | | | 10,11 | | 14 | |

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_A \le +125°C$ unless otherwise sprcified | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Receiver** | | | | | | |
| Output disable time, from $\overline{CS}$ to An | $t_{PHZ1}$ | Bn at 0.8 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, T/R at 0.8 V dc, See figure 5 S1 open | 9 | | 12 | ns |
| | | | 10,11 | | 13 | |
| Output enable time, from $\overline{CS}$ to An | $t_{PZH1}$ | Bn at 0.8 V dc, $V_{CC}$ = 4.5 to 5.5 V dc, T/$\overline{R}$ at 0.8 V dc See figure 5 S1 open | 9 | | 14 | ns |
| | | | 10,11 | | 22 | |
| Output disable time, from T/$\overline{R}$ to An | $t_{PLZ2}$ | $V_I$ (An, Bn) = 2.0 V dc, $V_L$ = 5.0 V dc, $\overline{CS}$ at 0.8 V dc, See figure 5 $V_{CC}$ = 4.5 to 5.5 V dc, S1 closed | 9 | | 17 | |
| | | | 10,11 | | 20 | |
| Output enable time, from T/$\overline{R}$ to An | $t_{PZL2}$ | $V_I$ (An, Bn) = 2.0 V dc, $V_L$ = 5.0 V dc, $\overline{CS}$ at 0.8 V dc, See figure 5 $V_{CC}$ = 4.5 to 5.5 V dc, S1 closed | 9 | | 25 | |
| | | | 10,11 | | 40 | |
| Output disable time, from T/$\overline{R}$ to An | $t_{PHZ2}$ | $V_L$ = 0.0 V dc, $\overline{CS}$ at 0.8 V dc, See figure 5 $V_{CC}$ = 4.5 to 5.5 V dc, S1 closed | 9 | | 12 | |
| | | | 10,11 | | 13 | |
| Output enable time, from T/$\overline{R}$ to An | $t_{PZH2}$ | $\overline{CS}$ at 0.8 V dc, See figure 5 $V_{CC}$ = 4.5 to 5.5 V dc, S1 open | 9 | | 15 | |
| | | | 10,11 | | 22 | |
| Receiver noise rejection pulse duration from Bn to An | $t_{W(NR)}$ | See figure 6, S1 closed, $V_{CC}$ = 4.5 to 5.5 V dc, $V_L$ = 5.0 V dc | 9 | 4 | | |
| | | | 10,11 | 2 | | |

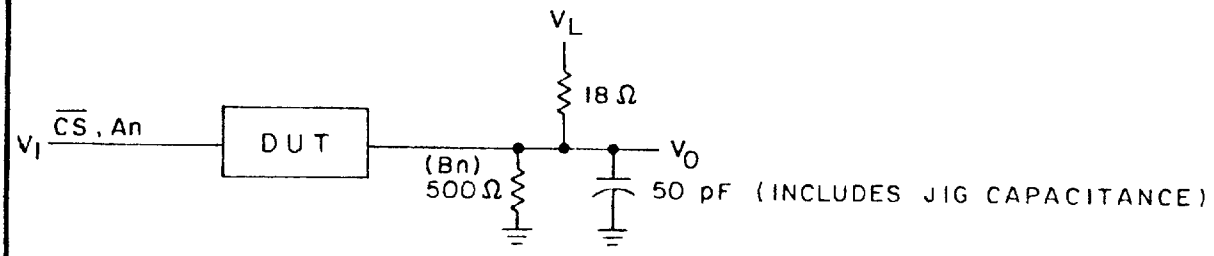
1/ Functional test shall be conducted at input test conditions of GND $\le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

| Device type | 01 |
|---|---|
| Case outlines | R, S, and 2 |
| Terminal number | Terminal symbol |
| 1 | A1 |
| 2 | A2 |
| 3 | A3 |
| 4 | A4 |
| 5 | $V_{CC}$ |
| 6 | A5 |
| 7 | A6 |
| 8 | A7 |
| 9 | A8 |
| 10 | $\overline{CS}$ |
| 11 | T/$\overline{R}$ |
| 12 | B8 |
| 13 | B7 |
| 14 | B6 |
| 15 | B5 |
| 16 | GND |
| 17 | B4 |
| 18 | B3 |
| 19 | B2 |
| 20 | B1 |

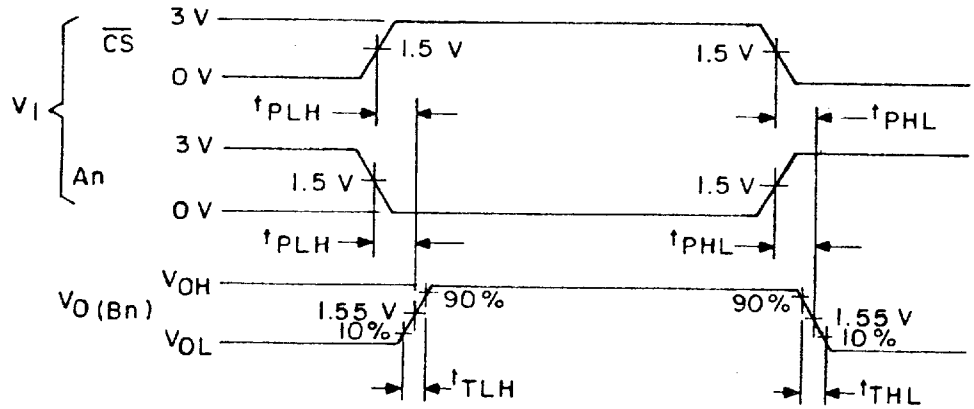
| Controls | | Channels |
|---|---|---|
| $\overline{CS}$ | T/$\overline{R}$ | A ↔ B |
| L | H | T(A → B) |
| L | L | R(B → A) |
| H | X | D |

NOTE:
H = high level,
L = low level,
R = receive,
T = transmit,
D = disable,
X = irrelevant.

FIGURE 1. Terminal connections and truth table.



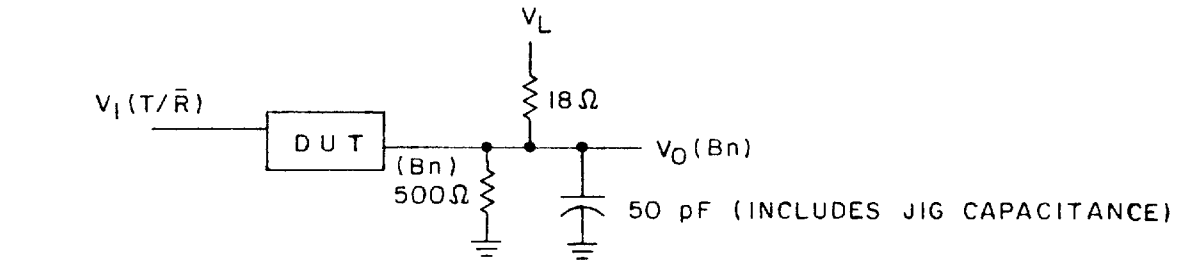

TEST CIRCUIT



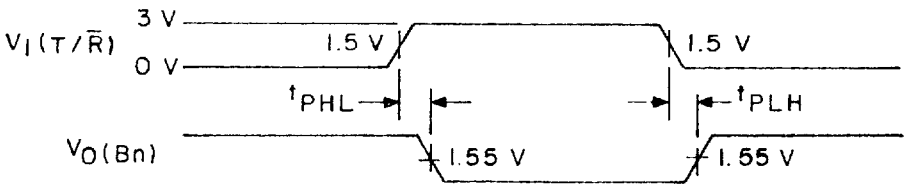

VOLTAGE WAVEFORMS

NOTE: FOR $V_I(\overline{CS})$, $t_r = t_f \leq 5$ ns FROM 10% TO 90%

FIGURE 2. Driver delay waveforms.



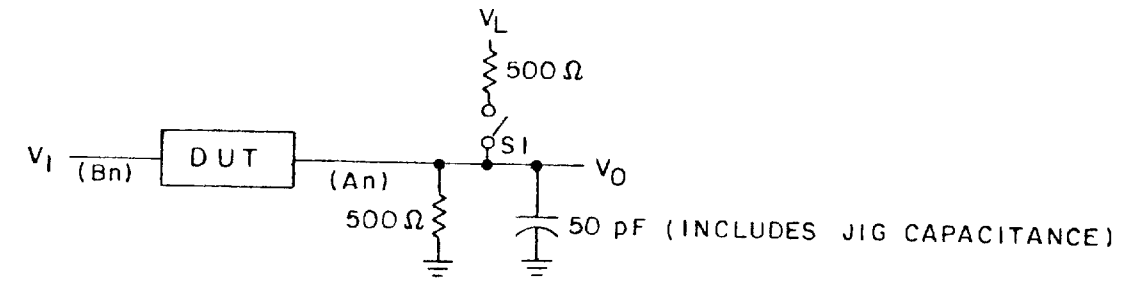

TEST CIRCUIT



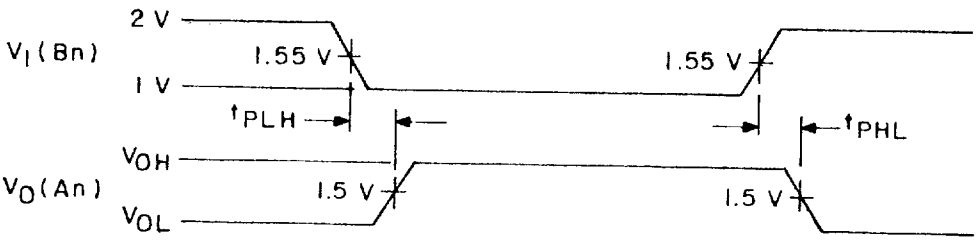

VOLTAGE WAVEFORMS

NOTE: FOR $V_I(T/\overline{R})$, $t_r = t_f \leq 5$ ns FROM 10 % TO 90 %

FIGURE 3. Delay waveforms from $T/\overline{R}$ to Bn.



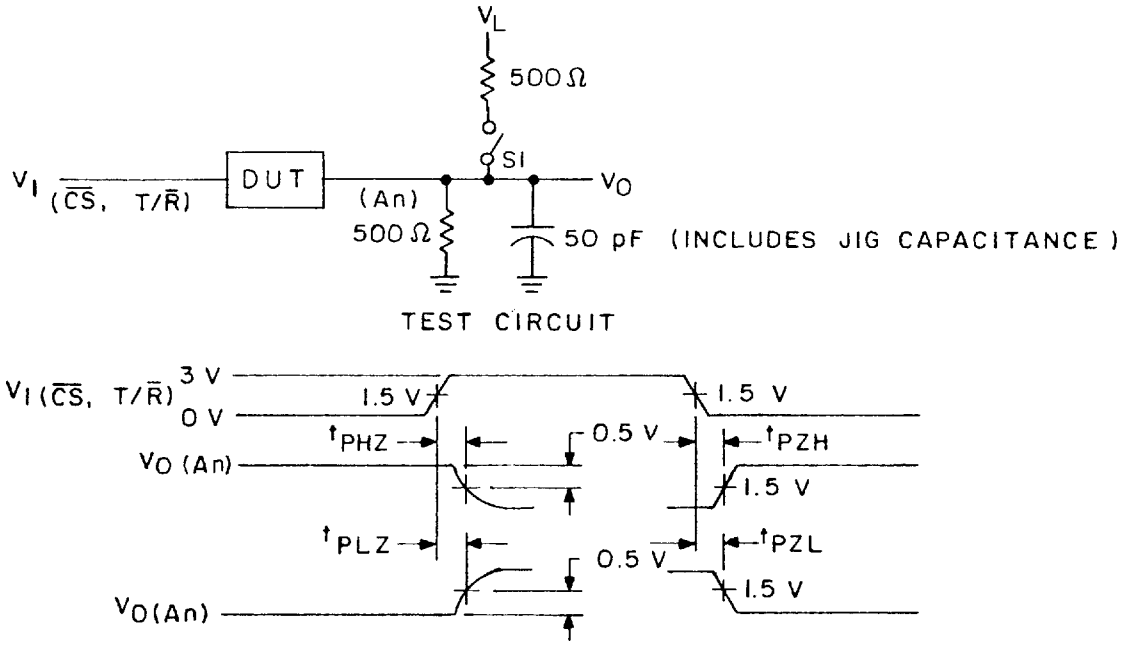

TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTE: FOR $V_I$(Bn), $t_r = t_f \leq$ 10ns FROM 10% TO 90%

FIGURE 4. Receiver delay waveforms.



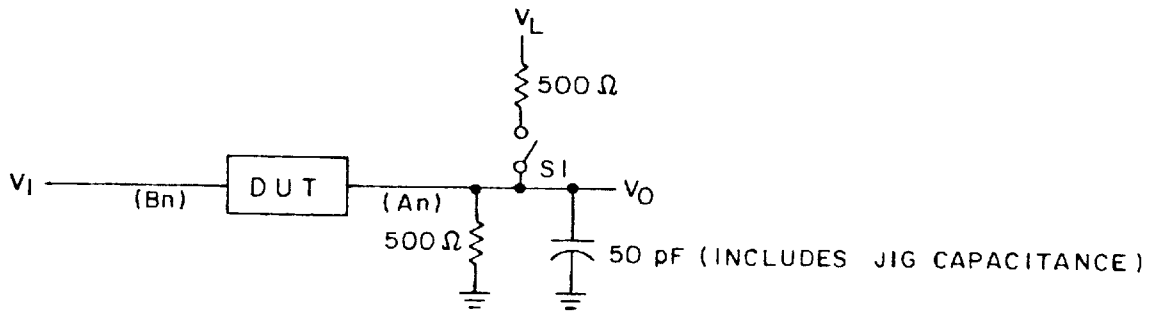

TEST CIRCUIT



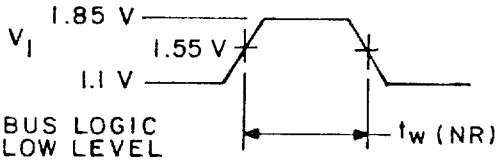

VOLTAGE WAVEFORMS

NOTE: FOR $V_I$ ($\overline{CS}$, T/$\overline{R}$), $t_r = t_f \leq 5$ ns FROM 10% TO 90%.

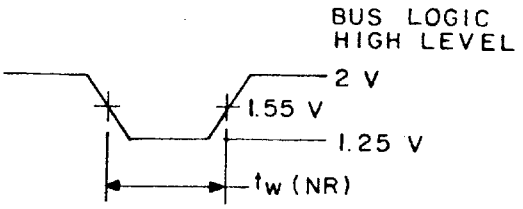
FIGURE 5. Delay waveforms from $\overline{CS}$ or T/$\overline{R}$ to An.




TEST CIRCUIT




$t_w$ IS INCREASED UNTIL THE OUTPUT VOLTAGE FALL JUST REACHES 2.0 V.




$t_w$ IS INCREASED UNTIL THE OUTPUT VOLTAGE RISE JUST REACHES 0.8 V.

VOLTAGE WAVEFORMS

NOTE: FOR $V_I$ (Bn), $t_r = t_f \leq 2$ ns FROM 10% TO 90%.

FIGURE 6. Receiver noise immunity waveforms.

3.2.7 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | - - - |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

*PDA applies to subgroup 1.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.