Preliminary

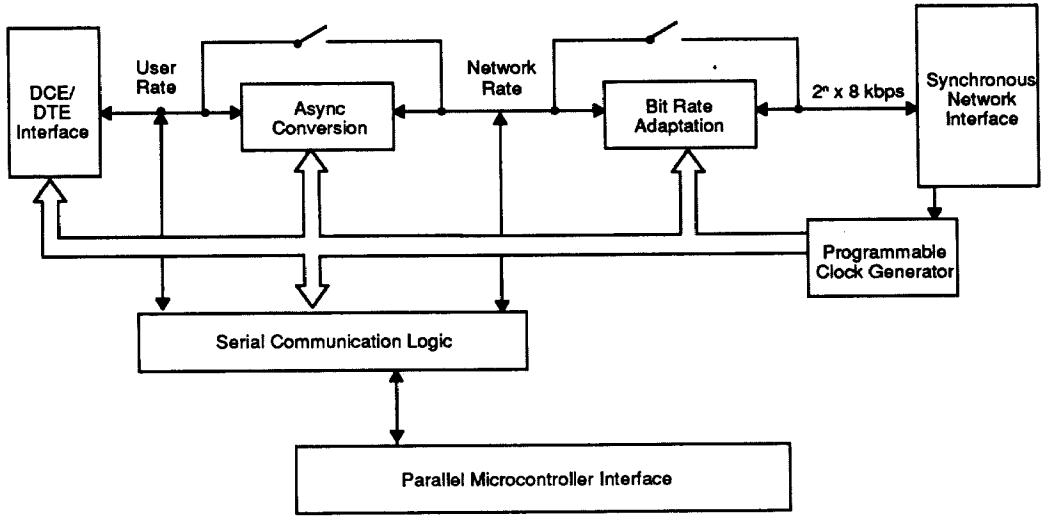
Am2110
ISDN Terminal Adapter Circuit (ITAC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Universal adapter for ISDN R reference point
- Support of async and sync interfaces: X.21, X.21 bis, V.24, RS232C
- Programmable speeds from 300 bps to 64 kbps
- Bit rate adaptation according to X.30, V.110, ECMA.102, V.120 and DMI
- Programmable time slots and subchannels for intermediate rates
- Automatic calling/answering with on-chip controllers
- In-band parameter exchange support
- Parallel 8-bit microcontroller interface
- DMA support
- Single +5 V supply, low power CMOS technology

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The ISDN Terminal Adapter Circuit (ITAC) is a monolithic, full custom circuit for interfacing standard terminals and PCs to a circuit switched data network or an ISDN. It may be programmed to perform bit rate adaptation for 64 kbps clear channels according to the newest rate adaptation protocols. The on-chip communication controllers handle signaling between data equipment and the network, effectively replacing the "smart modem" of the PSTN. The features of the ITAC make it suitable for use in advanced networking applications that require flow control, in-band parameter exchange and interworking.

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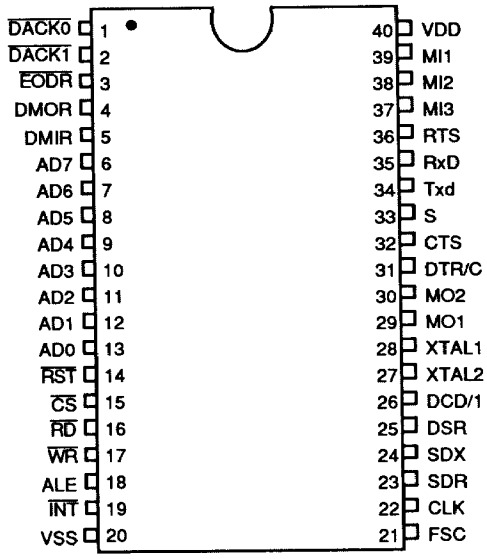
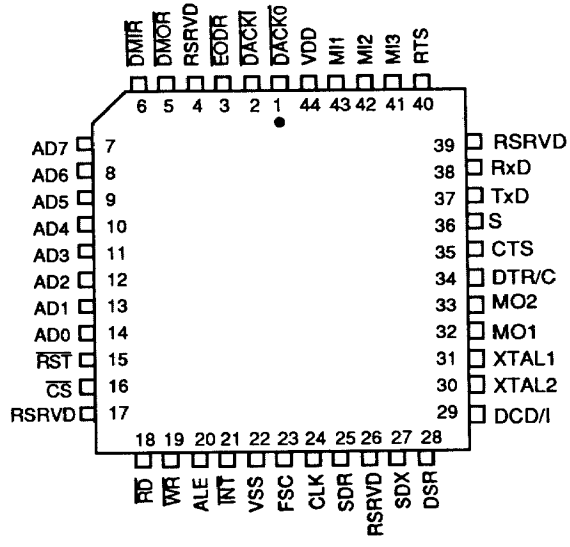
CONNECTION DIAGRAMS
Top View

40-Pin DIP



44-Pin PLCC



Note: Pin 1 is marked for orientation.

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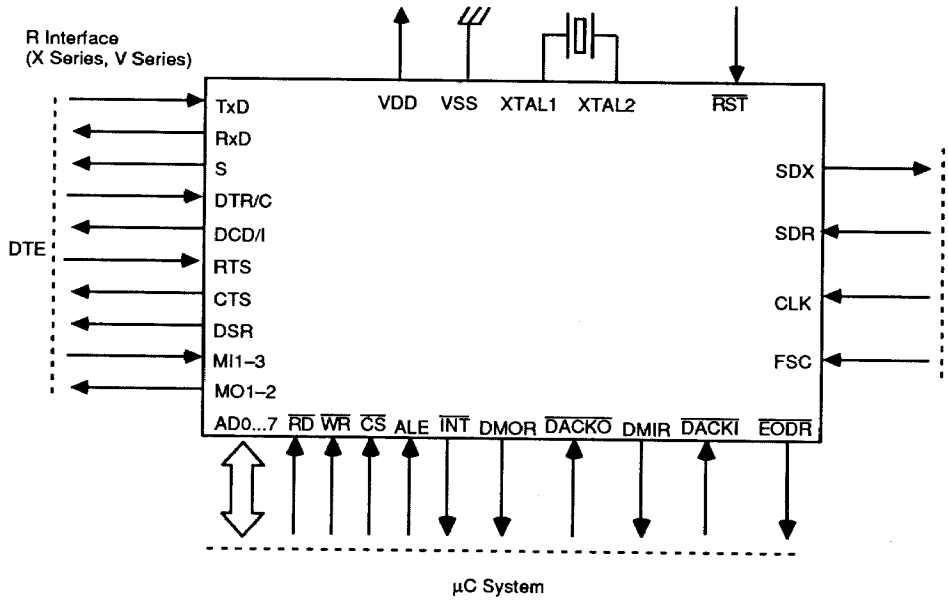
LOGIC SYMBOL



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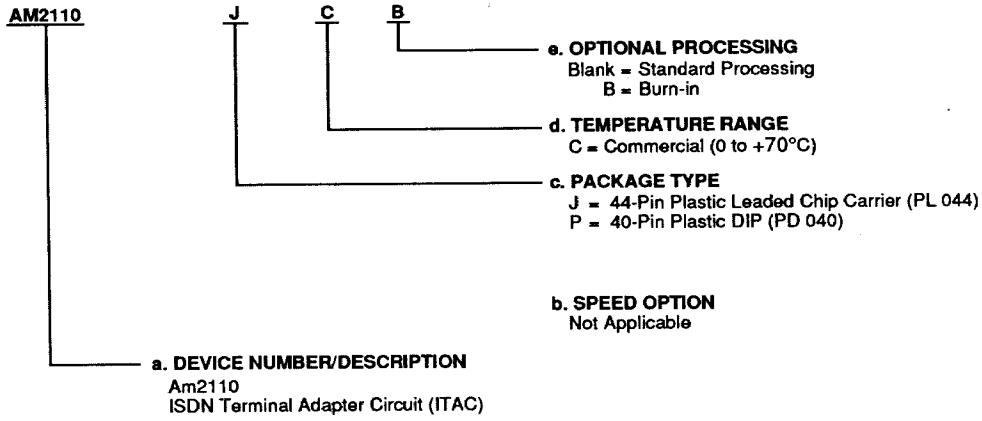
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2110	JC, JCB, PC, PCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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PIN DESCRIPTION

DCE Mode

AD0–AD7
Address/Data Bus (Input/Output)

ALE
Address Latch Enable (Input)

CLK
Clock (Input)
Data clock for the synchronous network interface.

$\overline{CS}$
Chip Select (Input)

CTS
Clear to Send (Output)
(106) V.24 interchange circuit.

$\overline{DACKI}$
DMA Input Acknowledge (Input)

$\overline{DACKO}$
DMA Output Acknowledge (Input)

DCD/I
Data Channel Received Line Signal Detector (Output)
Carrier Detect (109) V.24/Indicate X.21 interchange circuit.

DMIR
DMA Input Request (Output)

DMOR
DMA Output Request (Output)

DSR
Data Set Ready (Output)
(107) V.24 interchange circuit.

DTR/C
Data Terminal Ready (Input)
(108) V.24/control X.21 interchange circuit.

$\overline{EODR}$
End of DMA Output Request (Output)

FSC
Frame Sync (Input)
8 kHz.

$\overline{INT}$
Interrupt (Open Drain)
Open-drain interrupt request.

MI1–3
Multifunctional (Input)
V.24 interchange circuit.

MO1–2
Multifunctional (Output)
V.24 interchange circuit.

$\overline{RD}$
Read Enable (Input)

$\overline{RST}$
Reset (Input)

RTS
Request to Send

RxD
Receive Data to DTE (Output)
Data is clocked off by the ITAC on the falling edge of "S" on synchronous DT interfaces.

S
(Output)
Bit element timing for synchronous DTE.

SDR
Synchronous Data Receive (Input)
Data are input on the falling edge of CLK.

SDX
Synchronous Data Transmit (Output)
Data are on the rising edge of CLK.

TxD
Transmit Data from DTE (Input)
Data is latched by the ITAC on the rising edge of "S" on synchronous DTE interfaces.

$\overline{WR}$
Write Enable (Input)

XTAL1
Connection for External Crystal (Input)
Input for external clock generator.

XTAL2
Connection for External Crystal (Output)
N.C. when clock generator is used.

VDD
(Input)
Power supply, ±5 V ±5%.

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VSS
(Input)
Power supply, ground.

DTE Mode

DCD

DSR
Data Set Ready (Input)
(107) V.24 interchange circuit.

DTR
Data Terminal Ready (Output)
(108) V.24 interchange circuit.

MO3
Multifunctional (Output)
V.24 interchange circuit.

RTS
Request to Send (Output)
(105) V.24 interchange circuit.

RxD
Receive Data from DCE (Input)

TxD
Transmit Data to DCE (Output)

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PIN NAMES

Note: Pin names refer to DCE mode.

AD0–7	I/O	Address/Data bus
ALE	I	Address Latch Enable
CLK	I	Network Clock
$\overline{CS}$	I	Chip Select
CTS	O	Clear to Send
$\overline{DACKI}$	I	DMA Input Acknowledge
$\overline{DACKO}$	I	DMA Output Acknowledge
DCD/I	O	Carrier Detect/Indicate
DMIR	O	DMA Input Request
DMOR	O	DMA Output Request
DSR	O	Data Set Ready
DTR/C	I	Data Terminal Ready/Control
$\overline{EODR}$	O	End of DMA Output Request
FSC	I	8 kHz Frame Sync Clock
$\overline{INT}$	O	Interrupt request
MI1–3	I	Multifunctional Inputs
MO1–2	O	Multifunctional Outputs
$\overline{RD}$	I	Read Enable
$\overline{RST}$	I	Reset
RTS	I	Request to Send
RxD	O	Receive Data
S	O	Bit Clock
SDR	I	Synchronous Data Receive
SDX	O	Synchronous Data Transmit
TxD	I	Transmit Data
$\overline{WR}$	I	Write Enable
XTAL1,2	I/O	Connections for 10.752 MHz crystal or external oscillator

System Integration

Terminal Adapter for ISDN Basic Access

A typical implementation of an ISDN basic access for a conventional X- or V-series terminal using the ITAC is shown in Figure 1.

The ITAC can be connected via a serial synchronous interface to an ISDN basic access transceiver/LAPD controller (in this case, the ISDN Subscriber Access Controller for the S interface, ISAC-S). These two devices, together with the terminal controller, convert V- and X-series interface characteristics to the functional and procedural interface characteristics required by an ISDN at reference point S.

The ITAC subchannel multiplexing feature allows sharing a single 64 kbps bearer channel by up to eight independent terminals. This is illustrated in Figure 2.

Figure 2 also illustrates how the ISDN Subscriber Access Controller for the U interface (ISAC-P) can be used, instead of the ISAC-S, in U interface applications.

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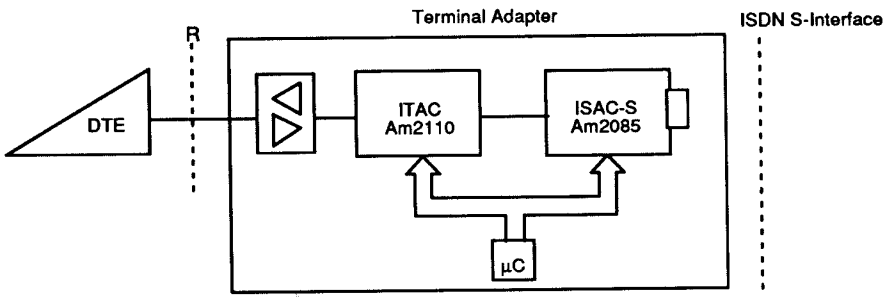
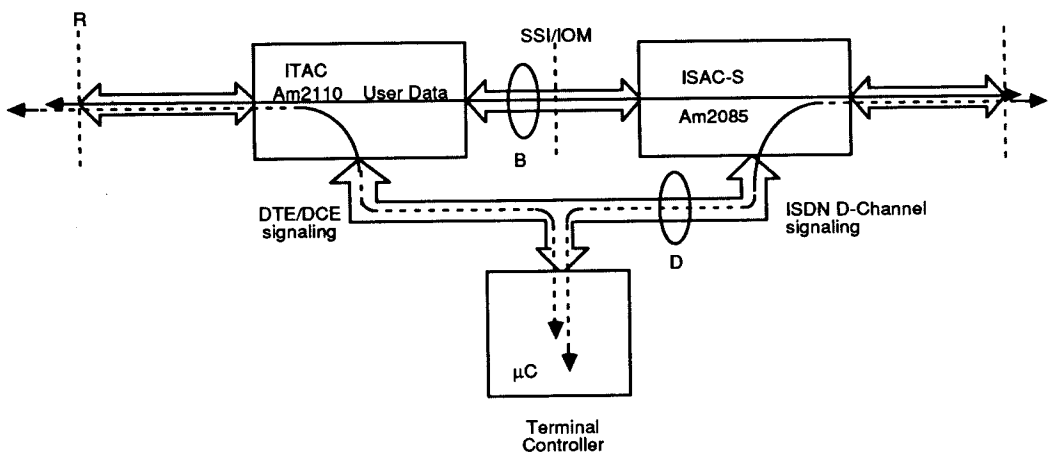


(a)



(b)

Figure 1. **(a) Universal TA for the ISDN basic access R reference point (bit stuffing or flag stuffing bit rate adaptation)**

(b) Data paths for bit rate adapation according to V.110/X.30

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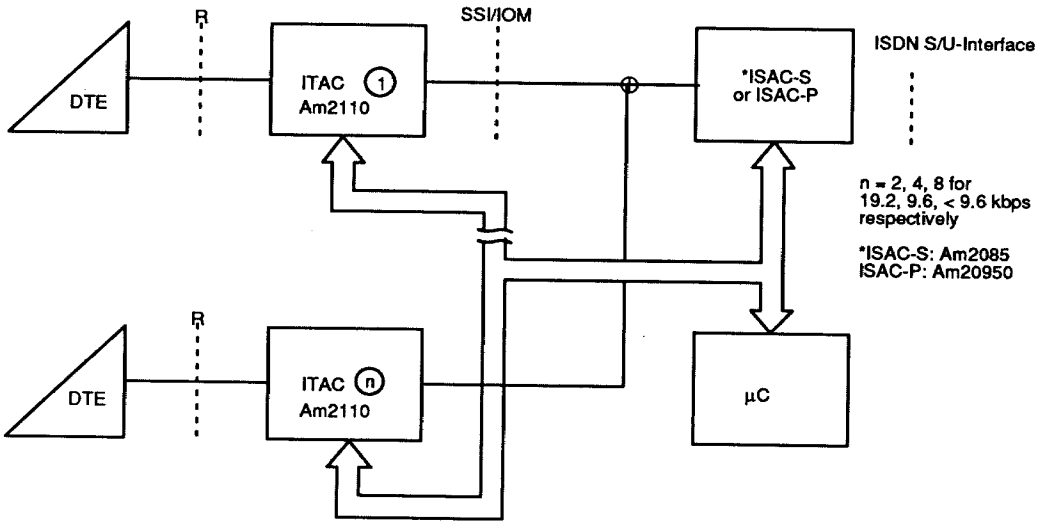

Figure 2. Sharing of bearer channels among several independent DTEs (up to 16 DTEs for two B channels).

PC Adapter Board

The ITAC may be used to enable communication between a personal computer and conventional asynchronous or synchronous terminals. In this case, the data is sent and received over the parallel microcontroller interface, via the integrated communication FIFOs, or using DMA. Depending on the bit rate adaptation scheme used, the ITAC performs the appropriate formatting functions (V.110, V.120 or DMI, or V.110 embedded HDLC).

Other Applications

The synchronous network interface of the ITAC is compatible to most PCM systems using programmable time slots. Consequently, the circuit in association with all IOM-compatible circuits is ideally suited for applications on PABX line cards and concentrators/multiplexers.

Other applications of the ITAC include: host computer multiple line communication couplers, primary access/DMI peripheral boards, and Interworking Units (IWUs) between ISDN and analog PSTN.

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FUNCTIONAL DESCRIPTION

General Functions and Device Architecture

A simplified block diagram of the ITAC is on page 1.

Data conversion is implemented by two main blocks. First, user data is transformed to a data rate synchronous to the ISDN, called the Network rate, by an Async/Sync converter.

The Bit Rate Adaption block converts the Network rate into a rate which can be transmitted to the ISDN, $2^n \times 8$ kbps, n = 0,1,2,3.

For synchronous switched-through DTE data, the Asynch/Synch Converter is not used, and the Network rate is identical to the User rate. Otherwise the Network rate is defined independent of the User rate.

Through the Serial Communication Logic, the microcontroller can access the receive and transmit data.

An architectural overview of the ITAC is shown in Figure 3.

The Programmable Clock Generator provides timing synchronized by the network master clock, to the different functional blocks.

The Async/Sync Converter (ASC) block contains the stop bit and break signal manipulations necessary for asynchronous DCE/DTE interfaces according to V.22. The Intermediate Rate Conversion (IRC) and the Bearer Rate Conversion (BRC) blocks correspond to the RA1 and RA2 stages of X.30 (I.461) and V.110 (I.463) CCITT recommendations.

The Data Multiplexer switches the data between the DCE/DTE interface, the Intermediate Rate Conversion block and the Serial Communication Logic. The latter consists of a Universal Synchronous/Asynchronous-receiver and transmitter section and of an HDLC receiver and transmitter section, each with an integrated FIFO. The flexible FIFOs with DMA capability are optimized for fast parallel access to the control and user data streams.

The ITAC performs recognition of local and remote DTE/DCE states via the Status Detect Logic.

The microcontroller interface consists of registers necessary to configure the circuit and to monitor state changes.

Finally, testing capabilities are provided, including test loops for data from local and from remote data terminals.

Operating Modes

The operating mode of the ITAC depends on the user interface type and on the bit rate adaptation protocol.

In the case of a synchronous DTE, either an X.21 or an X.21 bis (synchronous V.24) may be selected. Interworking between X.21 and X.21 bis DTEs is also provided for.

In the case of an asynchronous DCE/DTE interface, the ITAC may be used as a DCE or a DTE.

Transparent Mode

This mode is applied in the data transfer phase of a data call where only layer 1 conversion is required.

In this mode, the microcontroller need only monitor the changes of call status through the Status Detect Logic and/or through generated interrupts. All conversion functions are implemented by the ITAC and are transparent to the microcontroller (Figure 4).

The selectable User rates are summarized in Table 1, for both synchronous and asynchronous DCE/DTE interfaces.

For each of the async rates, the user is able to select the character length, the number of Stop elements, as well as the tolerance range for the handling of DTE overspeed.

Table 1. User Data Rates

User rate, bps	Async data	Sync data
300	X	
600	X	X
1200	X	X
2400	X	X
4800	X	X
9600	X	X
19200	X	X
38400	X	X
48000		X
56000		X
64000		X

As the name of this operation mode implies, the user data is handled transparently; in particular, no parity checking or generation is performed by the ITAC.

Non-transparent Mode

In the non-transparent mode, the Serial Communication Logic is involved in the reception or the transmission of data or control information. This mode of operation is used in particular in the setup phase of a data call, in the simulation of a Hayes Smartmodem command state, for In-band Parameter Exchange and in Host or Personal Computer applications (Figure 5).

It is realized in practice by switching the USART receiver or the HDLC receiver and/or the USART transmitter or the HDLC transmitter into the data path between the DCE/DTE interface and the network interface.

In this mode, higher-level functions are optionally performed by the ITAC on the user data, for example, parity generation and checking.

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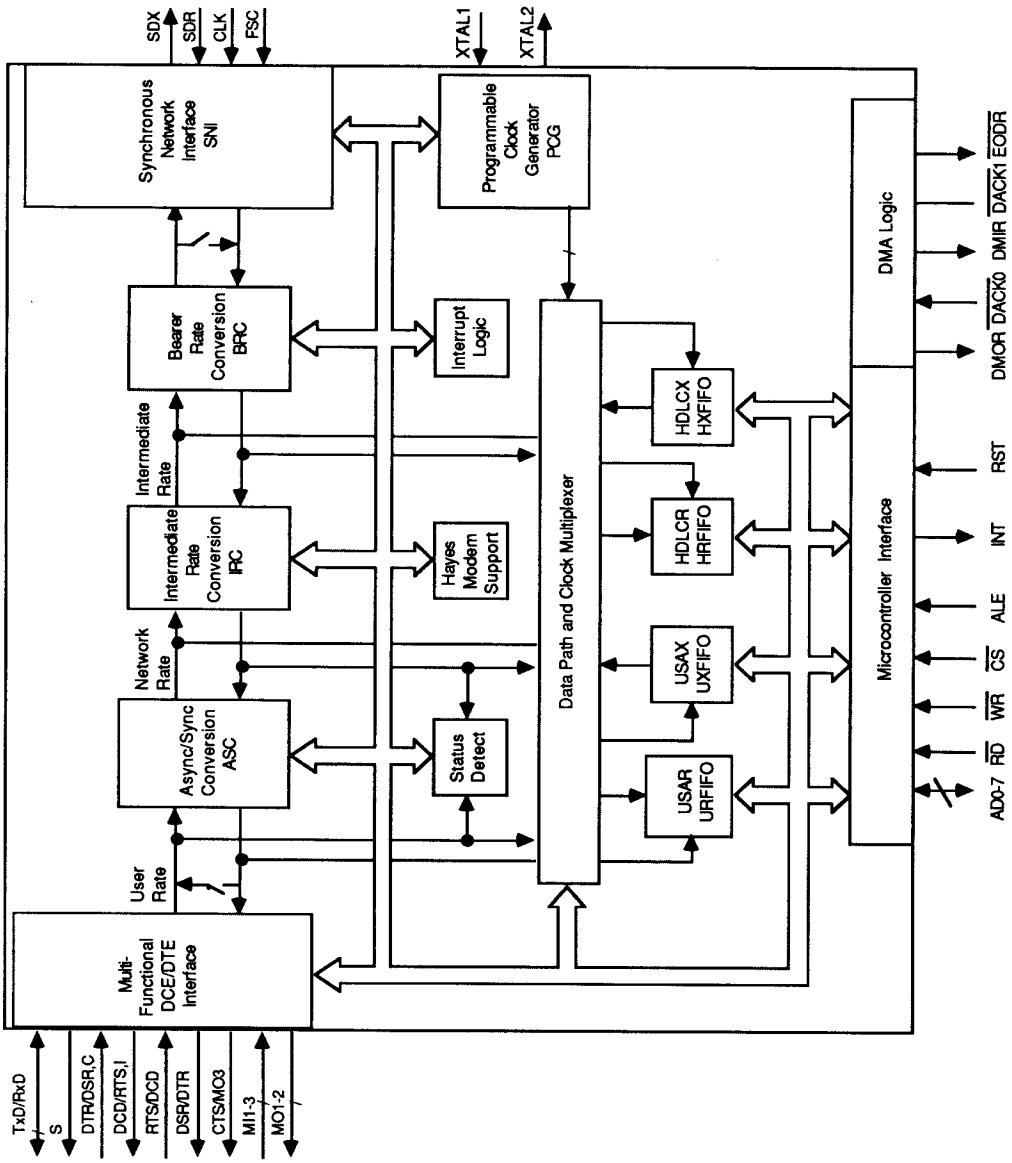

Figure 3. General Architecture of ITAC

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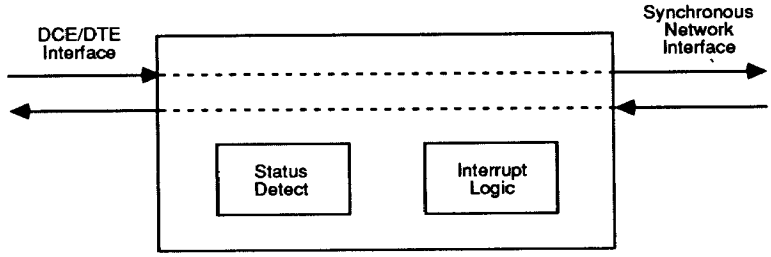

Figure 4. Transparent Mode

Interfaces

The ITAC supports interfaces:

- to a microcontroller system
- to synchronous/asynchronous DTEs
- to the network

Parallel Microcontroller Interface

The ITAC is programmable over an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 18 lines and is directly compatible with processors of the multiplexed address/data bus type (Table 2).

Table 2. Microcontroller Interface Signals for ITA

Symbol	Type	Name and Function
AD0–AD7	I/O	Address-Data bus. The multiplexed address/data bus transfers data and commands between the µC system and the ITAC.
$\overline{CS}$	I	Chip Select. A low on this signal selects the ITAC for a read/write operation.
$\overline{WR}$	I	Write. This signal indicates a write operation.
$\overline{RD}$	I	Read. This signal indicates a read operation.
$\overline{INT}$	OD	Interrupt Request. The signal is activated when the ITAC requests an interrupt. It is an open drain output.
ALE	I	Address Latch Enable. A high on this line indicates an address on the external address/data bus.
DMOR	O	DMA Output Request. The signal is activated when the ITAC wishes to output a byte of data via DMA.
DMIR	O	DMA Input Request. The signal is activated when the ITAC wishes to receive a byte of data via DMA.
$\overline{DACK0}$	I	DMA Output Acknowledge. DMA Controller's response to DMOR.
$\overline{DACK1}$	I	DMA Input Acknowledge. DMA Controller's response to DMIR.
$\overline{EODR}$	O	End-of-DMA output request for HDLC receiver.

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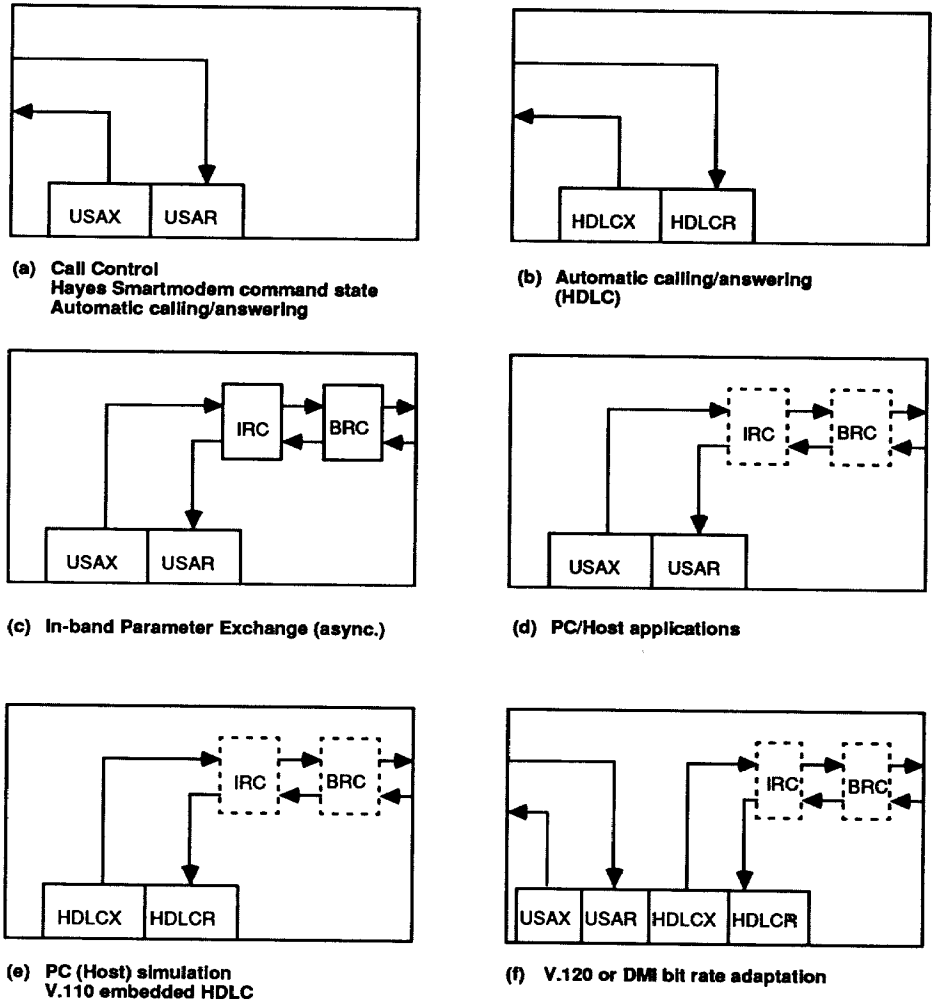

(a) Call Control
Hayes Smartmodem command state
Automatic calling/answering

(b) Automatic calling/answering
(HDLC)

(c) In-band Parameter Exchange (async.)

(d) PC/Host applications

(e) PC (Host) simulation
V.110 embedded HDLC

(f) V.120 or DMI bit rate adaptation

Figure 5. Non-transparent Modes of the ITAC

DCE/DTE Interface

The DCE/DTE interface of the ITAC consists of six input and seven output lines. In addition to common X.21 and V.24 interface interchange circuits, the circuit supports three programmable, multifunctional inputs and two programmable, multifunctional outputs. The assignment of the DCE/DTE interchange circuits are as shown in Table 3.

The bits received and transmitted on RxD and TxD are such that logical "1" = high voltage and logical "0" = low voltage.

The control signals are such that state OFF = high voltage and state ON = low voltage.

For synchronous DTE interfaces, data on TxD are latched by the ITAC on the rising edges of S, and data on RxD are clocked off by the ITAC on the falling edges of S.

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Table 3. ITAC DCE/DTE Interface Signals

Pin DCE mode	Pin DTE mode	Mnemonic	Description	X.21	V.24 / X.21 bis
I	O	TxD	Transmit Data	T	103
O	I	RxD	Receive Data	R	104
O		S	Signal Element Timing	S	114/115 (sync only)
I	O	DTR/C	Data Terminal Ready/Control	C	108
O	I	DCD/I	Data Carrier Detect/Indicate	I	109
I	O	RTS	Request to Send	–	105
O	I	CTS	Clear to Send	–	106
O	I	DSR	Data Set Ready	–	107
I	I	MI1–3	Multifunctional Inputs		programmable
O	O	MO1–2	Multifunctional Outputs		programmable

Synchronous Network Interface

The Synchronous Network Interface (SNI) consists of four physical connections (Figure 7). Two lines are for the transmission of data, one for each direction. The other two lines are for the bit and frame clocks.

The bit rate on the Serial Data Receive SDR and Serial Data Transmit SDX lines is equal to the bit clock frequency (CLK). Data is output on SDX on the rising edges of CLK and latched from SDR on the falling edges. The particular channel where data is to be received and transmitted by the ITAC is programmable. The position of the time channel is relative to the Frame Sync signal (FSC) which marks the beginning of the frame. The repetition rate of FSC is 8 kHz. The maximum bit rate is 4.096 Mbps, corresponding to a maximum of 512 bits per frame.

Programmable Clock Generator

The Programmable Clock Generator (PCG) consists of DPLL circuitry synchronized by the network reference clock (FSC) and driven by an external crystal of frequency 10.752 MHz ±100 ppm or by an external oscillator. It delivers the clocks used by the different functional blocks:

- Bit clock for the Intermediate Rate Converter: 8, 16, 32 or 64 kHz
- Frame clock for the Intermediate Rate Converter
- Network rate clock: 600 Hz to 64 kHz
- User rate clock: 600 Hz to 64 kHz
- Transmit async clock: 300 x 2^n, (n = 0,1,2,3,4,5,6,7) synchronized by the leading edge of a start bit.
- Receive async clock: 300 x 2^n Hz.

The clocks are synchronized upon the timing received from the Synchronous Network Interface, when provided. When the SNI timing is not provided, the clocks are running free if not disabled by the microcontroller. Upon application of network clocking, synchronization of the clocks is automatically performed in such a way that any phase jump does not exceed 1 of the nominal synchronous clock period.

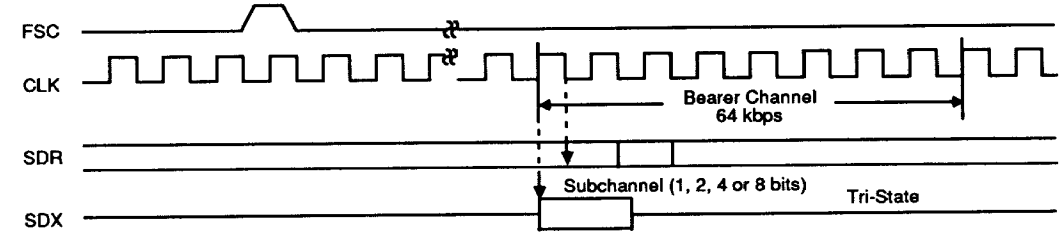

Figure 6. Timing of the Synchronous Network Interface

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Table 4. Network Rate-to-Intermediate Rate Conversion Summary

Network rate bps	Intermediate rate (kbps)	Frame length (bit)	User data bit repetition factor
600	8	4 x 80	8
1200	8	2 x 80	4
2400	8	80	2
4800	8	80	1
9600	16	80	1
19200	32	80	1
38400	64	80	1
48000	64	32	1
56000	64	8/64	1
64000	64	transparent	1

Async/Sync Converter

The ASC transforms the stream of Start/Stop formatted characters into a synchronous bit stream defined by 2^n times 600 bps, and vice versa.

The possible asynchronous rates are: 300, 600, 1200, 2400, 4800, 9600, 19200 and 38400 bps.

Functions in the Transmit Direction

The async-to-sync converter transforms the asynchronous characters (User rate) into a selected synchronous Network rate. The Network rate is equal to 2^n x nominal User rate (n = 0 to 7).

- Framing upon the incoming characters from local DTE/DCE. (Baud rate factor 16)
- Handling of underspeed and overspeed:

  Transmitted characters are padded with Stop elements as often as necessary to match the Network rate. In case of overspeed, Stop elements are deleted within the limits of the selected tolerance range.
- Recognition and generation of break signals:

  A break signal is generated in accordance with V.110 when at least M-bits of Start polarity at User rate are detected.

Note: M denotes the number of bits per character in the selected format including Start and Stop bits.

Functions in the Receive Direction

The sync-to-async converter transforms the synchronous bit stream (Network rate) into an asynchronous User rate. The latter is equal to 2^n x Network rate, (n = 0 to 6) for Network rate greater than 600 bps. It is either 300 or 600 bps for Network rate equal to 600 bps.

- Framing upon the incoming characters from the Intermediate Rate Converter
- Missing Stop elements:

  Missing Stop elements are restored. If necessary, the length of Stop elements are reduced according to the selected tolerance range, to allow for overspeed on the transmitting side.
- Break signal:

  The 2M + 3 or more bits of Start polarity received from the transmitting side are output to the DCE/DTE interface.

Intermediate Rate Converter

The IRC converts

- The synchronous net data originating from the DCE/DTE interface, the Async-to-Sync Converter or the Serial Communication Logic into an intermediate rate equal to 2^nx 8 kbps.
- The intermediate rate into synchronous net data sent to the DCE/DTE interface, the Sync-to-Async Converter or the Serial Communication Logic.

  The intermediate rate and the frame are implicitly determined by the Network rate, as shown in Table 4.

  For rates up to 38400 bps, the frame is based on the 80-bit frame structure shown in Table 5.

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Table 5. 80-bit Frame Structure (X.30/V.110)

Bit number	Bit position 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1	D2	D3	D4	D5	D6	Si
2	1	D7	D8	D9	D10	D11	D12	X
3	1	D13	D14	D15	D16	D17	D18	Sj
4	1	D19	D20	D21	D22	D23	D24	Sk
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D25	D26	D27	D28	D29	D30	Sl
7	1	D31	D32	D33	D34	D35	D36	X
8	1	D37	D38	D39	D40	D41	D42	Sm
9	1	D43	D44	D45	D46	D47	D48	Sn

The adaptation of 48 and 56 kbps rates is based on a 32- and a 64-bit frame, respectively, according to V.110.

Functions In the Receive Direction

- Frame recovery

  The frame alignment pattern is composed of eight zeros and nine ones. In addition, bit E7 is used for superframe alignment in the 600 bps case.

  The receiver indicates its state of synchronism to the microcontroller via a maskable interrupt status.
- Extraction of D bits
- Extraction of status bits

  These bits are accessible to the microcontroller. Additionally, they can be directly mapped on to the DCE/DTE interface in synchronism with the D-bits according to X.30 or V.110. If an X.21 interface is selected, the SP, SQ and SR are mapped on I interchange circuit. Otherwise, SA (S1,S3, S6, S8) and SB (S4, S9) are mapped as shown in Figure 7.
- Extraction of E and X bits

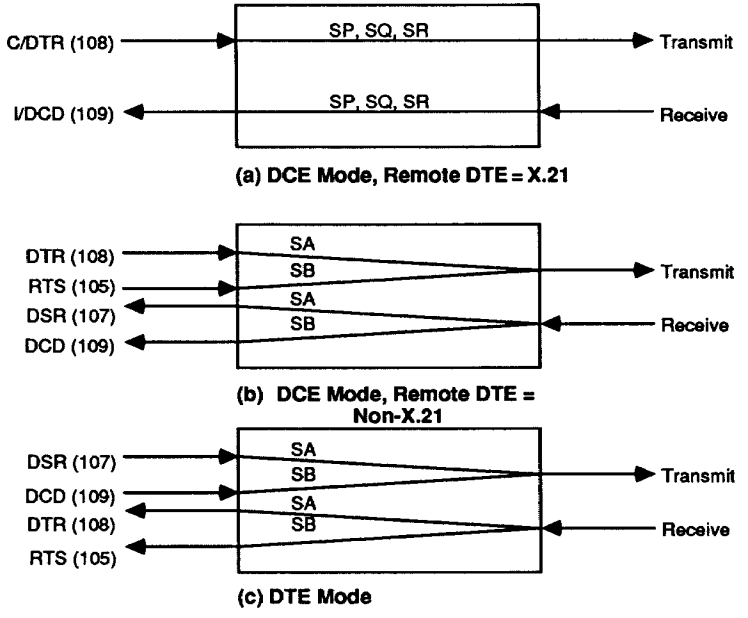

Figure 7. Status Bit Mapping Summary

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These bits are accessible to the microcontroller. A change is reported via a maskable interrupt status.

Functions in the Transmit Direction

- Frame setup
- Insertion of D-bits
- Insertion of status bits

  These bits either originate from the microcontroller or they convey the state of DTE interchange circuits at specific sampling points according to recommendation X.30 or V.110. In the latter case, if an X.21 interface is programmed, the SP, SQ and SR bits reflect the state of C interchange circuit. Otherwise, SA (S1, S3, S6, S8) and SB (S4, S9) are mapped as shown in Figure NO TAG.
- Insertion of E and X bits.

  These bits originate from the microcontroller.

Bearer Rate Converter

The BRC takes the intermediate rate data to groups of 1, 2 or 4 bits, to be sent as a subchannel in a 64 kbps bearer channel, and vice versa. The BRC is not used in the case of programmed network rate greater than or equal to 38400 bps.

Status Detect Logic

The ITAC performs detection of local DCE/DTE interchange circuit states for V.24 interfaces. The local DCE/DTE states monitored by the Status Detect Logic are DTR (108), RTS (105) and MI1–3 (DSR, DCD and MI1–3 in DTE mode). Changes of state are reported to the Microcontroller Interface Logic by a maskable interrupt status.

In the case of a local X.21 DTE, combined local (TxD, C) status recognition is performed by the Status Detect Logic. Valid X.21 states are reported to the Microcontroller Interface Logic after 16 bit times over a status bit. The valid states are shown in Table 6.

When the local DTE is synchronous and the local DTE or the remote DTE is of the X.21 type, combined remote (TxD, C) status recognition is performed as also shown in Table 6.

Table 6. Valid X.21 States

Local DTE status (TxD, C) local	Remote DTE status (TxD, C) remote
(1, ON)	(1, ON)
(0, ON)	
(1, OFF)	(1, OFF)
(0, OFF)	(0, OFF)
(0011, OFF)	(0011, OFF)
(01, OFF)	
(00001111, OFF)	

Hayes Protocol Support

The Hayes (Smartmodem) Protocol is supported by the integrated USART plus additional hardware.

In the "on-line mode," the ITAC behaves as a conventional modem, treating the data transparently as explained in the *Transparent Mode* section on page 10. To implement the Hayes modem command mode, the USART with its associated FIFOs is switched into the data path for the exchange of control character sequences with the local DTE.

In the Hayes Smartmodem protocol, the return to the command mode from the on-line mode is possible without tearing down the data call. The return is effected after the reception of escape characters.

The ITAC implements this procedure by recognizing a local character(s) from the local DTE. In addition, the "guard time" specified in the Hayes protocol can be supervised via a status bit.

Flow Control Support

A flow control option, for use with TAs supporting asynchronous DTEs, is offered by the ITAC. Flow control allows the connection of asynchronous DTEs operating at different user data rates by reducing the character output of the faster to that of the slower DTE.

The connection of two DTEs operating at unequal rates requires that the selected Network rate is different from the User rate for one of the ITACs.

If the Network rate is lower than the User rate, external buffering of the characters received from the local DTE is implemented by switching the USART in the transmit data path. The receive data path requires no buffering, and the speed conversion is automatically handled by the ITAC (Figure 8a).

If, on the other hand, the User rate is lower than the Network rate, external buffering of the characters received from the network is implemented by switching the USART in the receive data path. The transmit data path is transparent (Figure 8b).

For use in a terminal adapter connected to the faster DTE (Figure 9a and b), the ITAC supports in-band and out-band local flow control procedures. In-band flow control is implemented by outputting a special XON/XOFF character to the local DTE. The character is inserted in the input data stream upon a microcontroller command without loss of receive characters. Out-band flow control is implemented by the microcontroller directly controlling an output line, CTS.

Remote flow control is required in the case where the Network rate of one of the terminal adapters is higher than the selected User rate (Figure 9b). The X-bit is used to carry flow control information. The microcontroller is able to directly set the X-bit according to the

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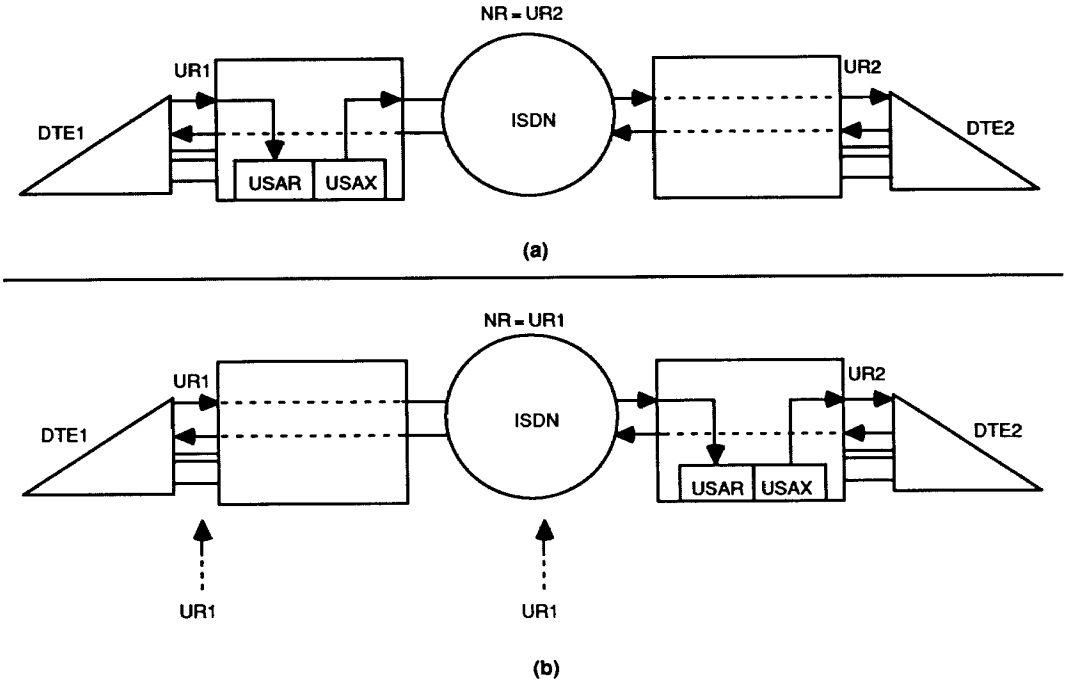

Figure 8. Local and Remote Flow Control Situations. It is assumed that DTE1 is always the faster DTE.

state of the character buffer on the transmitting side. On the receiving side, the ITAC reports any changes in the X-bit by a maskable interrupt.

For the case where a DTE itself transmits flow control characters to slow down the remote DTE, the ITAC provides for recognition and inhibiting of two programmable characters from the DCE/DTE interface. Finally, to support the connection of terminal adapters employing in-band remote flow control, the ITAC is also able to recognize two programmable characters from the network.

Serial Communication Logic

The Serial Communication Logic consists of two independent controllers, the USART and the HDLC controller, with their associated FIFOs.

FIFO Operation

The length of each of the Receive FIFOs (RFIFO) and Transmit FIFOs (XFIFO) is nine characters/bytes.

The first bit of a character/byte received or transmitted is the rightmost stored bit or LSB. Characters are right-justified.

Interrupt status bits indicate the state of RFIFO and XFIFO. Data can be loaded and fetched by the microcontroller, or using DMA. However, even in the DMA case the FIFOs are used. This gives a worst case reaction time of 1 ms in both non-DMA and DMA operation (worst case of 64 kbps), to maintain a constant data throughput.

In the HDLC case several frames can be simultaneously stored in the RFIFO and the XFIFO.

USART

In its asynchronous mode, the USART has the following programmable settings (Table 7).

Table 7. Programmable Settings of the USART

Parameter	Values
Character length excluding possible parity bit	5, 6, 7, 8
Parity check/generation	yes, no
Parity type	even, odd, 0,1
Number of stop bits	1, 2

When enabled, the receiver searches for valid character frames (Start + character + Stop) and stores the charac-

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ters in the RFIFO as they arrive, stripping off the start and stop bit(s).

A possible parity bit is stored in the RFIFO as the bit immediately on the left of the MSB. Thus the parity is transferred to the microprocessor, an exception being: number of character data bits = 8 plus parity.

In the case where a parity error is detected (and parity check/generation is programmed), this fact is indicated with a status bit at the time the microcontroller reads the corresponding character from the RFIFO. Similarly, a framing error status is generated at the time when the illegal character is read from the RFIFO.

A break signal is received if a row of null bits of length > M − 1 is detected from the DCE/DTE interface, or of length > 2M − 2 is detected from the network. A break signal is reported by an interrupt status.

When the asynchronous transmitter is enabled, the transmission of any characters entered in the XFIFO is immediately started. Characters are separated by the selected number of Stop bits. Characters may be entered in the XFIFO even if the async transmitter is not enabled. When the XFIFO runs empty, continuous "1" is transmitted until a new character is available.

Break signals of any length may be transmitted.

In the synchronous mode of the USART, the characters received and transmitted have a length of eight bits, including possible parity.

The sync receiver has two modes of operation: Transparent mode and Hunt mode. In the Transparent mode the receiver, when enabled, immediately starts storing received characters without regard for octet synchronization. In the Hunt mode, the receiver searches for one (monosync) or two (bisync) programmable characters before starting to store the received characters. The Hunt mode and the Transparent mode may be entered at any time by issuing the corresponding command.

If desired, a programmable parity check is performed on the receive characters, as in the asynchronous case.

The operation of the transmitter is similar to the operation in the async mode. However, no parity is generated. Further, in the synchronous mode, the last character is repeatedly transmitted when the XFIFO runs empty, as opposed to constant "1" in the async mode.

HDLC Controller

The functions performed by the HDLC receiver are:

- flag detection
- zero deletion
- CRC checking (generator polynomial: $x16 + x12 + x5 + 1$)
- check for abort
- check for idle

When enabled, the receiver enters a hunt phase and remains in the hunt phase until it detects a valid opening flag.

Once a flag is recognized by the receiver, not followed by another flag or by an abort or idle sequence, all the subsequent eight-bit bytes are stored in the RFIFO, up to and excluding the Frame Check Sequence (FCS) that immediately precedes the closing flag. When the closing flag is detected, a "receive status byte" is appended to the stored frame. This status byte contains status information pertaining to the received frame: frame aborted yes/no, CRC error yes/no data overflow yes/no, and number of significant bits in the last receive byte.

As the receive status byte is read, an interrupt status is generated to indicate the end of the receive frame.

When the beginning of a receive frame is detected and the RFIFO is full, the frame will be completely lost and an interrupt status is generated.

The functions performed by the HDLC transmitter are:

- flag generation
- zero insertion
- CRC generation
- abort sequence generation
- interframe time fill generation

When the transmitter is enabled, the transmission of any bytes entered in the XFIFO is immediately started, preceded by an opening flag.

To indicate the end of frame, the microcontroller sets a control bit after having entered the last data byte of that frame in the XFIFO. Every write operation of the bit serves as a frame delimiter.

As long as frames are entered in the XFIFO, they are transmitted in the order in which they were entered.

When no data is available in the XFIFO and the transmitter is enabled, interframe time fill (either non-shared flags or continuous ones), is transmitted.

When the XFIFO becomes empty and a frame end indication has not been issued, an error interrupt status is generated. An abort sequence (instead of FCS plus flag) is automatically transmitted following the last byte entered.

Maintenance Functions

Two test loops are provided in the ITAC. The "remote" test loop is located close to the DCE/DTE interface. The "local" test loop is located close to the Synchronous Network Interface (Figure 9).

In the remote loop mode, communication between the local DCE/DTE and Serial Communication Logic is possible.

In the local loop mode "all ones" or tri-state is transmitted to the Synchronous Network Interface.

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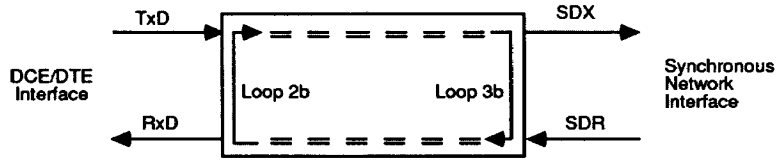

Figure 9. ITAC Test Loops

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OPERATIONAL DESCRIPTION

Register Set

The communication between the microcontroller and the ITAC is done via a set of directly accessible 8-bit registers.

The register set can be divided into:

- interrupt status registers and status registers for supervising the operation of the circuit, and registers for data transfer to the microcontroller;
- control registers for configuring the ITAC according to the different phases of a data call, registers for parameter selection, command registers and registers for data transfer from the microcontroller.

Interrupt Structure

Since the ITAC provides only one interrupt request output, the cause of an interrupt is determined by the microcontroller by reading the Interrupt Status Register IST. The bits in IST point to status registers, as shown in Figure 10.

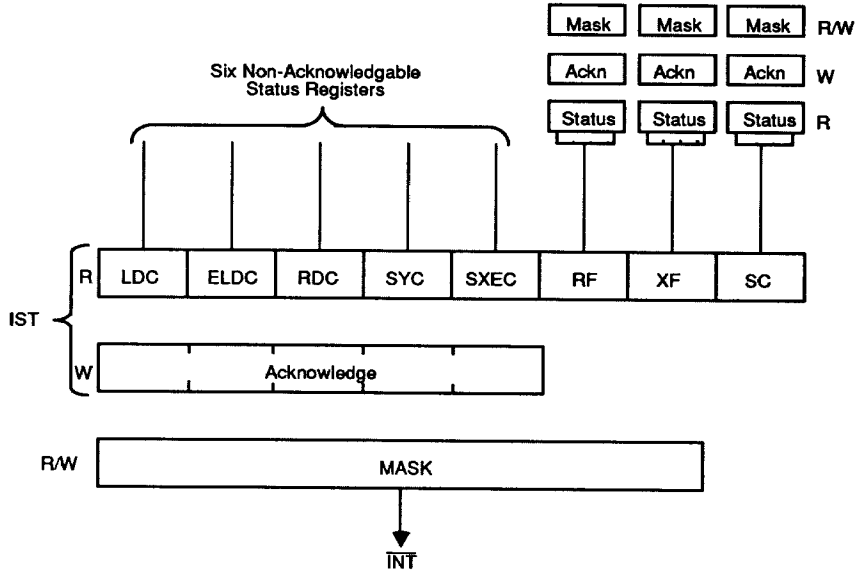

Figure 10. Interrupt/Status Register Structure

A "1" in any of the IST register bits causes the $\overline{INT}$ line to be activated.

$\overline{INT}$ is deactivated when all the bits set in IST are acknowledged by the microcontroller, or reset internally by the ITAC.

The IST register bits can be selectively masked (MASK). This has no effect on the IST register bits, but a masked interrupt status bit in IST does not cause the $\overline{INT}$ line to be activated.

Status Registers

The status registers are listed in Table 8.

Six of the registers contain information concerning the state of the communicating DTEs, the state of synchronization of the ITAC, and S, X and E bit status. A change in any of the registers causes an interrupt status bit in IST to be set.

The other three registers include the state of the Serial Communication Logic and information about special events. A "1" in one of the bits in these registers causes the interrupt status bit in IST to be set. An active status is reset when the condition that caused it is no longer true, or when acknowledged by the microcontroller. The registers have an individual mask register. An active mask bit prevents the bit in IST from being set, but the status can be polled in the originating register.

Acknowledgment is performed by writing a "1" in the position of the status bit.

In addition to the eight status registers which are part of the interrupt logic, one register is provided which is polled by the microcontroller but which may not cause interrupts (STR).

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Table 8. Interrupts and Status Registers

Interrupt status	Source of Interrupt Status	Maskable status	Interrupt/Status acknowledged through
LDC	Change in Local DTE Status (LDS	No	IST
ELDC	Change in Local DTE Status (ELDS)	No	IST
RDC	Change in Remote DTE Status (RDS)	No	IST
SYC	Change in Synchronization Status (SYS)	No	IST
SXEC	Change in S, X, or E bits (SXS, ES)	No	ST
RF	Receiver and RFIFO Status (RFS):	Yes	RFS
	HDLC Receive Data USART Receive Data HDLC Receive FIFO Full USART Receive FIFO Full Receive Message End Reception Receive Message End Framing Error Parity Error		
XF	Transmitter and XFIFO Status (XFS):	Yes	XFS
	HDLC Transmit FIFO Write Enable USART Transmit FIFO Write Enable HDLC Transmit FIFO Empty USART Transmit FIFO Empty HDLC Transmit Data Underrun		
SC	Special Condition Status (SCS):	Yes	SCS
	HDLC Receive FIFO Overflow USART Receive FIFO Overflow Break Begin Break End Local Character 1 Recognized Local Character 2 Recognized Remote Character 1 Recognized Remote Character 2 Recognized		
	Additional status information:		
	Status Register (STR)		STR

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Write Registers

Table 9. Write Registers

Mask Registers		Write/Read
MASK	Interrupt Status Mask Register	W/R
RFIM	Receiver & RFIFO Interrupt Status Mask Register	W/R
XFIM	Transmitter & XFIFO Interrupt Status Mask Register	W/R
SCIM	Special Condition Interrupt Status Mask Register	W/R
Configuration Registers		
GCR	General Configuration Register	W/R
SCR	Special Configuration Register	W/R
AICR	Asynchronous Interface Configuration Register	W/R
DPCR	Data Path Configuration Register	W/R
HMR	HDLC Mode Register	W/R
UMR	USART Mode Register	W/R
Operational Parameter Registers		
BRS	Bit Rate Select	W/R
TSR	Time Slot Register	W/R
NRF	Number of Retry Frames	W/R
Control Registers		
LDR	Local DTE Register	W/R
RDR	Remote DTE Register	W/R
XER	Transmitted E-bits	W/R
Command Registers		
HCC	HDLC Controller Commands	W
UCC	USART Controller Commands	W
INSC	Character Insert	W/R
Constants & Special Character Registers		
SYN	Synchronization character	W/R
LCAR1	Recognizable Character 1 from Local DTE/DCE	W/R
LCAR2	Recognizable Character 2 from Local DTE/DCE	W/R
RCAR1	Recognizable Character 1 from Remote TA/DTE	W/R
RCAR2	Recognizable Character 2 from Remote TA/DTE	W/R
Other Registers		
TEST	Test Register	W

Reset State

The ITAC is in the reset state after power-on or after the application of a reset pulse on $\overline{RST}$.

In the reset state, all control registers are zeroed and all interrupts are masked. Synchronous Network Interface and DCE/DTE interface outputs are tri-state.

Power-Down State

The ITAC may be set in a standby state to save unnecessary power consumption when idle. For switching the ITAC between standby and operational states two cases are distinguished, according to whether the DCE/DTE interface is an X.21 interface, or a V.24 interface.

The characteristics of the standby state are shown in Table 10.

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Table 10. Characteristics of the Standby State

Output or function	X.21 (V24 = 0)	V.24 (V24 = 1)
Microcontroller Interface	Operational	Operational
Oscillator	Disabled	Enabled
Other logic	Disabled	DTR detection
RxD	Previous state	Previous state
S	Logical 1 or tri-state	Logical 1 or tri-state
Other DCE/DTE outputs	Previous state	Previous state
SDX	Tri-state	Tri-state

For an X.21 interface, switching between "standby" and "operational" is only subject to the state of the control bit PU (Power Up). The oscillator reaches a steady state within 10 ms after the PU bit is set to one.

In the V.24 case, standby is reached when PU is set to zero and DTR(108) interchange circuit is OFF. When DTR is switched ON, the standby state is left, an interrupt is generated, and the PU bit is set to one by internal logic. (Figure 11).

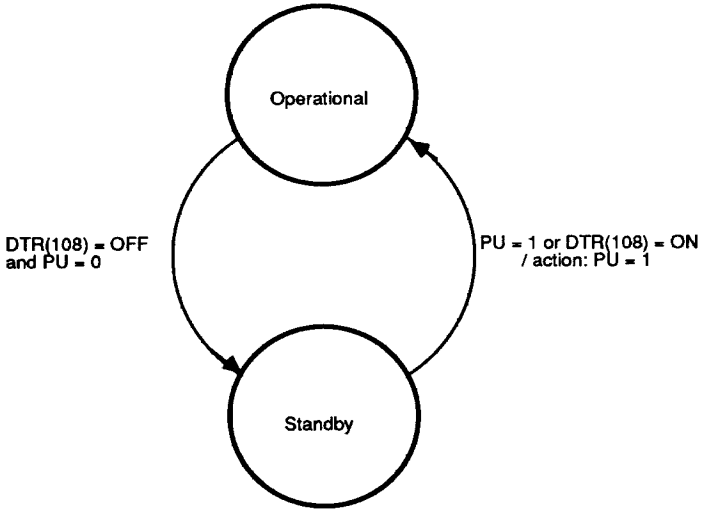

Figure 11. Standby State Diagram (V24 = 1)

Initialization

After reset, the user has to write a minimum number of registers to set the ITAC into an operational state. The most important among these are:

- General Configuration Register (GCR)
- Bit Rate Select Register (BRS)
- Data Path Configuration Register (DPCR)
- Local DCE/DTE Interface Register (LDR).

Interrupts are enabled via the MASK register.

The microcontroller may switch the ITAC into operational state at any time, not necessarily at initialization—unless a clock is required by the local DTE—but, say, upon detecting an incoming data call. Also the automatic wake-up feature can be used in the case of an outgoing call. Note that switching between "standby" and "operational" does not affect the contents of the registers.

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Processing

If the ITAC is run in transparent mode, the microcontroller has only a supervisory function. Special events, such as loss of synchronization, or changes in the state of the local or the remote DTE can be monitored via the interrupt logic, or by polling.

In the non-transparent mode, the Serial Communication Logic is activated. Data transfer itself can be interrupt, polling or DMA-driven.

Interrupt Operations

If neither the USART nor the HDLC controller is used in DMA, the non-DMA mode is selected (DMA = 0).

Reception

The reception of data is supervised via the Receiver and RFIFO Status register (RFS).

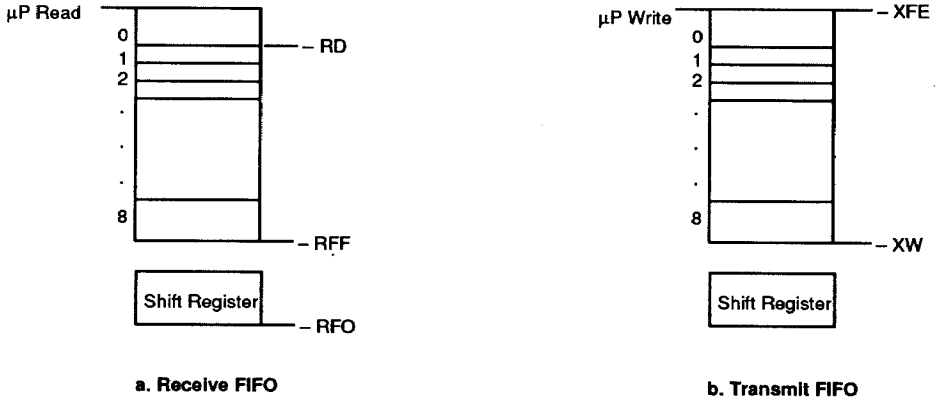
USART

The USART Receive Data (URD) maskable interrupt status indicates that at least one character is stored in the Receive FIFO. The URD status is reset when the RFIFO is empty.

The reaction time of the microcontroller to a URD interrupt status is, in the worst case, 1 ms (64 kbps synchronous data transfer).

The receive FIFO Full (URFF) interrupt status indicates that the Receive FIFO contains nine characters. This interrupt should be serviced with a high priority, otherwise a Receive FIFO Overflow (URFO) interrupt status might occur.

The Framing Error and Parity Error bits (FER, PER) may also be enabled to generate an interrupt, or, else, can be polled in RFS. These bits are updated every time a character is read from RFIFO.



a. Receive FIFO

b. Transmit FIFO

Figure 12. FIFO Status Indications

HDLC

Data transfer over the HDLC receive FIFO is similar to the USART case. The interrupt status HDLC Receive Data (HRD) indicates that at least one byte of data is stored in RFIFO. The HDLC Receive FIFO Full (HRFF) interrupt status indicates that nine bytes are stored. Loss of data is indicated by:

- HDLC Receive FIFO Overflow (HRFO) interrupt status if the first byte of an HDLC frame could not be stored because of a full RFIFO, and consequently one or more HDLC frames are lost;
- Otherwise the loss of data is indicated by the RDO (Receive Data Overflow) bit in the status byte of the corresponding frame.

The end of a frame is indicated by the Receive Message End (RME) bit in RFS. This status is updated every time a byte is read from RFIFO, and may also be enabled as an interrupt status.

Transmission

The transmission of data is supervised via the Transmitter and XFIFO Status register (XFS).

USART

The USART Transmit FIFO Write enable (UXW) maskable interrupt status indicates that one or more characters may be written in the Transmit FIFO. The UXW status is reset when the XFIFO is full.

When all characters in the XFIFO have been read, a Transmit FIFO Empty (UXFE) interrupt status is generated. When the XFIFO becomes empty, "1" (async), or

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the last entered character (sync) is continuously transmitted.

HDLC

Data transmission over the HDLC XFIFO is similar to the USART case. In addition to HXW and HXFE a HDLC Transmit Data Underrun (HXDU) interrupt status bit is provided, which is activated when the last byte in XFIFO has been transmitted and no XME command has been issued. The frame is closed with an abort sequence. If the frame is not yet complete, the HXFE interrupt should be serviced with high priority to prevent HXDU from occurring.

Polling Operations

For polling driven operations non-DMA mode is programmed in the General Configuration Register (DMA = 0). Interrupts are disabled by masking in the MASK register. The Interrupt Status Register, however, can be polled and the status bits may be acknowledged as usual. Events can also be masked at the status register level, in which case they do not cause bits to be set in the Interrupt Status Register.

DMA Operations

USART

DMA mode (DMA = 1) with USART (DMH = 0) is programmed in the General Configuration Register.

Receiver

The USART Receive FIFO Full (URFF) interrupt status indicates that a DMA output request (DMOR) is pending and the RFIFO is full. It serves as a request for the microcontroller to program the DMA controller. The URFF status is withdrawn when less than nine characters are present in the ITAC.

Up to nine characters may be stored inside the ITAC before loss of data. The DMOR request is automatically generated until all characters have been read.

Generation of DMOR request is blocked when a PER or an FER interrupt status occurs (if enabled in RFIM). Generation of DMOR can be resumed when the PER/FER interrupt status is acknowledged by the microcontroller.

Loss of data is indicated by the URFO interrupt.

Transmitter

The DMA input request (DMIR) is initially generated by the ITAC when the DMA Start Command (UDMS) is issued. A DMIR request is generated as long as space is left in the XFIFO. If the DMA controller does not respond to the request before the last character is read from the XFIFO, a Transmit FIFO Empty (UXFE) interrupt is generated and DMIR is withdrawn. After a UXFE interrupt, DMA transfer may be started anew by reissuing a UDMS command.

HDLC

DMA mode (DMA = 1) with HDLC (DMH = 1) is programmed in the General Configuration Register.

Receiver

The HDLC Receive FIFO Full (HRFF) interrupt status indicates that a DMA output request (DMOR) is pending and the RFIFO is full. It serves as a request for the microcontroller to program the DMA controller. The HRFF status is withdrawn when less than nine bytes are present in the ITAC.

A Receive Message End Received (RMER) interrupt can be also used as a request to program the DMA controller. It indicates that the end of an HDLC frame has been received.

Up to nine bytes may be stored inside the ITAC before loss of data. The DMOR request is generated until all bytes have been read.

When the status byte pertaining to a received HDLC frame is read, a Receive Message End (RME) interrupt status is generated. Simultaneously, EODR output is activated. The status bit remains set until acknowledged by the microcontroller. Generation of DMOR requests is blocked until RME has been acknowledged, and restarted thereafter. If the microcontroller does not acknowledge the RME status before a RFIFO overflow occurs, then:

- If the first byte of a receive frame could not be stored, a HDLC Receive FIFO Overflow (HRFO) is generated;
- Otherwise, the overflow is indicated in the status byte of the corresponding frame.

The EODR output is deactivated when RME is acknowledged.

Transmitter

The DMA input request (DMIR) is initially generated by the ITAC when the DMA Start Command (HDMS) is issued. When a byte has been fetched for transmission, a new request is generated. If the DMA controller does not respond to the request before the XFIFO is empty, a Transmit FIFO Empty (HXFE) interrupt is generated, DMIR is withdrawn and the frame is automatically closed by appending a FCS and a closing flag. DMA transfer may be started anew by reissuing a HDMS command.

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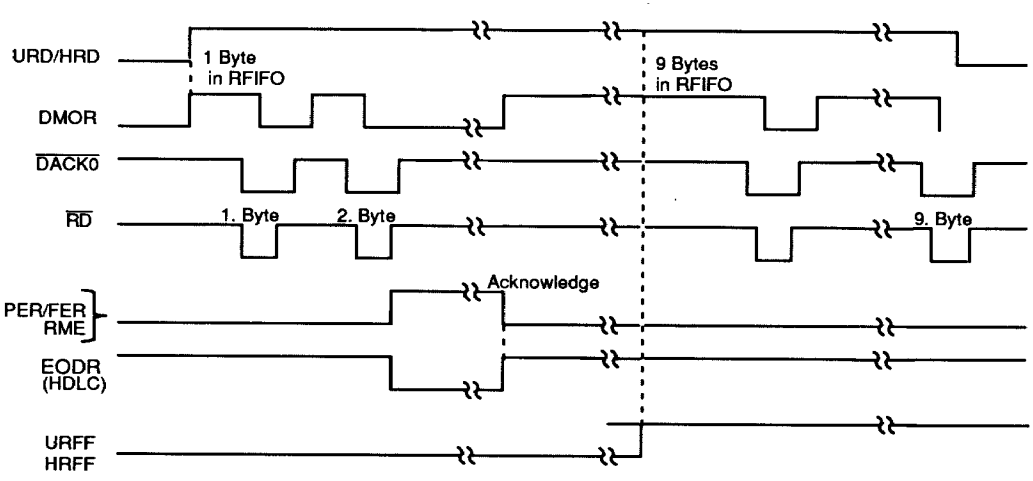
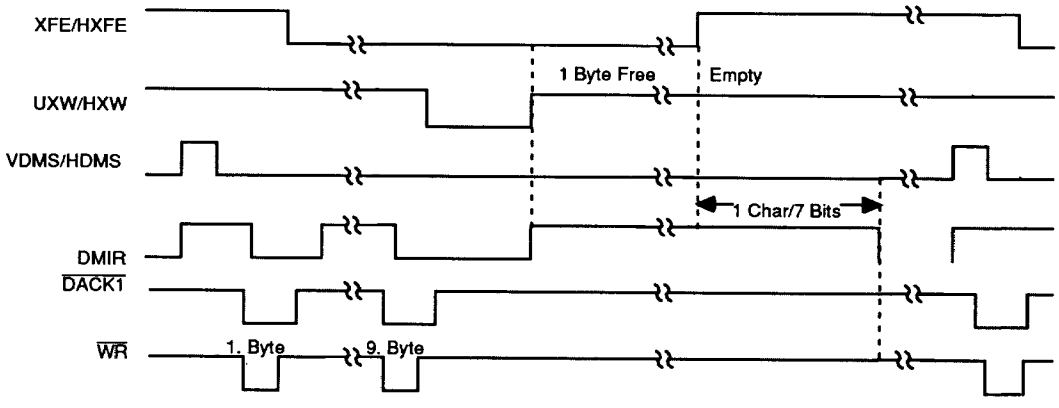


a. Receive



b. Transmit

Figure 13. DMA Operation

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DETAILED REGISTER DESCRIPTION

Register Space

In order to facilitate a direct connection to 16-bit processors, it is possible to access all ITAC registers using either even microprocessor addresses only or odd microprocessor addresses only.

The register address map is shown in Figure 14.

Interrupt/Status Registers

Interrupt Status Register (IST)

LDC	ELDC	RDC	SYC	SXEC	RF	XF	SC

LDC Local DTE Status Change (status register LDS)

ELDC Extended Local DTE Status Change (status register ELDS)

RDC Remote DTE Status Change (status register RDS)

SYC Synchronization Status Change (status register SYS)

SXEC S, X or E bit Status Change (status register SXS, ES)

RF Receiver and RFIFO Status (status register RFS)

XF Transmitter and XFIFO Status (status register XFS)

SC Special Condition Status (status register SCS)

Local DTE Status (LDS)

Non-X.21 Mode (V24 = 1)

DTR	RTS	MI1	MI2	MI3	X	X	X

DTR Data Terminal Ready interchange circuit state

RTS Request To Send interchange circuit state

MI1–3 Multifunctional input states

X.21 Mode (V24=0)

LONO	LOFO1	LL3	X	X	X	X	X

LON0 Local (0, ON) state

LOF01 Local (0101..., OFF) state

LL3 Local Loop 3. Local (00001111..., OFF) state

Extended Local DTE Status (ELDS)

X.21 mode only (V24 = 0).

LONX	LOFX	LON1	LOF1	LOF0	LL2	X	X

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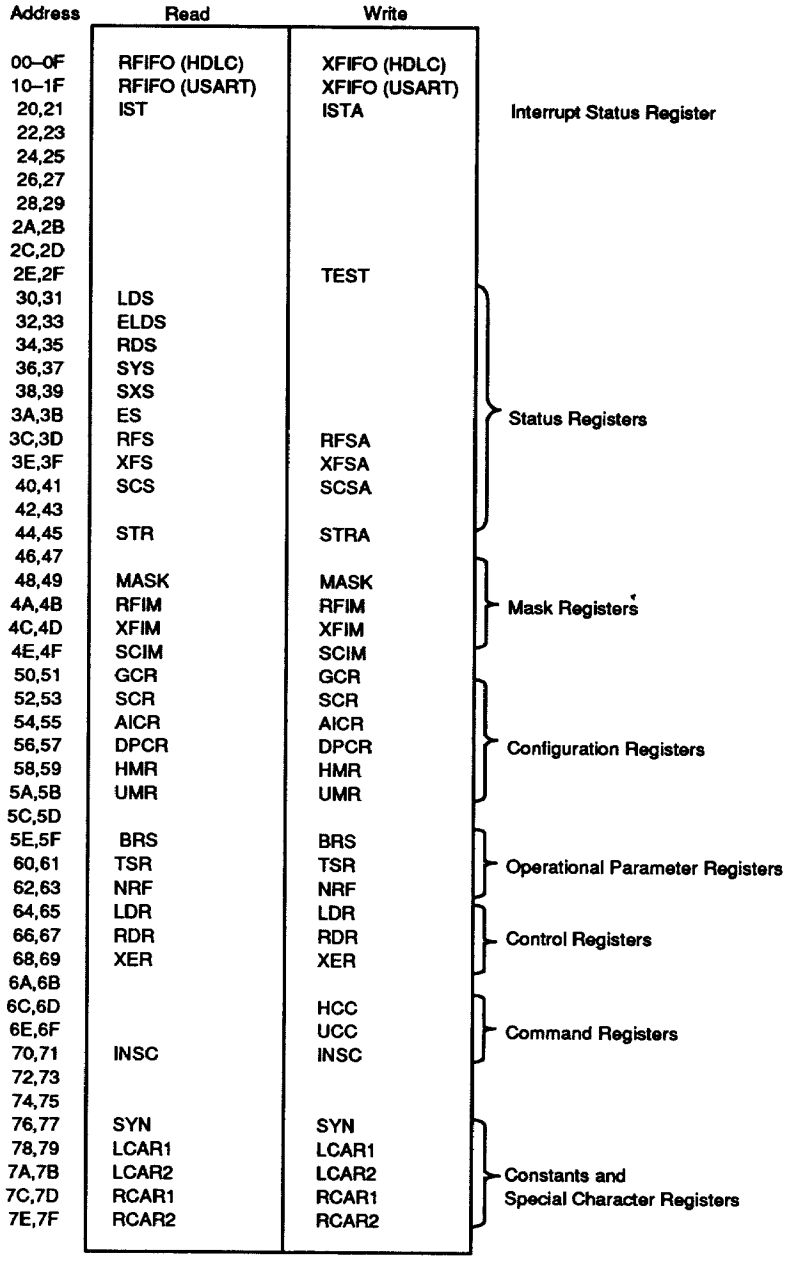

Figure 14. ITAC Register Map

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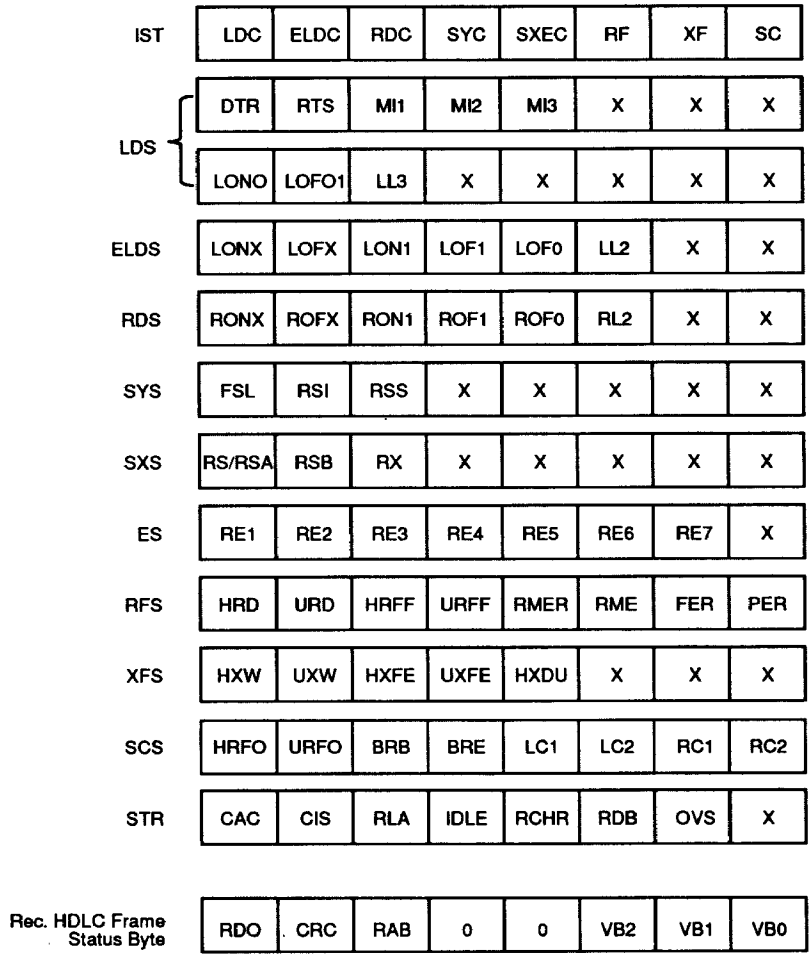

Figure 15. ITAC Status Register Summary

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Extended Local DTE Status (ELDS)

X.21 mode only (V24 = 0).

LONX	LOFX	LON1	LOF1	LOF0	LL2	X	X

LONX Local (X, ON) state

LOFX Local (X, OFF) state

LON1 Local (1, ON) state

LOF1 Local (1, OFF) state

LOF0 Local (0, OFF) state

LL2 Local Loop 2. Local (0011. . . , OFF) state

Remote DTE Status (RDS)

RONX	ROFX	RON1	ROF1	ROF0	RL2	X	X

RONX Remote (X, ON) state

ROFX Remote (X, OFF) state

RON1 Remote (1, ON) state

ROF1 Remote (1, OFF) state

ROF0 Remote (0, OFF) state

RL2 Remote Loop 2. Remote (0011. . . , OFF) state

Synchronization Status (SYS)

FSL	RSI	RSS	X	X	X	X	X

FSL Frame Sync Loss of the intermediate rate receiver. At least three consecutive erroneous frames have been received.

RSI Resynchronization Impossible. The intermediate rate receiver has not achieved synchronization.

RSS Resynchronization Successful. The intermediate rate receiver is synchronous.

S- and X-Bit Status (SXS)

RS/RSA	RSB	RX	X	X	X	X	X

RS/RSA Received S (V110 = 0) or SA (V110 = 1) bit

RSB Received SB bit (V110 = 1)

RX Received X bit

E-Bit Status (ES)

RE1	RE2	RE3	RE4	RE5	RE6	RE7	X

RE1–7 Received E-bits

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Receiver and RFIFO Status (RFS)

HRD	URD	HRFF	URFF	RMER	RME	FER	PER

HRD HDLC Receive Data in RFIFO

URD USART Receive Data in RFIFO

HRFF HDLC Receive FIFO Full

URFF USART Receive FIFO Full

RMER Receive Message End Reception

RME Receive Message End

FER Framing Error

PER Parity Error

Transmitter and XFIFO Status (XFS)

HXW	UXW	HXFE	UXFE	HXDU	X	X	X

HXW HDLC Transmit FIFO Write enable

UXW USART Transmit FIFO Write enable

HXFE HDLC Transmit FIFO Empty

UXFE USART Transmit FIFO Empty

HXDU HDLC Transmit Data Underrun

Special Condition Status (SCS)

HRFO	URFO	BRB	BRE	LC1	LC2	RC1	RC2

HRFO HDLC Receive FIFO Overflow

URFO USART Receive FIFO Overflow

BRB Break Signal Begin

BRE Break Signal End

LC1 LCAR1 Character recognized from local DTE

LC2 LCAR2 Character recognized from local DTE

RC1 RCAR1 Character recognized from remote DTE/TA

RC2 RCAR2 Character recognized from remote DTE/TA

Status Register (STR)

CAC	CIS	RLA	IDLE	RCHR	RDB	OVS	X

CAC Command Accepted. Polling bit to monitor the execution of HRR, HXR, URR, UXR, SBK, HNT and TRA command

CIS Character Insertion Status. A character can be inserted in the receive character stream using INSC (1)

RLA Receive Line Active. HDLC flags/messages are being received (1) or not (0)

IDLE Idle state on HDLC receive line. A row of at least fifteen ones has been detected since the last acknowledgment (1)

RCHR Receive Characters detected. Only stop bits have been received from the DCE/DTE interface since the last acknowledgment (0)

RDB Receive Data Byte. Set after every eighth bit in X.30/V.110 frame (P8,Q8,R8 or D8,D16,D24. . .)

OVS Overspeed. The local DTE/DCE is transmitting characters at a rate exceeding the tolerance range

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Receive HDLC Frame Status Byte

RDO	CRC	RAB	0	0	VB2	VB1	VB0

RDO Receive Data Overflow

CRC CRC Check Correct (1)

RAB Receive Abort

VB2–0 Valid bit count in the last byte received

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Write Register

Mask Registers:

MASK									R/W
RFIM									R/W
XFIM									R/W
SCIM									R/W

Configuration Registers:

GCR	PU	DOE	V24	V110	ASY	ENFR	DMA	DMH	R/W
SCR	TS5	DLL	LCS	RCS	F56	0	0	0	R/W
AICR	CHL1	CHL0	STP	TR	0	0	0	0	R/W
DPCR	RDC1	RDC0	XDC1	XDC0	RSC	XSC	TL2	TL3	R/W
HMR	HRLC	HXLC	HREN	HXEN	HINV	ITF	0	0	R/W
UMR	ASYC	PTY	UREN	UXEN	SCM	PY1	PY0	0	R/W

Operational Parameter Registers:

BRS	UR3	UR2	UR1	UR0	NR3	NR2	NR1	NR0	R/W
TSR	TS4	TS3	TS2	TS1	TS0	ICS2	ICS1	ICS0	R/W
NRF	N7	N6	N5	N4	N3	N2	N1	N0	R/W

Figure 16. ITAC Control Register Summary

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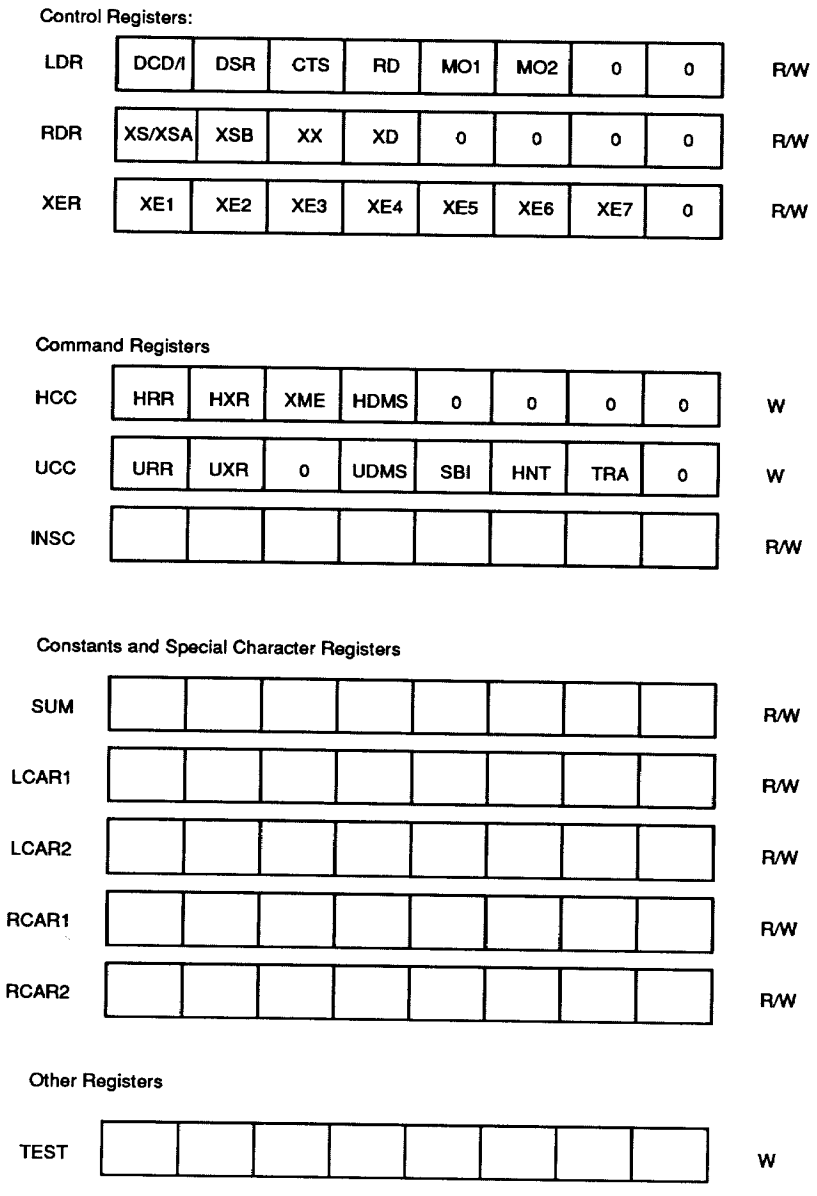

Figure 16. ITAC Control Register Summary (continued)

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Mask Registers

Interrupt Status Mask Register (MASK) R/W

A zero in a bit of MASK inhibits the interrupt from the corresponding bit position of the IST register. However the bit in IST will still indicate the status and thus masked interrupts may be polled.

Receiver & RFIFO Interrupt Status Mask Register (RFIM) R/W

A zero in a bit of RFIM inhibits the status in IST being activated by the corresponding bit in RFS. However the bit in RFS will still indicate the status and thus may be polled.

Transmitter & XFIFO Interrupt Status Mask Register (XFIM) R/W

A zero in a bit of XFIM inhibits the status in IST being activated by the corresponding bit in XFS. However the bit in XFS will still indicate the status and thus may be polled.

Special Condition Interrupt Status Mask Register (SCIM) R/W

A zero in a bit of SCIM inhibits the status in IST being activated by the corresponding bit in SCS. However, the bit in SCS will still indicate the status and thus may be polled.

Configuration Registers

General Configuration Register (GCR) R/W

PU	DOE	V24	V110	ASY	ENFR	DMA	DMH

PU Power-up. Forces the ITAC into power-up

DOE DCE/DTE Interface Output Enable

V24 X.21 (0) or non-X.21 (1) interface

V110 Protocol according to X.30 (0) or V.110 (1)

ASY Async (1) or Sync (0) DCE/DTE interface

ENFR Enable Frame. When 0, the Synchronous Network Interface output is inactive and the receiver is idle

DMA DMA mode (1) or not (0)

DMH DMA mode for HDLC controller (1) or for USART (0)

Special Configuration Register (SCR) R/W

TS5	DLL	LCS	RCS	F56	0	0	0

TS5 Time Slot Select MSB. Used only for Synchronous Network Interface data rates greater than 2.048 Mbps

DLL Double Last Look On. Receive status bit changes are mapped on DCE/DTE interface using double last look logic (1)

LCS Local Character Stop. Any character from DCE/DTE interface that matches LCAR1 or LCAR2 is stopped (1). Used for XON/XOFF flow control and Hayes protocol

RCS Remote Character Stop. Any character from remote DTE/TA that matches RCAR1 or RCAR2 is stopped (1).Used for XON/XOFF flow control

F56 Frame for 56 kbps. Bit 8 of a 64 kbps channel is filled with "1" (0), or with the pattern "0X S3 S4 1 1 1 1" (1)

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Async Interface Configuration Register (AICR) R/W

CHL1	CHL0	STP	TR	0	0	0	0

CHL0–1 Character Length, excluding possible parity bit:

CHL1	CHL0	Length
0	0	eight
0	1	seven
1	0	six
1	1	five

STP Stop bits. One (0) or two (1) stop bits per character.

TR Tolerance Range. Normal 12.5% (0) or extended 25% (1) tolerance range for local DTE overspeed.

Data Path Configuration Register (DPCR) R/W

RDC1	RDC0	XDC1	XDC0	RSC	XSC	TL2	TL3

RDC0–1 Receive Data Connect

RDC1	RDC0	
0	0	RxD is connected to register bit RD
0	1	RxD is connected to Serial Communication Logic
1	0	RxD is connected to D-bits

XDC0–1 Transmit Data Connect

XDC1	XDC0	
0	0	D-bits are equal to register bit XD
0	1	D-bits originate from Serial Communication Logic
1	0	D-bits originate from TxD

RSC Receive S-bit Connect. Received S/SA, SB bits are mapped on to DCE/DTE interface interchange circuits (1).

XSC Transmit S-bit Connect. Transmitted S/SA, SB bits originate from the microcontroller interface (0) or are mapped from DCE/DTE interface interchange circuits (1).

TL2 Test Loop 2 activation.

TL3 Test Loop 3 activation.

HDLC Mode Register (HMR) R/W

HRLC	HXLC	HREN	HXEN	HINV	ITF	0	0

HRLC HDLC Receiver to Local DTE Connection. The HDLC Receiver is connected to DCE/DTE interface and the USART Receiver to network (1) or vice versa (0).

HXLC HDLC Transmitter to Local DTE Connection. The HDLC Transmitter is connected to DCE/DTE interface and the USART Transmitter to network (1) or vice versa (0).

HREN HDLC Receiver Enable.

HXEN HDLC Transmitter Enable.

HINV HDLC normal (0) or inverted (1).

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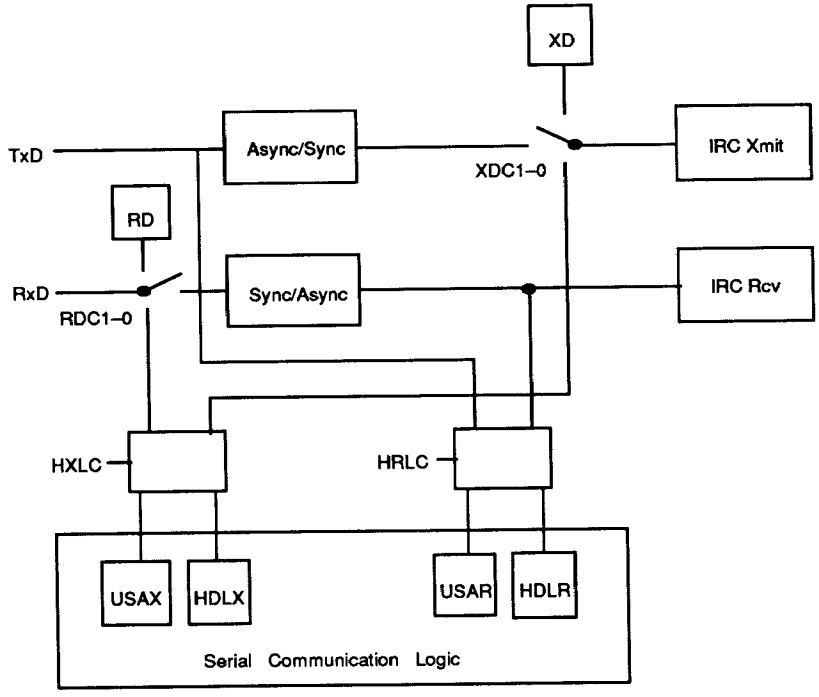

Figure 17. Serial Communication Logic

USART Mode Register (UMR) R/W

ASYC	PTY	UREN	UXEN	SCM	PY1	PY0	0

ASYC Asynchronous (1) or Synchronous (0) mode.

PTY Parity. Hardware parity check/generation (1) or not (0).

UREN USART Receiver Enable.

UXEN USART Transmitter Enable.

SCM Synchronous Communication Mode. Bisync (0) or Monosync (1).

PY0–1 Parity type. Used when PTY = 1.

PY1	PY0	Type
0	0	0
0	1	odd
1	0	even
1	1	1

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Operational Parameter Registers

Bit Rate Select (BRS) R/W

UR3	UR2	UR1	UR0	NR3	NR2	NR1	NR0

UR0–3 User rate

NR0–3 Network rate

UR3	UR2	UR1	UR0	Rate, bps	DTE TYPE ASY=1	DTE TYPE ASY=0
0	0	0	0	300	x	
0	0	0	1	600	x	x
0	0	1	0	1200	x	x
0	0	1	1	2400	x	x
0	1	0	0	4800	x	x
0	1	0	1	9600	x	x
0	1	1	0	19200	x	x
0	1	1	1	38400	x	x
1	0	0	0	48000		x
1	0	0	1	56000		x
1	0	1	0	64000		x
1	0	1	1	reserved		
1	1	x	x	reserved		

NR3	NR2	NR1	NR0	Rate, bps
0	0	0	x	600
0	0	1	0	1200
0	0	1	1	2400
0	1	0	0	4800
0	1	0	1	9600
0	1	1	0	19200
0	1	1	1	38400
1	0	0	0	48000
1	0	0	1	56000
1	0	1	0	64000
1	0	1	1	reserved
1	1	x	x	reserved

Time-Slot Register (TSR) R/W

TS4	TS3	TS2	TS1	TS0	ICS2	ICS1	ICS0

TS0–4 Time Slot Select. Selects one 8-bit time slot out of a maximum of 32 or 64 (if TS5 is used) on the Synchronous Network Interface.

ICS0–2 Intermediate Rate Channel Select. Position of the first bit of intermediate rate channel inside the 8-bit time slot.

Number of Retry Frames Register (NRF) R/W

Determines the number of intermediate rate frames after initial Frame Sync Loss (FSL) status, during which resynchronization is attempted. If synchronism is not achieved within NRF frames, a RSI status is generated.

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Control Registers

Local DTE Control Register (LDR) R/W

DCD/I	DSR	CTS	RD	MO1	MO2	0	0

DCD/I State of DCD/I interchange circuit.

DSR State of DSR interchange circuit.

CTS State of CTS interchange circuit.

RD Value of RxD.

MO1–2 State of Multifunctional Output 1–2.

Remote DTE Control Register (RDR) R/W

XS/XSA	XSB	XX	XD	0	0	0	0

XS/XSA Value of Transmitted S/SA bit.

XSB Value of Transmitted SB-bit.

XX Value of Transmitted X-bit.

XD Value of Transmitted D-bit.

Transmitted E-bit Register (XER) R/W

XE1	XE2	XE3	XE4	XE5	XE6	XE7	0

Value of transmitted E-bits in intermediate rate frame.

Command Registers

HDLC Controller Command Register (HCC) W

HRR	HXR	XME	HDMS	0	0	0	0

HRR HDLC Receiver Reset.

HXR HDLC Transmitter Reset.

XME Transmit Message End.

HDMS DMA Start for HDLC Transmitter.

USART Controller Command Register (UCC) W

URR	UXR	0	UDMS	SBK	HNT	TRA	0

URR USART Receiver Reset.

UXR USART Transmitter Reset.

UDMS DMA Start for USART Transmitter.

SBK Set Break. Forces the USART output to zero (start polarity) regardless of any data being transmitted at the time.

HNT Set Hunt Mode. Forces the USART to search for sync character(s) before starting to store data.

TRA Set Transparent Mode. Enables the USART to store receive data without regard for octet synchronization.

Character Insert Register (INSC) R/W

The character written in this register is inserted in the received character stream at the next opportunity. Received characters are not disturbed. The register may be written when CIS status bit is equal to "1."

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Constants and Special Character Registers

Synchronization Character Register (SYN)

In the hunt phase, the receiver searches for one (monosync) or two (bisync) characters before storing data.

Local Characters 1 and 2 (LCAR1, LCAR2)

Characters from the DCE/DTE interface are compared with LCAR1 and LCAR2. Upon a match, an interrupt status may be generated, and the character is optionally stopped. Used for Hayes protocol and for XON/XOFF flow control.

Remote Characters 1 and 2 (RCAR1, RCAR2)

Characters from the remote DTE/TA are compared with RCAR1 and RCAR2. Upon a match, an interrupt status may be generated, and the character is optionally stopped. Used for XON/XOFF flow control.

Other Registers

Test Register (TEST) W

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ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias . . . . . 0 to +70° C
Storage temperature . . . . . –65 to +125° C
Voltage on any pin
with respect to ground . . . . . –0.4 to V_{DD} +0.4 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0° to +70°C
Operating V_{DD} . . . . . 4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

T_A = 0 to +70°C; V_{DD} = 5 V ±5%, V_{SS} = 0 V.

Table 11. DC Characteristics

Symbol	Parameter	Limit Values Min.	Max.	Unit	Test Condition
V_{IL}	Input low voltage	–0.4	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD} + 0.4	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output high voltage	2.4		V	I_{OH} = –400 µA
V_{OH}	Output high voltage	V_{DD} –.5	V		I_{OH} = –200 µA
I_{CC}	Power operational supply			mA	V_{DD} = –5.V, CLK = 4 MHz Inputs at 0 V/V_{DD}
	Current power down			mA	No output loads
I_{LI}	Input leakage current		±10	µA	0 V < V_{IN} < V_{DD} to 0 V
I_{LO}	Output leakage current				0 V < V_{OUT} < V_{DD} to 0 V

PRELIMINARY

Capacitances

T_A = 25°C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V.

Table 12. DC Capacitances

	Symbol	Parameter	Limit Values Min.	Max.	Unit	Test Condition
All pins except SR1,2 XTAL1,2	CIN	Input capacitance			7	pF
	CIO	I/O capacitance			7	pF
XTAL1,2	CLD	Load capacitance			50	pF

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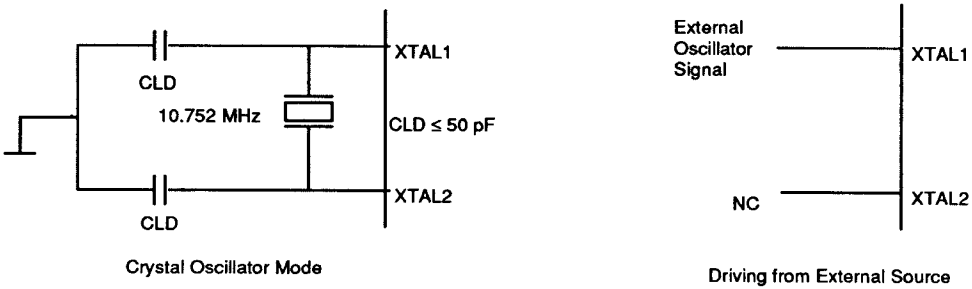

Figure 18. Recommended Oscillator Circuits

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SWITCHING CHARACTERISTICS over operating range

T_A = 0 to +70°C, V_{DD} = 5 V ±5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for logical "1" and at 0.8 V for a logical '0". The AC testing input/output waveforms are shown in Figure 19.

Figure 19. Input/Output Waveform for AC Tests

Clock

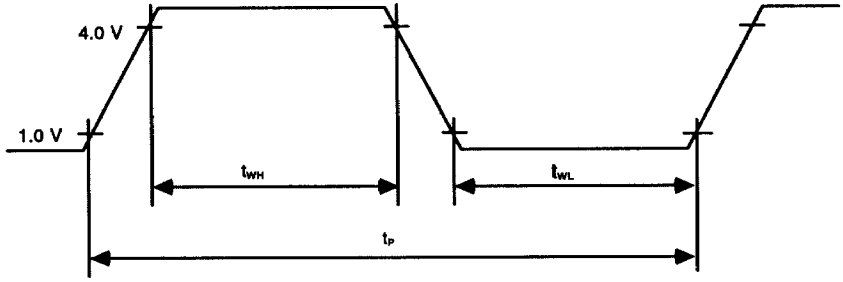

Figure 20. Definition of XTAL1 Period with Width

XTAL1,2

Table 13. XTAL1,2 Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Condition
t_P	Clock period	−100 ppm	93.005	+100 ppm	ns	
t_{WH}	Clock high	35			ns	
t_{WL}	Clock low	35			ns	

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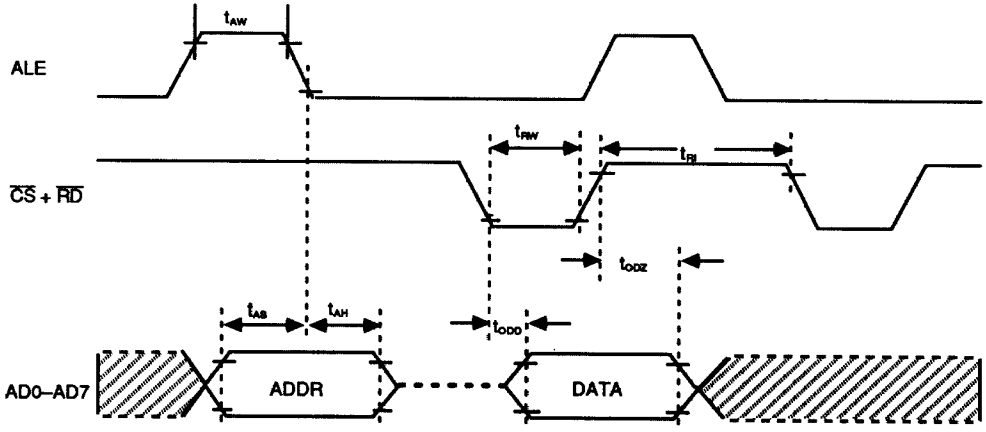

Figure 21. Microcontroller Read Cycle

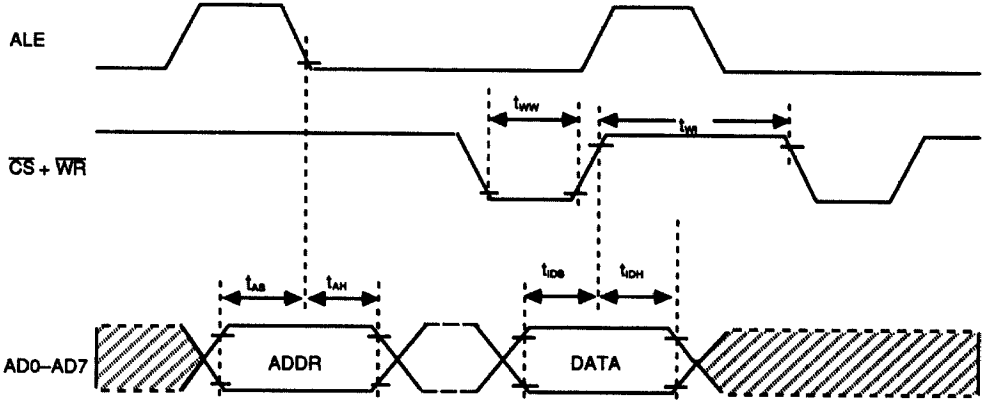

Figure 22. Microcontroller Write Cycle

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Table 14. Microcontroller Interface Timing

Symbol	Description	Min.	Max.	Unit	Condition
t_{AW}	ALE pulse width	50		ns	
t_{AS}	Address setup time to ALE	20		ns	
t_{AH}	Address hold time from ALE	10		ns	
t_{RW}	$\overline{RD}$ pulse width	110		ns	
t_{DDO}	Data output delay from $\overline{RD}$		110	ns	
t_{DDZ}	Output data high impedance from $\overline{RD}$		25	ns	
t_{RI}	$\overline{RD}$ control interval	70		ns	
t_{WW}	$\overline{WR}$ pulse width	60		ns	
t_{IDS}	Data setup time to $\overline{WR}$ + $\overline{CS}$	35		ns	
t_{IDH}	Data hold time from $\overline{WR}$ + $\overline{CS}$	10		ns	
t_{WI}	$\overline{WR}$ control interval	70		ns	

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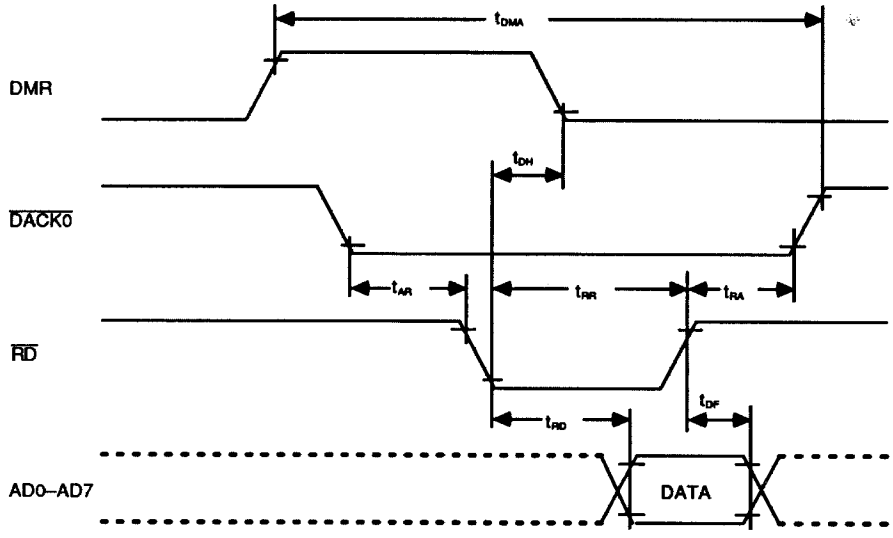
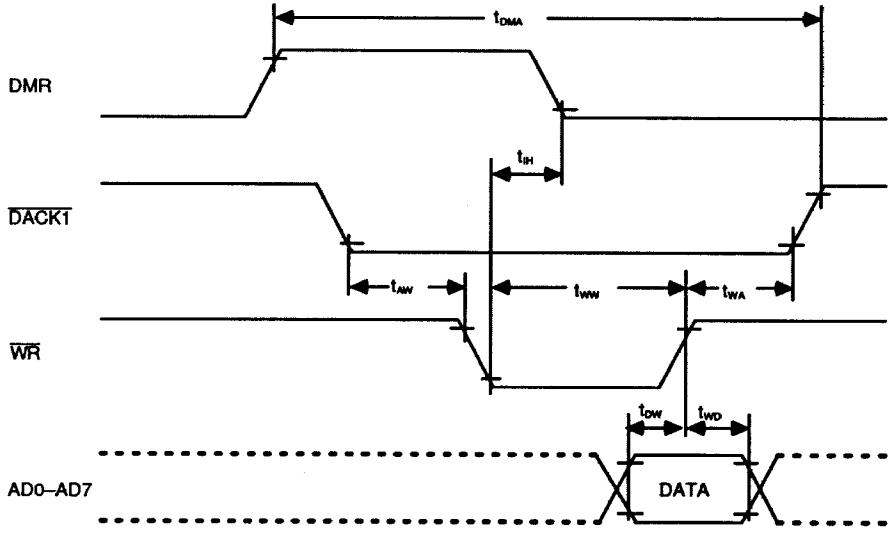


a. DMA Read



b. DMA Write

Figure 23. DMA Cycle

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Table 15. DMA Characteristics

Symbol	Description	Min.	Max.	Unit	Condition
t_{DH}	DMDR hold time		60	ns	
t_{AR}	Address stable before $\overline{RD}$	0		ns	
t_{RD}	Data delay from $\overline{RD}$		150	ns	
t_{DF}	Output floating delay	20		ns	
t_{RA}	Address hold after $\overline{RD}$	0		ns	
t_{RR}	$\overline{RD}$ pulse width	150		ns	
t_{IH}	DMIR hold time		80	ns	
t_{AW}	Address stable before $\overline{WR}$	0		ns	
t_{WA}	Address hold after $\overline{WR}$	0		ns	
t_{DW}	Data setup to $\overline{WR}$	30		ns	
t_{WD}	Data hold after $\overline{WR}$	25		ns	
t_{WW}	$\overline{WR}$ pulse width	100		ns	

Serial Interface Timing

Table 16. CLK Characteristics

Symbol	Description	Min.	Max.	Unit	Condition
t_P	CLK period	244		ns	
t_{WH}	CLK high	100		ns	
t_{WL}	CLK low	100		ns	

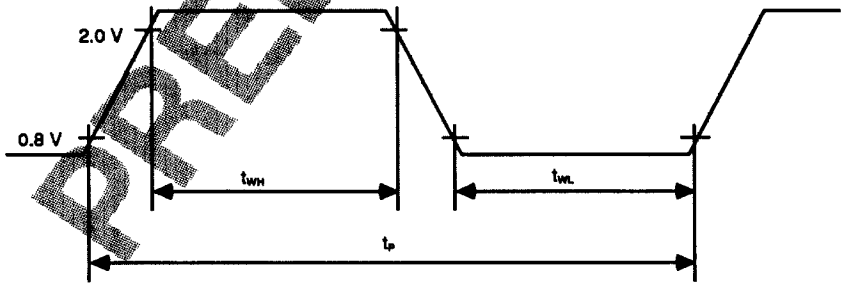

Figure 24. Definition of CLK Period and Width

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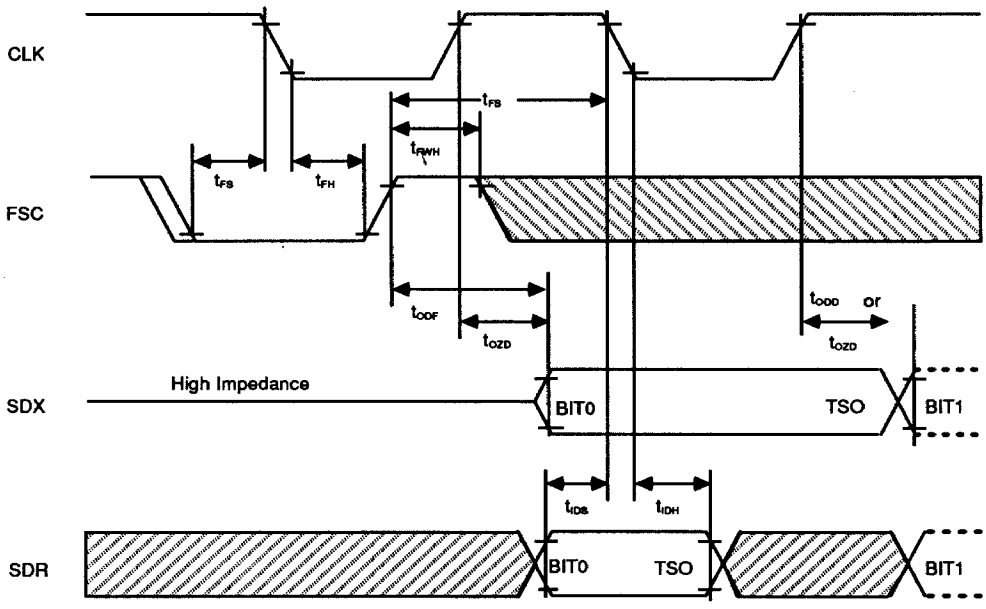

Figure 25. Synchronous Network Interface Timing

Table 17. Synchronous Network Interface Timing

Symbol	Description	Min.	Max.	Unit	Condition
t_{FS}	FSC setup time	40		ns	
t_{FH}	FSC hold time	40		ns	
t_{FWH}	FSC high width	40		ns	
t_{OZD}	SDX from high impedance to active from CLK		100	ns	
t_{ODD}	SDX from CLK		100	ns	
t_{ODZ}	SDX from active to high impedance from CLK		80	ns	
t_{ODF}	SDX from high impedance to active from FSC (Note)		100	ns	
t_{IDS}	SDR setup time	20		ns	
t_{IDH}	SDR hold time	40		ns	

PRELIMINARY

Note: This delay from FSC applies only when FSC repetition period is less than 512 bits, time slot 0 has been programmed, and CLK precedes FSC.

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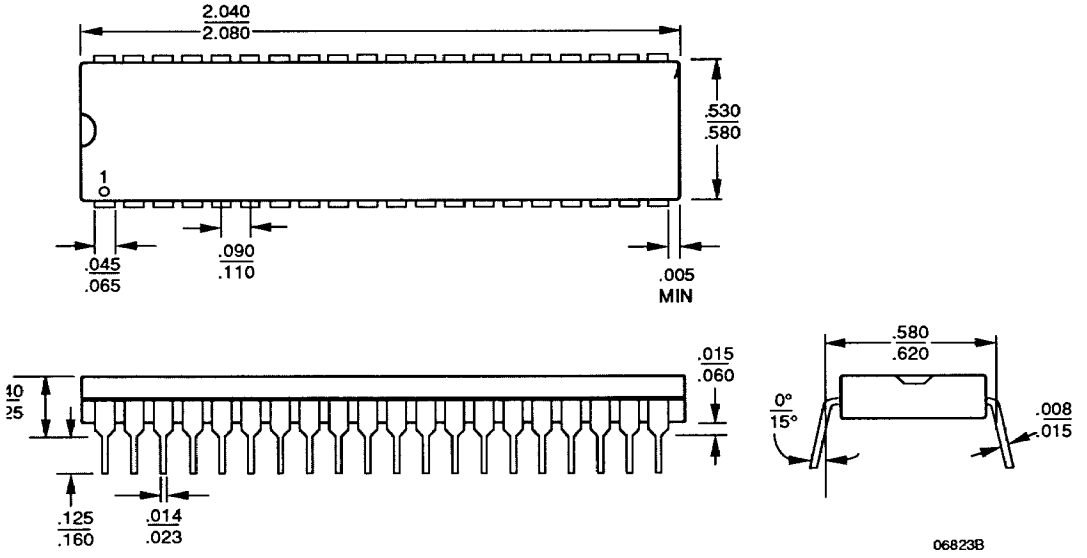
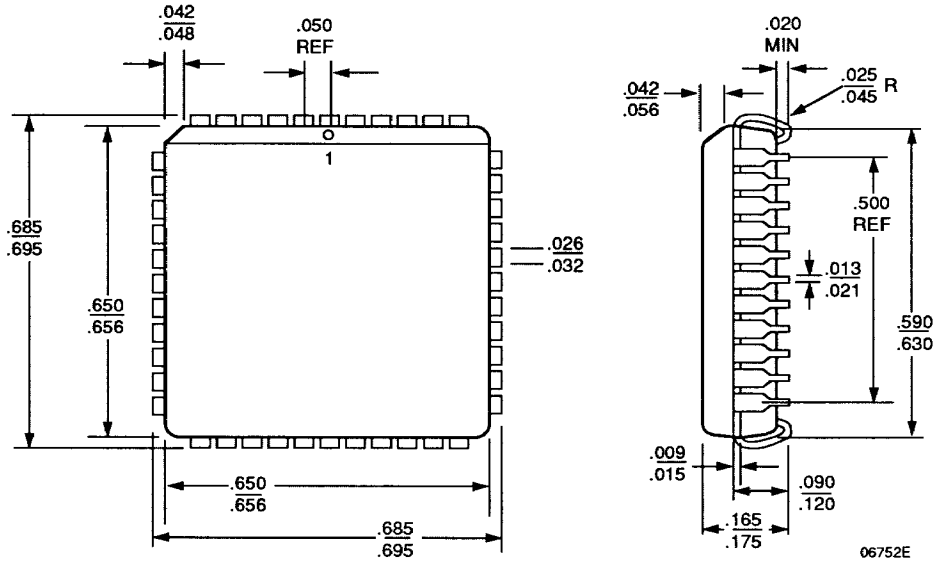
PHYSICAL DIMENSIONS

PD 040



PL 044



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