AMENDMENT

Am29F080 Data Sheet

1996 Flash Products Data Book/Handbook

INTRODUCTION

This amendment supersedes information regarding the Am29F080 device in the 1996 Flash Products Data Book/Handbook, PID 11796D. This document includes replacement pages for the Am29F080 data sheet, PID 19643A, which was also released as a standalone document.

This amendment will be available online via AMD's World Wide Web site (http://www.amd.com), in addition to the literature ordering hotline. All changes contained in this document will be included in the next release of the Flash Products Data Book/Handbook.

DOCUMENT ORGANIZATION

Table 1 lists the data book pages affected by this document and contains a description of changes for each page.

The remainder of this document contains the change pages. In the footer of the change pages are page numbers in parenthesis, which indicates the corresponding page in the data book or data sheet.

Table 1. Am29F080 Data Sheet Changes

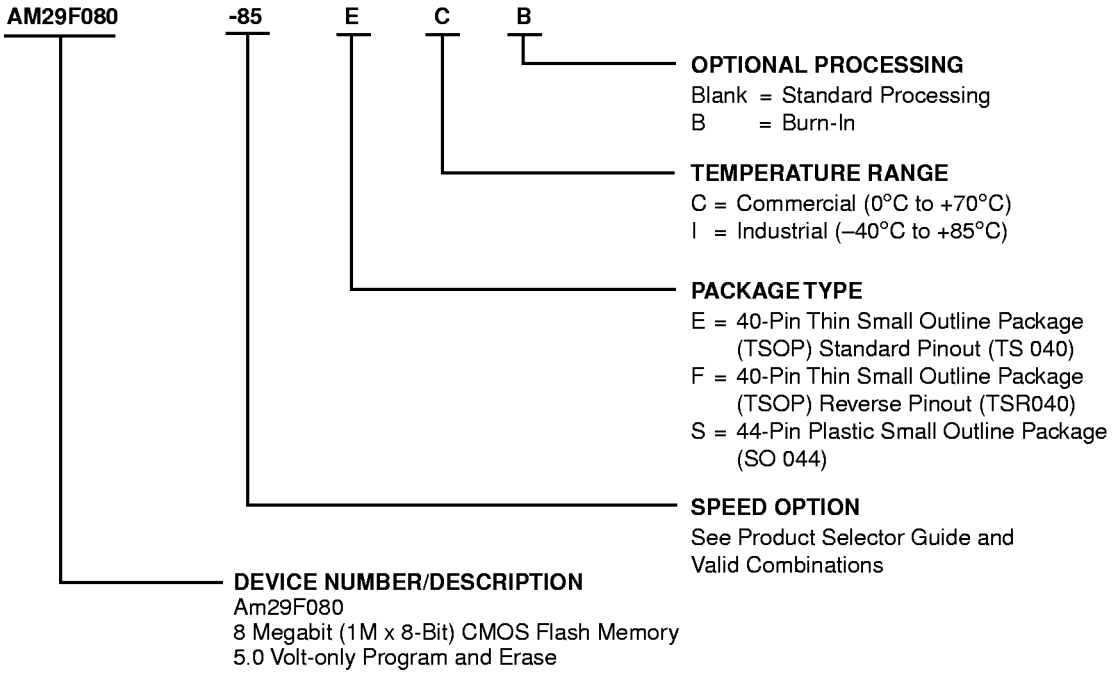
Amendment Page	Data Book Page	Standalone Data Sheet Page	Description of Changes
2	1-169	7	**Ordering Information, Standard Products:** Added the industrial temperature range to the -85 and -90 speed options.
3	1-185	23	**DC Characteristics, CMOS Compatible:** Improved specifications on I_{CC1}, I_{CC2}, and I_{CC3}. Added Note 4 to table.
4, 6	1-187, 1-194	25, 32	**AC Characteristics:** *Write/Erase/Program Operations:* Updated specifications for byte programming and sector erase.
5	1-192	30	**Figure 16, Temporary Sector Group Unprotect:** Corrected figure.
7	1-196	34	**Erase and Programming Performance:** Updated all parameters.
8, 9	Add to Section 6	35, 36	**Physical Dimensions:** *TS040 40 Pin Thin Small Outline Package, TSR040 40-Pin Reversed Thin Small Outline Package:* For standalone data sheet, modified drawing to indicate there are fewer pins shown on drawing than on actual product. For data book, the package drawings are new additions.

Publication# **19643** Rev: **A** Amendment/**1**
Issue Date: **December 1996**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F080-85	EC, ECB, EI, EIB, FC, FCB, FI, FIB, SC, SCB, SI, SIB
AM29F080-90	
AM29F080-120	
AM29F080-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DC CHARACTERISTICS (continued)

CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.0 Volt			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		25	40	mA
I_{CC2}	V_{CC} Active Program/Erase Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	40	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		1	5	µA
I_{CC4}	V_{CC} Standby Current (Reset)	$V_{CC} = V_{CC}$ Max, $\overline{RESET} = V_{SS} \pm 0.3$ V		1	5	µA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7x V_{CC}		V_{CC} +0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.0 Volt	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		4.2	V

Note:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 1 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *ICC active while Embedded Program or Erase Algorithm is in progress.*
3. *Not 100% tested.*

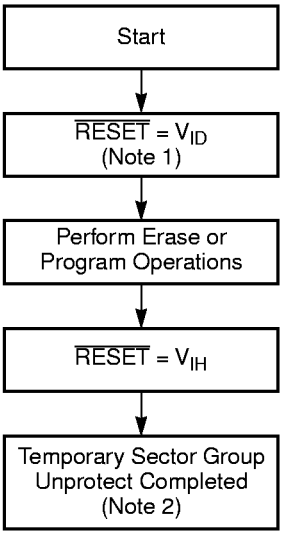
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Description			-85	-90	-120	-150	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note (Note 2))		Min	85	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	40	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	40	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note (Note 2))	Min	0	0	0	0	ns
			Toggle Bit I and $\overline{\text{Data}}$ Polling (Note (Note 2))	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ high to $\overline{WE}$ low)		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ setup Time		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	40	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	7	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note (Note 1))		Typ	1	1	1	1	sec
				Max	8	8	8	8	sec
	t_{VCS}	V_{CC} Setup Time (Note (Note 2))		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID} (Notes (Note 2), (Note 3))		Min	500	500	500	500	ns
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Notes (Note 2), (Note 3))		Min	4	4	4	4	µs
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	500	500	500	ns
	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min	40	40	50	60	ns

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*
3. *These timings are for Temporary Sector Group Unprotect operation.*



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Notes:

1. *All protected sector groups unprotected.*
2. *All previously protected sector groups are protected once again.*

Figure 15. Temporary Sector Group Unprotect Algorithm

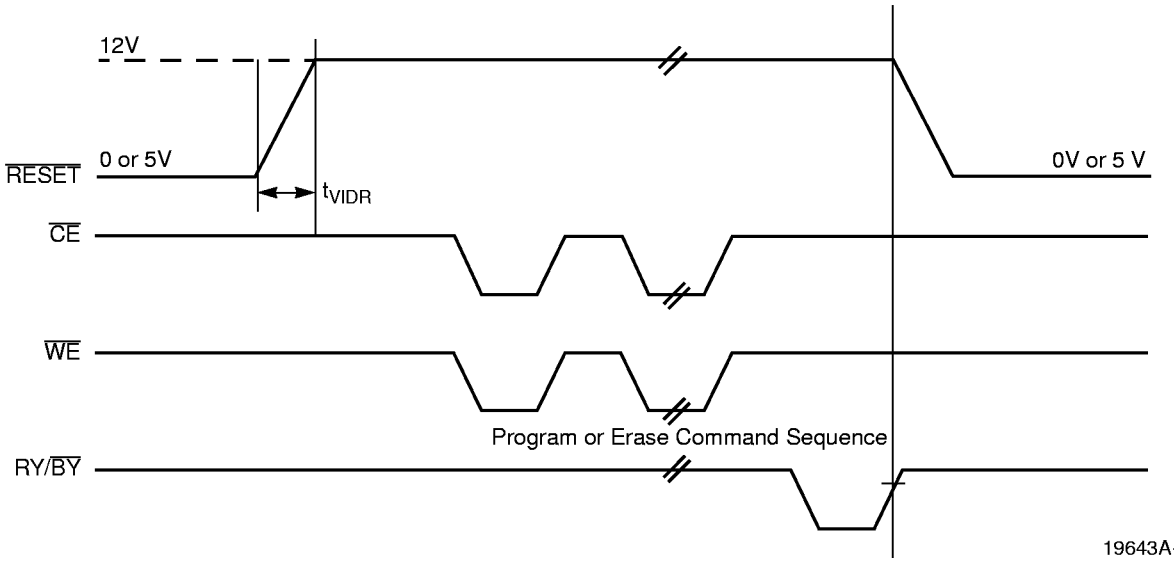

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Figure 16. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS

Write/Erase/Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			-85	-90	-120	-150	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note (Note 2))		Min	85	90	120	150	ns
t_{AVEL}	t_{AS}	Address setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	40	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	40	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note (Note 2))		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note (Note 2))	Min	0	0	0	0	ns
			Toggle Bit I and $\overline{Data}$ Polling (Note (Note 2))	Min	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{CE}$ setup Time		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min	40	45	50	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	7	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note (Note 1))		Typ	1	1	1	1	sec
				Max	8	8	8	8	sec

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Comments
	Typ (Note 1)	Max	Unit	
Sector Erase Time	1.0	8	sec	Excludes 00H programming prior to erasure
Chip Erase Time	16	128	sec	Excludes 00H programming prior to erasure
Byte Programming Time	7	300 (Note 3)	µs	Excludes system-level overhead (Note 4)
Chip Programming Time	7.2	21.6 (Notes 3,5)	sec	Excludes system-level overhead (Note 4)

Notes:

1. *25°C, 5 V V_{CC}, 100,000 cycles.*
2. *Although Embedded Algorithms allow for a longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.*
3. *Under worst case condition of 90°C, 4.5 V V_{CC}, 100,000 cycles.*
4. *System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00H before erasure.*
5. *The Embedded Algorithms allow for 2.5 ms byte program time. DQ5 = "1" only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Programming Times listed above.*

LATCHUP CHARACTERISTICS

Parameter Description	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 Volt, one pin at a time.

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

PSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	10	pF

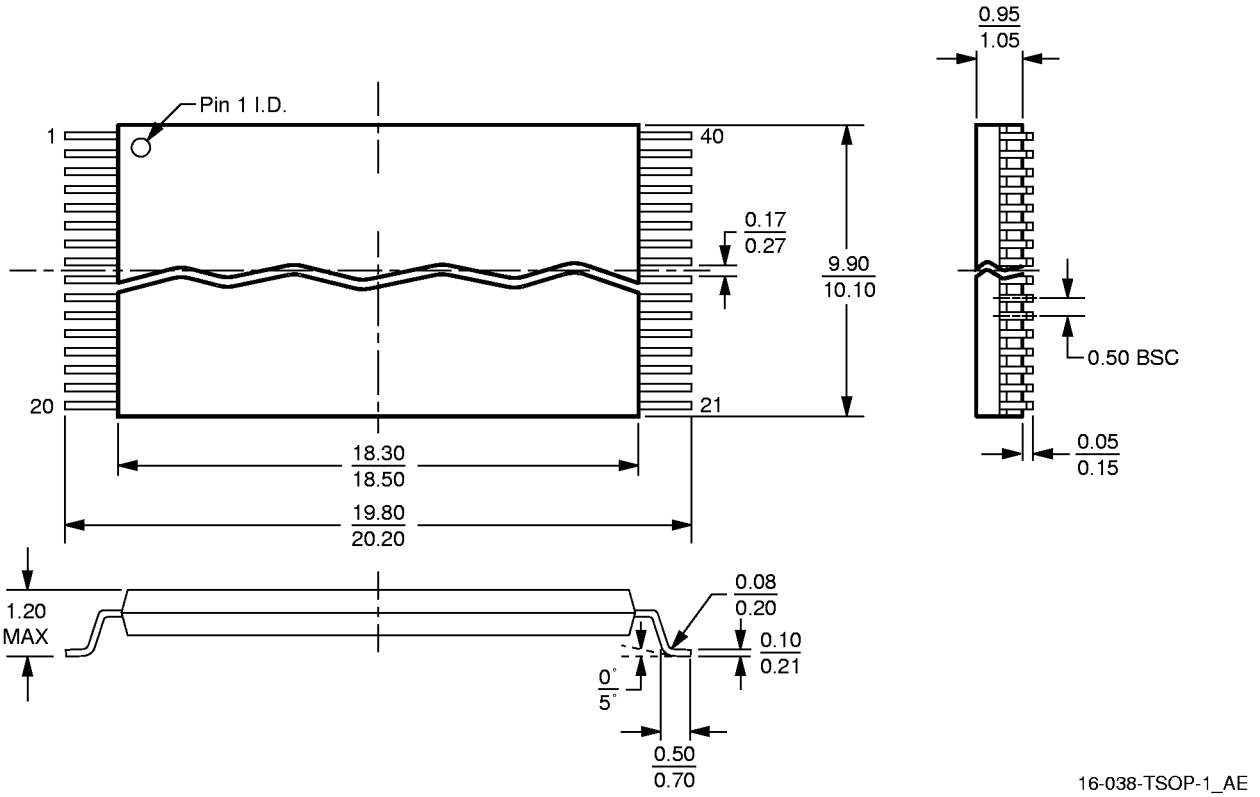
Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

PHYSICAL DIMENSIONS*

TS 040

40-Pin Thin Small Outline Package (measured in millimeters)



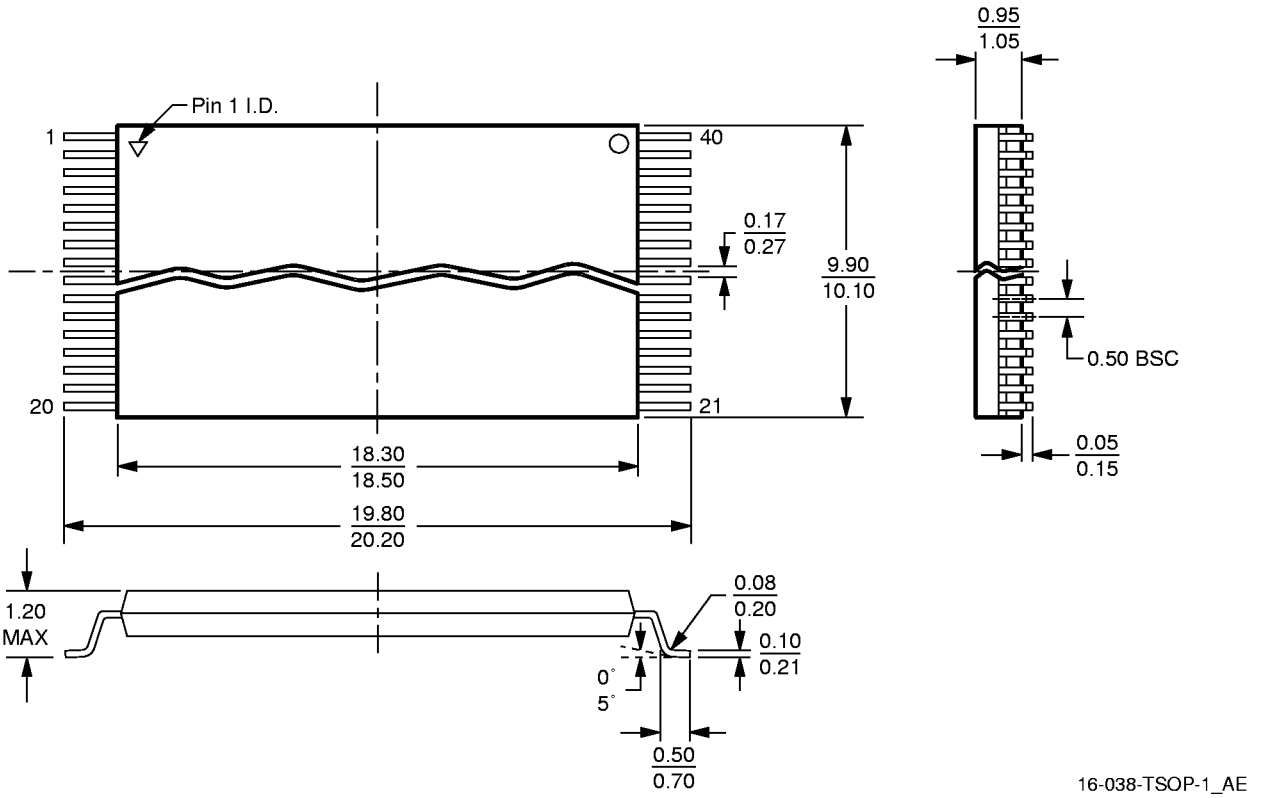
16-038-TSOP-1_AE
TS 040
9-16-96 lv

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS (continued)

TSR040

40-Pin Reversed Thin Small Outline Package (measured in millimeters)



16-038-TSOP-1_AE
TSR040
9-17-96 lv