HARRIS

HM-6516

2K x 8 CMOS RAM

Features

- Low Power Standby ..... 275µW/MHz Max.
- Low Power Operation ..... 55mW/MHz Max.
- Fast Access ..... 120/200ns Max.
- Industry Standard Pinout
- TTL Compatible
- Static Memory Cells
- High Output Drive
- On Chip Address Latches
- Easy Microprocessor Interfacing
- Wide Operating Temperature Ranges:
  - ▸ HM-6516-5 ..... 0°C to +70°C
  - ▸ HM-6516-9 ..... -40°C to +85°C
  - ▸ HM-6516-8 ..... -55°C +125°C

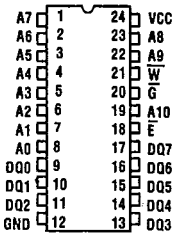
Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6516 is the popular 24 pin, 8 bit wide JEDEC standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMs, EPROMs, and ROMs.

The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Pinouts

TOP VIEW

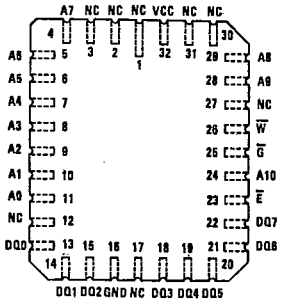


PIN NAMES

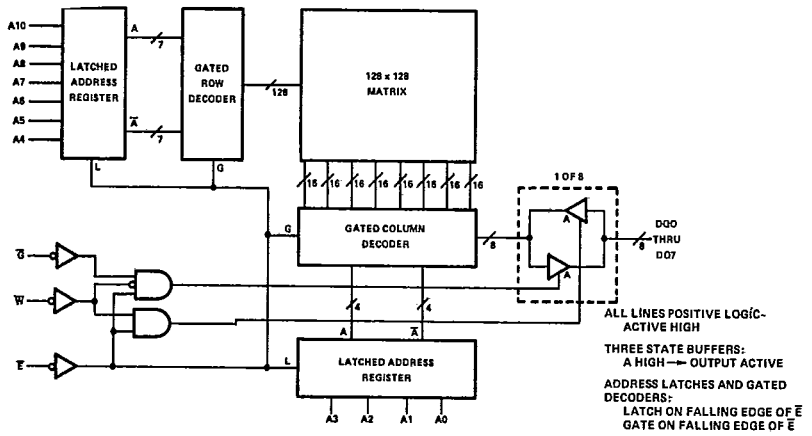
A - Address Input	G - Output Enable
DQ - Data Input/Output	W - Write Enable
E - Chip Enable	NC - No Connect

LCC

TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HM-6516B-8/HM-6516B-9

T-46-23-12

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 8°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 25953 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6516B-9 ..... -40°C to +85°C
HM-6516B-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6516B-9 -40°C to +85°C
T_A = HM-6516B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	10	mA	f = 1MHz, IO = 0, $\overline{G}$ = VCC, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	25	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.4	VCC +0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

T-46-23-12

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6516B-9 -40°C to +85°C
T_A = HM-6516B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	120	ns	(Notes 1, 4)
(3) TELQX	Chip Select Output Enable Time	10	-	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(5) TEHQZ	Chip Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(6) TGLQV	Output Enable Output Valid Time	-	80	ns	(Notes 1, 4)
(7) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(9) TELEH	Chip Enable Pulse Negative Width	120	-	ns	(Notes 1, 4)
(10) TEHEL	Chip Enable Pulse Positive Width	50	-	ns	(Notes 1, 4)
(11) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(12) TELAX	Address Hold Time	30	-	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	120	-	ns	(Notes 1, 4)
(14) TWLEH	Write Enable Pulse Setup Time	120	-	ns	(Notes 1, 4)
(15) TELWH	Write Enable Pulse Hold Time	120	-	ns	(Notes 1, 4)
(16) TDVWH	Data Setup Time	50	-	ns	(Notes 1, 4)
(17) TWHDX	Data Hold Time	10	-	ns	(Notes 1, 4)
(18) TWLDV	Write Data Delay Time	50	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	170	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 8°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 25953 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6516-9 ..... -40°C to +85°C
HM-6516-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6516-9 -40°C to +85°C
T_A = HM-6516-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	100	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	10	mA	f = 1MHz, IO = 0, $\overline{G}$ = VCC, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	50	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.4	VCC +0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6516-9 -40°C to +85°C
T_A = HM-6516-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	200	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	200	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(5) TEHQZ	Chip Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(6) TGLQV	Output Enable Output Valid Time	-	80	ns	(Notes 1, 4)
(7) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(9) TELEH	Chip Enable Pulse Negative Width	200	-	ns	(Notes 1, 4)
(10) TEHEL	Chip Enable Pulse Positive Width	80	-	ns	(Notes 1, 4)
(11) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(12) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	200	-	ns	(Notes 1, 4)
(14) TWLEH	Write Enable Pulse Setup Time	200	-	ns	(Notes 1, 4)
(15) TELWH	Write Enable Pulse Hold Time	200	-	ns	(Notes 1, 4)
(16) TDVWH	Data Setup Time	80	-	ns	(Notes 1, 4)
(17) TWHDX	Data Hold Time	10	-	ns	(Notes 1, 4)
(18) TWLDV	Write Data Delay Time	80	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	280	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 8°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 47°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 25953 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6516-5 ..... 0°C to +70°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6516-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	500	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	10	mA	f = 1MHz, IO = 0, $\overline{G}$ = VCC, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	250	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-5.0	+5.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.4	VCC +0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

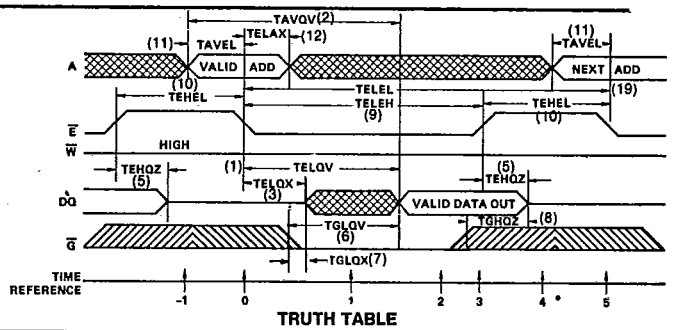
NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications V_{CC} = 5V ± 10%; T_A = HM-6516-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	200	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	200	ns	(Notes 1, 4)
(3) TELQX	Chip Select Output Enable Time	10	-	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(5) TEHQZ	Chip Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(6) TGLQV	Output Enable Output Valid Time	-	80	ns	(Notes 1, 4)
(7) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(8) TGHQZ	Output Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(9) TELEH	Chip Enable Pulse Negative Width	200	-	ns	(Notes 1, 4)
(10) TEHEL	Chip Enable Pulse Positive Width	80	-	ns	(Notes 1, 4)
(11) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(12) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(13) TWLWH	Write Enable Pulse Width	200	-	ns	(Notes 1, 4)
(14) TWLEH	Write Enable Pulse Setup Time	200	-	ns	(Notes 1, 4)
(15) TELWH	Write Enable Pulse Hold Time	200	-	ns	(Notes 1, 4)
(16) TDVWH	Data Setup Time	80	-	ns	(Notes 1, 4)
(17) TWHDX	Data Hold Time	10	-	ns	(Notes 1, 4)
(18) TWLDV	Write Data Delay Time	80	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	280	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle

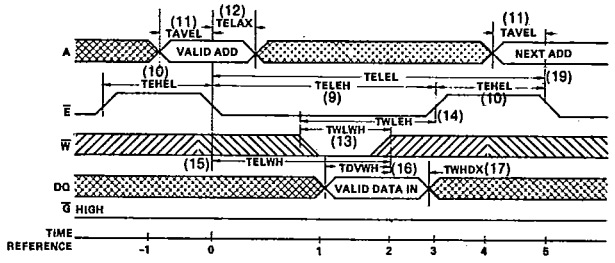


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	X	V	Z	Cycle Begins, Addresses are Latched
1	L	H	L	X	X	Output Enabled
2	L	H	L	X	V	Output Valid
3	↑	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	H	X	X	Memory Disabled
0	↓	X	H	V	X	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Write Period Begins
2	L	↑	H	X	V	Data In is Written
3	↑	H	H	X	X	Write Completed
4	H	X	H	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	H	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.