HARRIS

HM-6504

4096 x 1 CMOS RAM

Features

- Low Power Standby ..... 125µW Max.
- Low Power Operation ..... 35mW/MHz Max.
- Extremely Low Speed-Power Product
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- Three-State Output
- Standard JEDEC Pinout
- Fast Access Time ..... 120/200ns Max.
- Wide Operating Temperature Ranges:
  - ▸ HM-6504-9 ..... -40°C to +85°C
  - ▸ HM-6504-8 ..... -55°C to +125°C
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs—No Pull Up or Pull Down Resistors Required

Description

The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

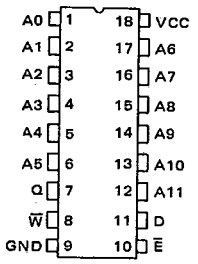
On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors. The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

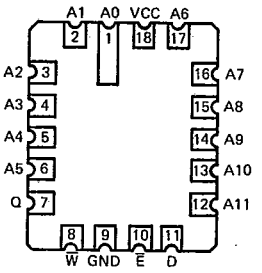
Pinouts

TOP VIEW



LCC

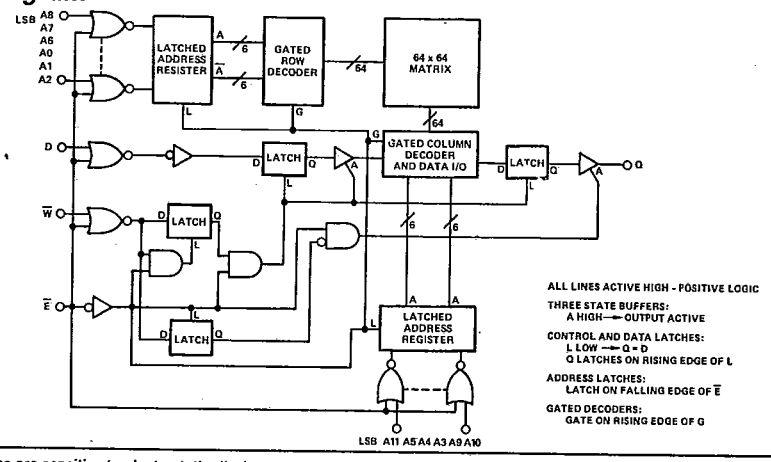
TOP VIEW



PIN NAMES

$\overline{A}$ — Address Input D — Data Input
$\overline{E}$ — Chip Enable Q — Data Output
$\overline{W}$ — Write Enable

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 7000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6504S-8 ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504S-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	25	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504S-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	120	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	20	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	70	-	ns	(Notes 1, 4)
(11) TWLEL	Early Write Pulse Setup Time	0	-	ns	(Notes 1, 4)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	ns	(Notes 2, 4)
(13) TELWH	Early Write Pulse Hold Time	40	-	ns	(Notes 1, 4)
(14) TDVWL	Data Setup Time	0	-	ns	(Notes 1, 4)
(15) TDVEL	Early Write Data Setup Time	0	-	ns	(Notes 1, 4)
(16) TWLDX	Data Hold Time	25	-	ns	(Notes 1, 4)
(17) TELDX	Early Write Data Hold Time	25	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	170	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 7000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6504S-9 ..... -40°C to +85°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	25	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	15	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	120	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	20	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	70	-	ns	(Notes 1, 4)
(11) TWLEL	Early Write Pulse Setup Time	0	-	ns	(Notes 1, 4)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	ns	(Notes 2, 4)
(13) TELWH	Early Write Pulse Hold Time	40	-	ns	(Notes 1, 4)
(14) TDVWL	Data Setup Time	0	-	ns	(Notes 1, 4)
(15) TDVEL	Early Write Data Setup Time	0	-	ns	(Notes 1, 4)
(16) TWLDX	Data Hold Time	25	-	ns	(Notes 1, 4)
(17) TELDX	Early Write Data Hold Time	25	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	170	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 7000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6504B-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6504B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	25	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	200	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	220	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	200	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	90	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	60	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	150	-	ns	(Notes 1, 4)
(11) TWLEL	Early Write Pulse Setup Time	0	-	ns	(Notes 1, 4)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	ns	(Notes 2, 4)
(13) TELWH	Early Write Pulse Hold Time	60	-	ns	(Notes 1, 4)
(14) TDVWL	Data Setup Time	0	-	ns	(Notes 1, 4)
(15) TDVEL	Early Write Data Setup Time	0	-	ns	(Notes 1, 4)
(16) TWLDX	Data Hold Time	60	-	ns	(Notes 1, 4)
(17) TELDX	Early Write Data Hold Time	60	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	290	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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Specifications HM-6504B-9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 7000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6504B-9 ..... -40°C to +85°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	25	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	15	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	200	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	220	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	200	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	90	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	60	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	150	-	ns	(Notes 1, 4)
(11) TWLEL	Early Write Pulse Setup Time	0	-	ns	(Notes 1, 4)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	ns	(Notes 2, 4)
(13) TELWH	Early Write Pulse Hold Time	60	-	ns	(Notes 1, 4)
(14) TDVWL	Data Setup Time	0	-	ns	(Notes 1, 4)
(15) TDVEL	Early Write Data Setup Time	0	-	ns	(Notes 1, 4)
(16) TWLDX	Data Hold Time	60	-	ns	(Notes 1, 4)
(17) TELDX	Early Write Data Hold Time	60	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	290	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Specifications HM-6504-8

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 7000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6504-8 ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	25	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

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A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	320	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	100	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	120	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	80	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	200	-	ns	(Notes 1, 4)
(11) TWLEL	Early Write Pulse Setup Time	0	-	ns	(Notes 1, 4)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	ns	(Note 2, 4)
(13) TELWH	Early Write Pulse Hold Time	80	-	ns	(Notes 1, 4)
(14) TDVWL	Data Setup Time	0	-	ns	(Notes 1, 4)
(15) TDVEL	Early Write Data Setup Time	0	-	ns	(Notes 1, 4)
(16) TWLDX	Data Hold Time	80	-	ns	(Notes 1, 4)
(17) TELDX	Early Write Data Hold Time	80	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	420	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Specifications HM-6504-9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 7000 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6504-9 ..... -40°C to +85°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	25	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	15	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

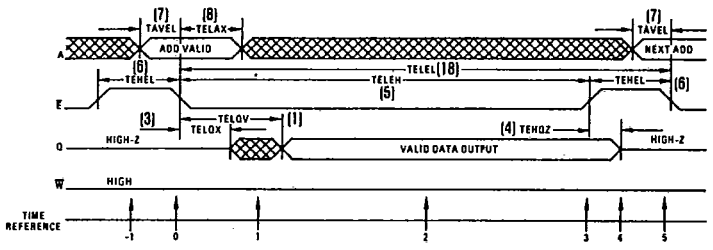
NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6504-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	320	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	100	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1,4)
(6) TEHEL	Chip Enable Pulse Positive Width	120	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	80	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	200	-	ns	(Notes 1, 4)
(11) TWLEL	Early Write Pulse Setup Time	0	-	ns	(Notes 1, 4)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	ns	(Notes 2, 4)
(13) TELWH	Early Write Pulse Hold Time	80	-	ns	(Notes 1, 4)
(14) TDVWL	Data Setup Time	0	-	ns	(Notes 1, 4)
(15) TDVEL	Early Write Data Setup Time	0	-	ns	(Notes 1, 4)
(16) TWLDX	Data Hold Time	80	-	ns	(Notes 1, 4)
(17) TELDX	Early Write Data Hold Time	80	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	420	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle

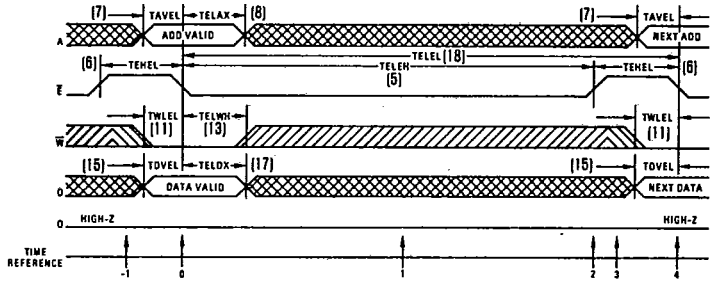


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	↑	H	X	V	Output Valid
3	↓	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as - 1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

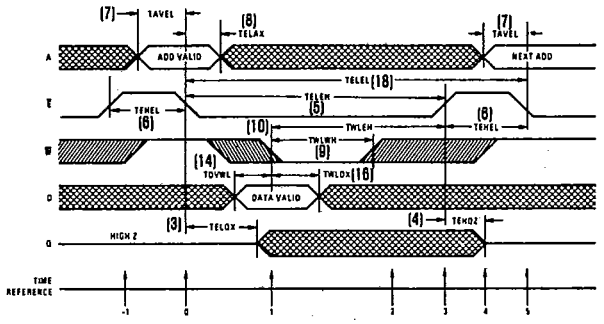


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	INPUTS D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write In Progress Internally
2	↑	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as - 1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Late Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins Addresses are Latched
1	L	↓	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write In Progress Internally
3	↑	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.