Preliminary

64Mb Synchronous DRAM

Features

- High Performance:

		-80 CL=3	-10 CL=3	-12 CL=3	Units
f_{CK}	Clock Frequency	125	100	83	MHz
t_{CK}	Clock Cycle	8	10	12	ns
t_{AC}	Clock Access Time	6	7	8	ns

- Single Pulsed $\overline{RAS}$ Interface
- Fully Synchronous to Positive Clock Edge
- Four Banks controlled by A12/A13 (Bank Select)
- Programmable CAS Latency: 2,3,4
- Programmable Burst Length: 1,2,4,8,full-page
- Programmable Wrap Sequence: Sequential or Interleave
- Multiple Burst Read with Single Write Option
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write control (x4,x8)
- Dual Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- 4096 refresh cycles/64ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3V ± 0.3V Power Supply
- LVTTL compatible
- Package: 54 pin 400 mil TSOP-Type II

Description

The IBM0364404C, IBM0364804C, and IBM0364164C are four bank Synchronous DRAMs organized as 4Mbit x 4 I/O x 4 Bank, 2Mbit x 8 I/O x 4 Bank, and 1Mbit x 16 I/O x 4 Bank, respectively. These synchronous devices achieve high speed data transfer rates of up to 125MHz by employing a pipeline chip architecture that synchronizes the output data to a system clock. The chip is fabricated with IBM's advanced 64Mbit single transistor CMOS DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address and data input/output (I/O or DQ) circuits are synchronized with the positive edge of an externally supplied clock.

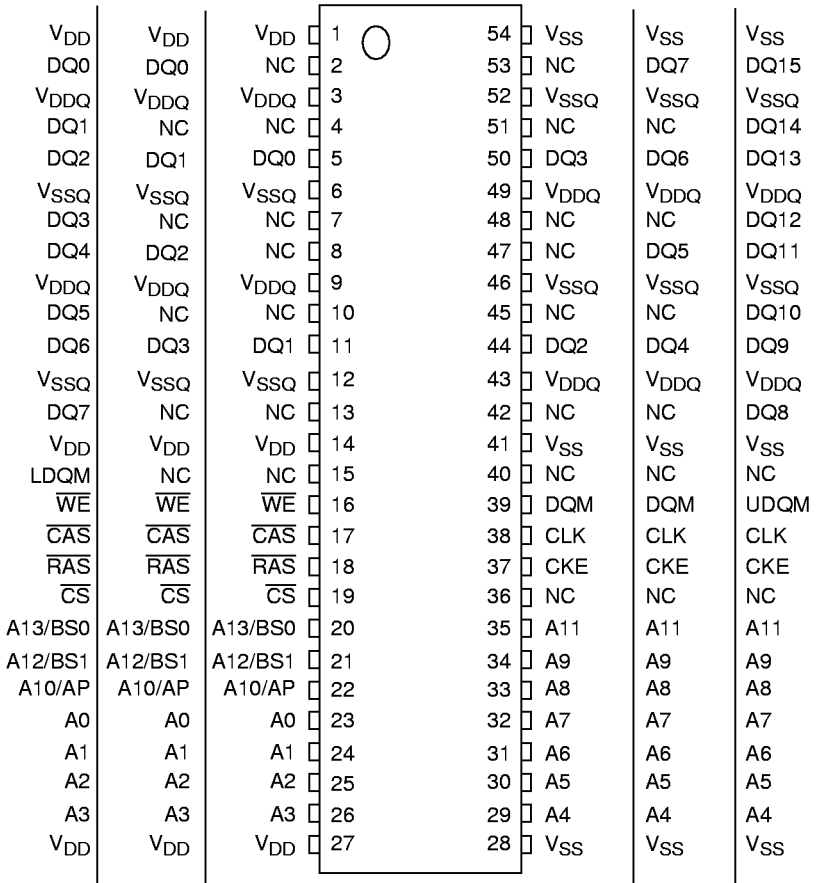
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{CS}$ are pulsed signals which are examined at the positive edge of each externally applied clock (CLK). Internal chip operating modes are defined by combinations of these signals and a command decoder initiates the necessary timings for each operation. A fourteen bit address bus accepts address data in the conventional $\overline{RAS}$/$\overline{CAS}$ multiplexing style. Twelve row addresses (A0-A11) and two bank select addresses (A12, A13) are strobed with $\overline{RAS}$. Ten column addresses (A0-A9) plus bank select addresses are strobed with $\overline{CAS}$. Column address A9 is dropped on the x8 device and column addresses A8 and A9 are dropped on the x16 device.

Prior to any access operation, the $\overline{CAS}$ latency, burst length, and burst sequence must be programmed into the device by address inputs A0-A9 during a mode register set cycle. In addition, it is possible to program a multiple burst sequence with single write cycle for write through cache operation.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 125MHz is possible depending on burst length, $\overline{CAS}$ latency, and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3V ± 0.3V power supply and are available in 400mil TSOP Type II packages.

Pin Assignments (Top View)



54-pin Plastic TSOP(II) 400 mil

4Mbit x 4 I/O x 4 Bank

IBM0364404CT3

2Mbit x 8 I/O x 4 Bank

IBM0364804CT3

1Mbit x 16 I/O x 4 Bank

IBM0364164CT3

Pin Description

CLK	Clock Input	**DQ0-DQ15**	Data Input/Output
CKE	Clock Enable	**DQM, LDQM, UDQM**	Data Mask
$\overline{CS}$	Chip Select	**VDD**	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	**VSS**	Ground
$\overline{CAS}$	Column Address Strobe	**VDDQ**	Power for DQs (+3.3V)
$\overline{WE}$	Write Enable	**VSSQ**	Ground for DQs
BS1, BS0 (A12, A13)	Bank Select	**NC**	No Connection
A0 - A11	Address Inputs	—	—

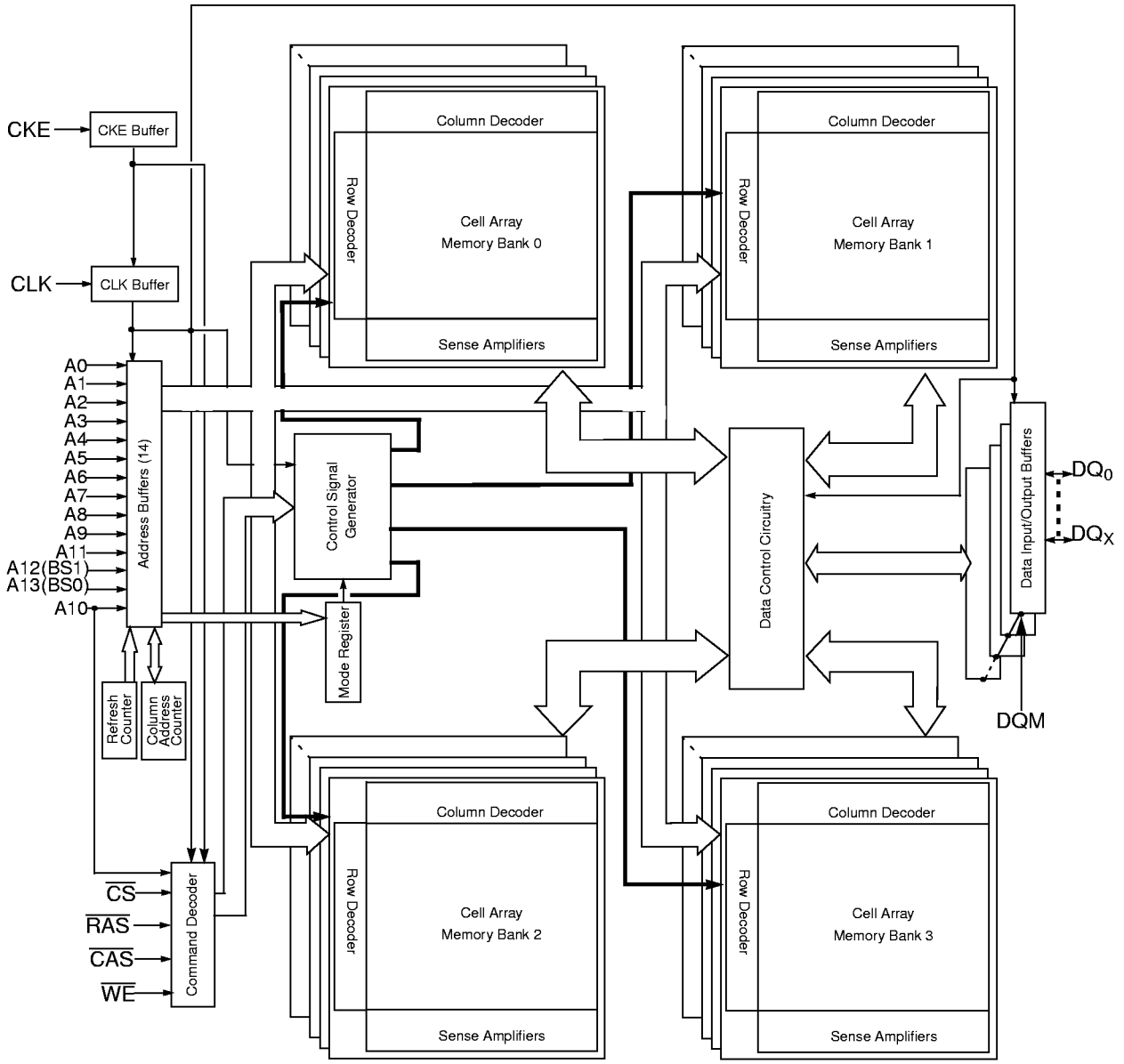
Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BS1, BS0 (A12, A13)	Input	Level	—	Selects which bank is to be active.
A0 - A11	Input	Level	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. A10 is used to invoke auto-precharge operation at the end of the burst read or write cycle. If A10 is high, auto-precharge is selected and BS0, BS1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with BS0, BS1 to control which bank(s) to precharge. If A10 is high, all banks will be precharged regardless of the state of BS. If A10 is low, then BS0 and BS1 are used to define which bank to precharge.
DQ0 - DQ15	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	Pulse	Active Low	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VDD, V_{SS}	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Ordering Information

Part Number	CAS Latencies	Power Supply	Clock Cycle	Package	Org.
IBM0364404CT3-80	2,3,4	3.3V	8ns	400mil Type II TSOP-54	x4
IBM0364404CT3-10	2,3,4	3.3V	10ns	400mil Type II TSOP-54	x4
IBM0364404CT3-12	2,3,4	3.3V	12ns	400mil Type II TSOP-54	x4
IBM0364804CT3-80	2,3,4	3.3V	8ns	400mil Type II TSOP-54	x8
IBM0364804CT3-10	2,3,4	3.3V	10ns	400mil Type II TSOP-54	x8
IBM0364804CT3-12	2,3,4	3.3V	12ns	400mil Type II TSOP-54	x8
IBM0364164CT3-80	2,3,4	3.3V	8ns	400mil Type II TSOP-54	x16
IBM0364164CT3-10	2,3,4	3.3V	10ns	400mil Type II TSOP-54	x16
IBM0364164CT3-12	2,3,4	3.3V	12ns	400mil Type II TSOP-54	x16

Block Diagram



Cell Array for 4Mb x 4 DQ x 4 Bank (per Bank): 4096 Row x 1024 Col x 4 DQ (DQ0-DQ3).
Cell Array for 2Mb x 8 DQ x 4 Bank (per Bank): 4096 Row x 512 Col x 8 DQ (DQ0-DQ7).
Cell Array for 1Mb x 16 DQ x 4 Bank (per Bank): 4096 Row x 256 Col x 16 DQ (DQ0-DQ15).

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs.

Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200µs is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once both banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

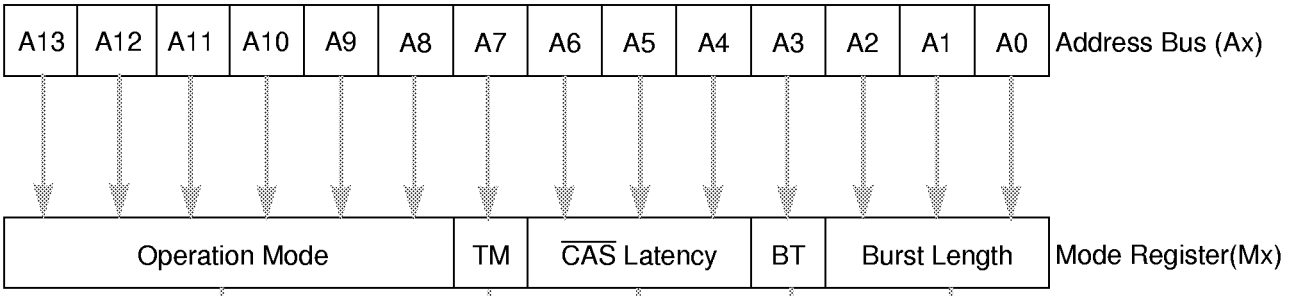
For application flexibility, $\overline{CAS}$ latency, burst length, burst sequence, and operation type are user defined variables and must be programmed into the SDRAM Mode Register with a single Mode Register Set Command. Any content of the Mode Register can be altered by re-executing the Mode Register Set Command. If the user chooses to modify only a subset of the Mode Register variables, all four variables must be redefined when the Mode Register Set Command is issued.

After initial power up, the Mode Register Set Command must be issued before read or write cycles may begin. Both banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ and $\overline{WE}$ at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to t_{RSC} has elapsed.

$\overline{CAS}$ Latency

The $\overline{CAS}$ latency is a parameter that is used to define the delay from when a Read Command is registered on a rising clock edge to when the data from that Read Command becomes available at the outputs. The $\overline{CAS}$ latency is expressed in terms of clock cycles and can have a value of 2, 3, or 4 cycles. The value of the $\overline{CAS}$ latency is determined by the speed grade of the device and the clock frequency that is used in the application. A table showing the relationship between the $\overline{CAS}$ latency, speed grade, and clock frequency appears in the Electrical Characteristics section of this document. Once the appropriate $\overline{CAS}$ latency has been selected it must be programmed into the mode register after power up, for an explanation of this procedure see Programming the Mode Register in the previous section.

Mode Register Operation (Address Input For Mode Set)



Test Mode

M7	Type
0	Normal
1	Test Mode

Burst Type

M3	Type
0	Sequential
1	Interleave

Operation Mode

M13	M12	M11	M10	M9	M8	Mode
0	0	0	0	0	0	Normal
0	0	0	0	1	0	Multiple Burst with Single Write

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). There are three parameters that define how the burst mode will operate. These parameters include burst sequence, burst length, and operation mode. The burst sequence and burst length are programmable, and are determined by address bits A0 - A3 during the Mode Register Set command. Operation mode is also programmable and is set by address bits A8 - A13.

The burst type is used to define the order in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequences are supported, sequential and interleaved. See Table.

The burst length controls the number of bits that will be output after a Read Command, or the number of bits to be input after a Write Command. The burst length can be programmed to have values of 1, 2, 4, 8 or full page (actual page length is dependent on organization: x4, x8, or x16). Full page burst operation is only possible using the sequential burst type.

Burst operation mode can be normal operation or multiple burst with single write operation. Normal operation implies that the device will perform burst operations on both read and write cycles until the desired burst length is satisfied. Multiple burst with single write operation was added to support Write Through Cache operation. Here, the programmed burst length only applies to read cycles. All write cycles are single write operations when this mode is selected.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
2	x x 0	0, 1	0, 1
	x x 1	1, 0	1, 0
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
Full Page (Note)	n n n	Cn, Cn+1, Cn+2, ...	Not Supported

Note: Page length is a function of I/O organization and column addressing.

X4 organization (CA0-CA9); Page Length = 1024 bits

X8 organization (CA0-CA8); Page Length = 512 bits

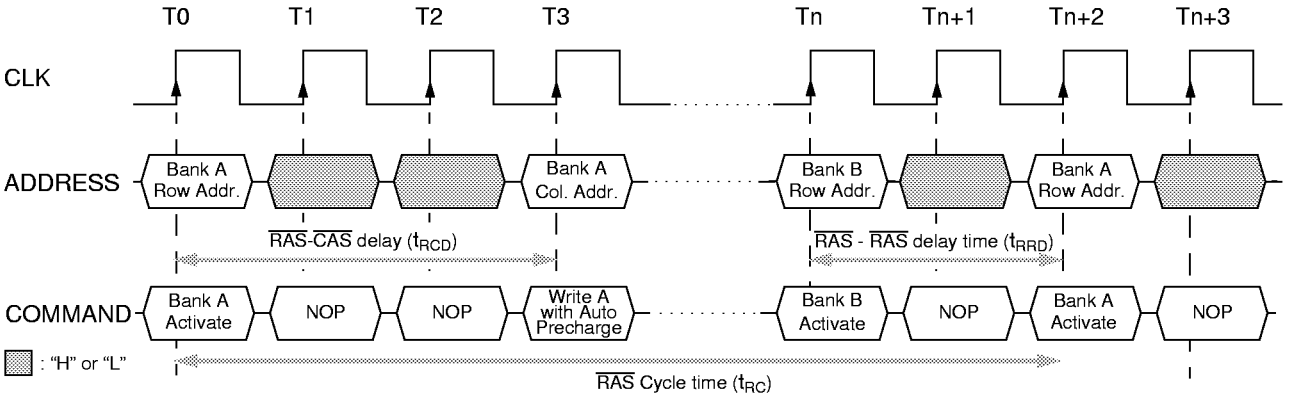
X16 organization (CA0-CA7); Page Length = 256 bits

Bank Activate Command

In relation to the operation of a fast page mode DRAM, the Bank Activate command corresponds to a falling $\overline{RAS}$ signal. The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank select address A12 - A13 is used to select the desired bank. The row address A0 - A11 is used to determine which row to activate in the selected bank.

The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must meet or exceed the $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}). Once a bank has been activated it must be pre-charged before another Bank Activate command can be applied to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD}). The maximum time that each bank can be held active is specified as $t_{RAS(max)}$.

Bank Activate Command Cycle ($\overline{CAS}$ Latency = 3)



Bank Select

The Bank Select inputs, BS0 and BS1, determine the bank to be used during a Bank Activate, Precharge, Read, or Write operation.

Bank Selection Bits

BS0	BS1	Bank
0	0	Bank0
0	1	Bank1
1	0	Bank2
1	1	Bank3

Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high and $\overline{CAS}$ low at the clock's rising edge after the necessary $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}). $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high), or a write operation ($\overline{WE}$ low). The address inputs determine the starting column address.

The SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 125MHz. The number of serial data bits for each access is equal to the burst length, which is programmed into the Mode Register. If the burst length is full page, data is repeatedly read out or written until a Burst Stop or Precharge Command is issued.

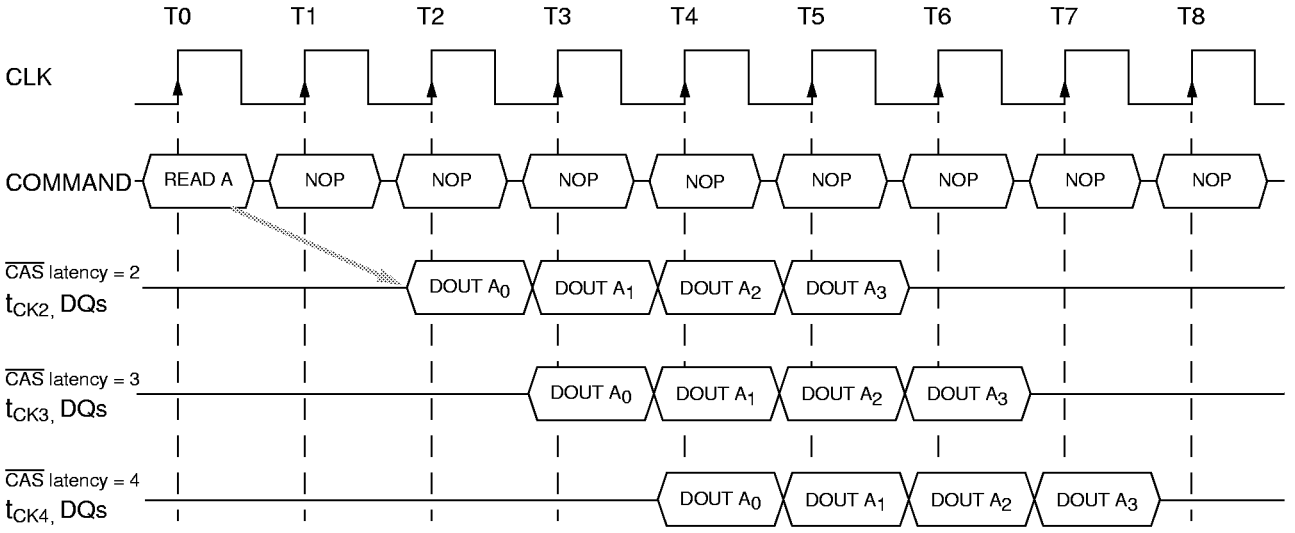
Similar to Page Mode of conventional DRAMs, a read or write cycle can not begin until the sense amplifiers latch the selected row address information. The refresh period (t_{REF}) is what limits the number of random column accesses to an activated bank. A new burst access can be done even before the previous burst ends. The ability to interrupt a burst operation at every clock cycle is supported; this is referred to as the 1-N rule. When the previous burst is interrupted by another Read or Write Command, the remaining addresses are overridden by the new address.

Precharging an active bank after each read or write operation is not necessary providing the same row is to be accessed again. To perform a read or write cycle to a different row within an activated bank, the bank must be precharged and a new Bank Activate command must be issued. When more than one bank is activated, interleaved (ping pong) bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, fast and seamless data access operation among many different pages can be realized. When multiple banks are activated, column to column interleave operation can be done between different pages. Finally, Read or Write Commands can be issued to the same bank or between active banks on every clock cycle.

Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst, the Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8, full page). The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the $\overline{CAS}$ latency that is set in the Mode Register.

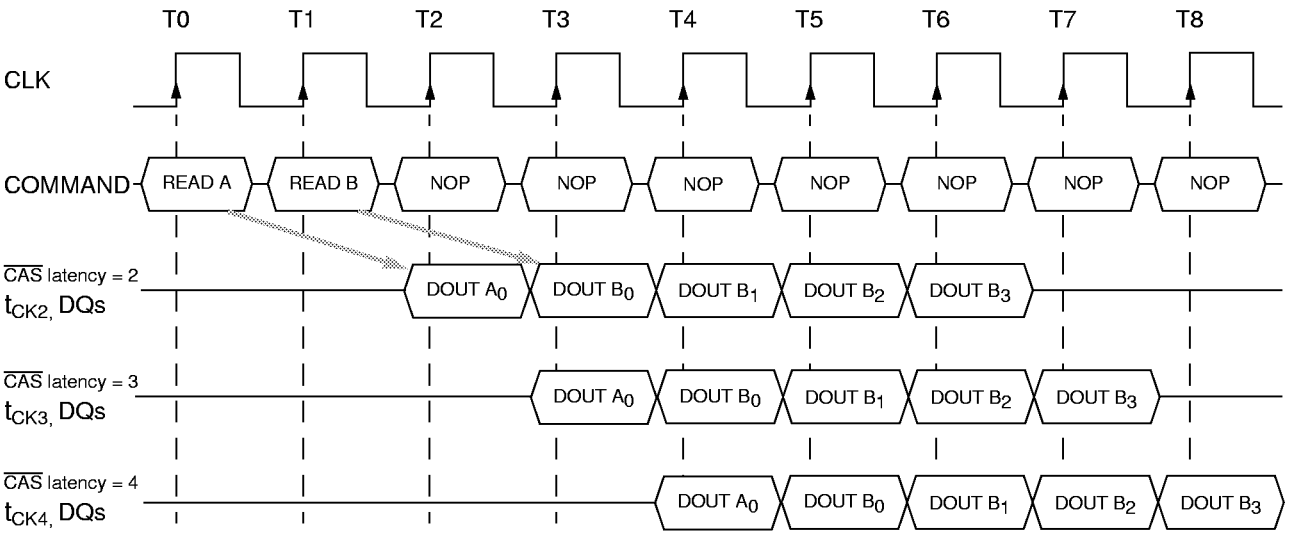
Burst Read Operation (Burst Length = 4, CAS latency = 2, 3, 4)



Read Interrupted by a Read

A Burst Read may be interrupted before completion of the burst by another Read Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read Command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read Command is satisfied, at this point the data from the interrupting Read Command appears.

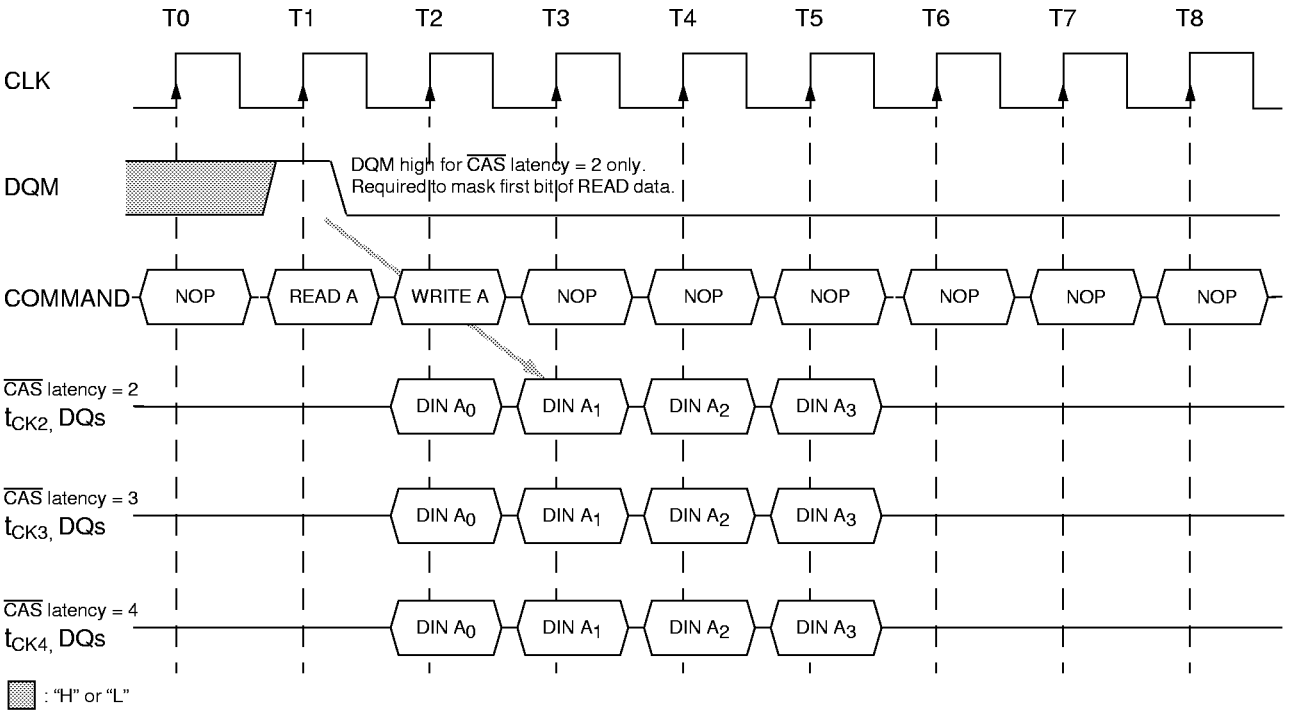
Read Interrupted by a Read (Burst Length = 4, CAS latency = 2, 3, 4)



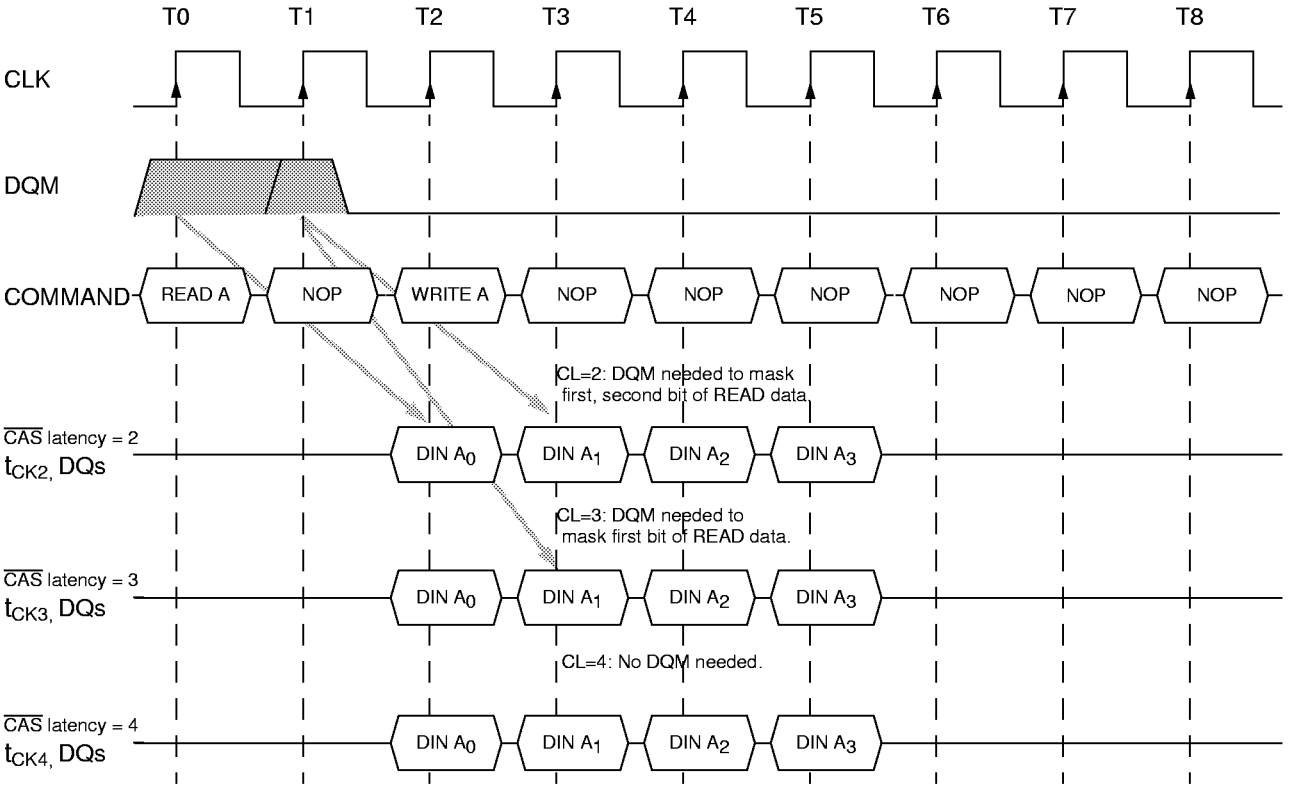
Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus.

Minimum Read to Write Interval (Burst Length = 4, CAS latency = 2, 3, 4)



Non-Minimum Read to Write Interval (Burst Length = 4, CAS latency = 2, 3, 4)



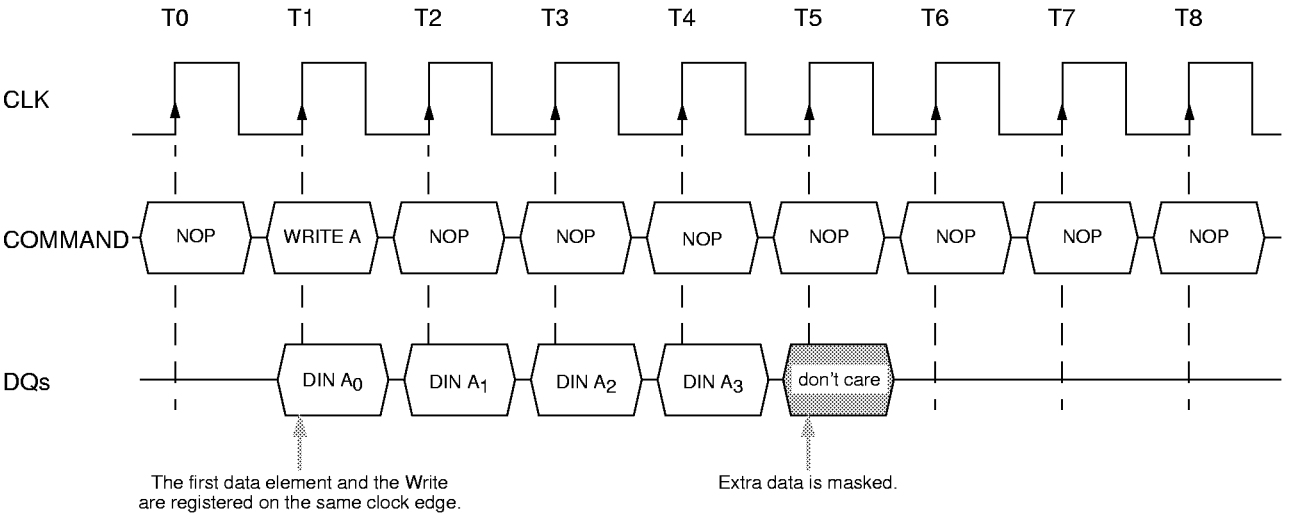
: DQM high for $\overline{CAS}$ latency = 2

: DQM high for $\overline{CAS}$ latency = 3

Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. There is no $\overline{CAS}$ latency required for burst write cycles. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

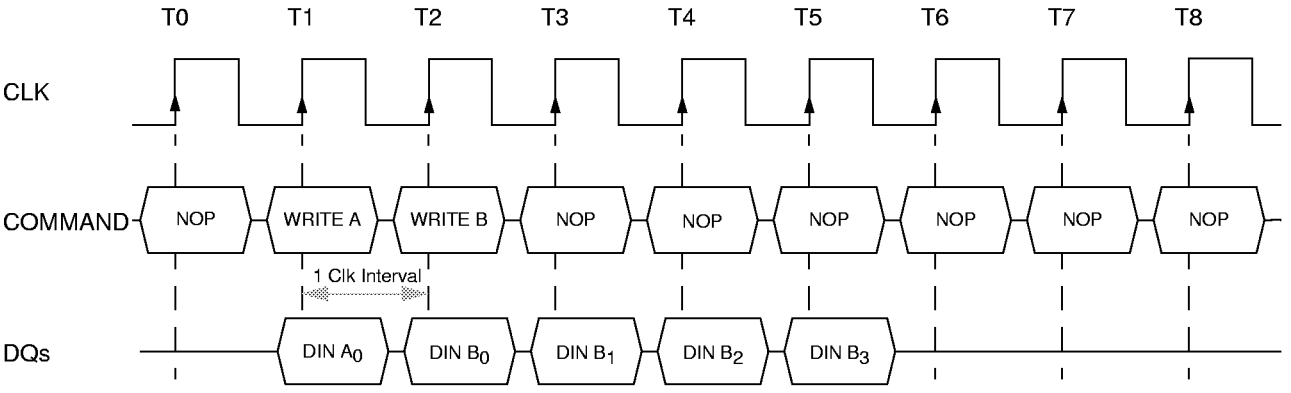
Burst Write Operation (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, or 4)



Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

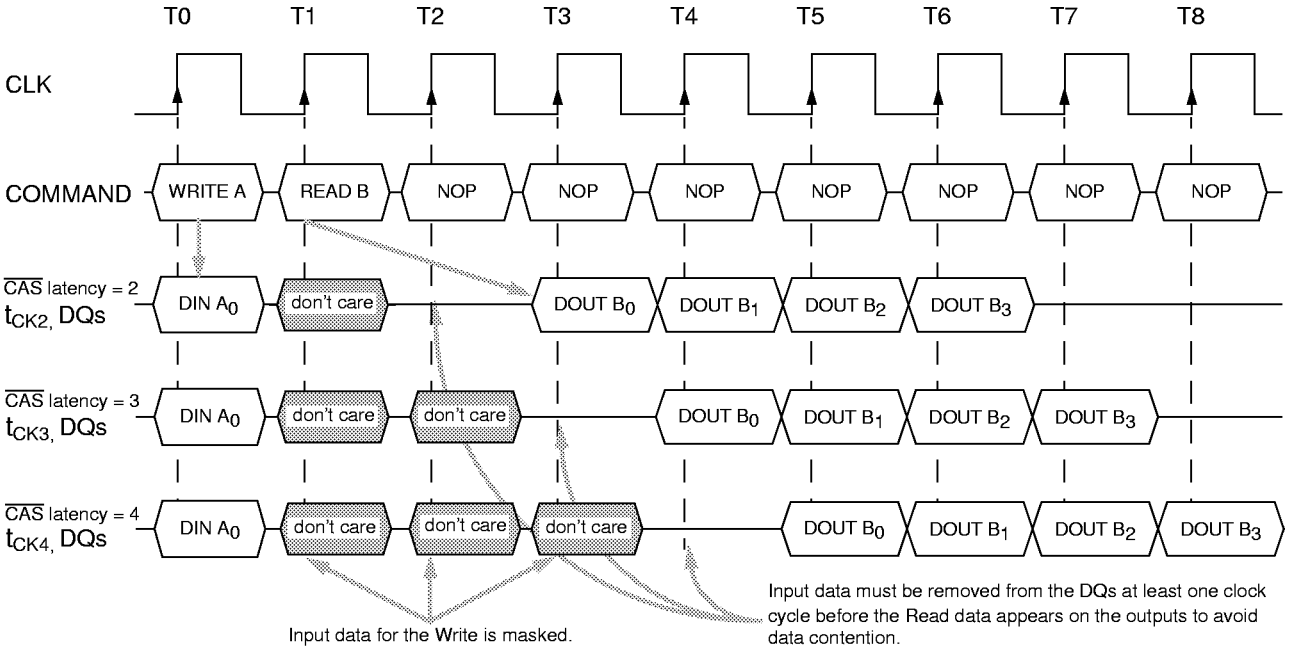
Write Interrupted by a Write (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, or 4)



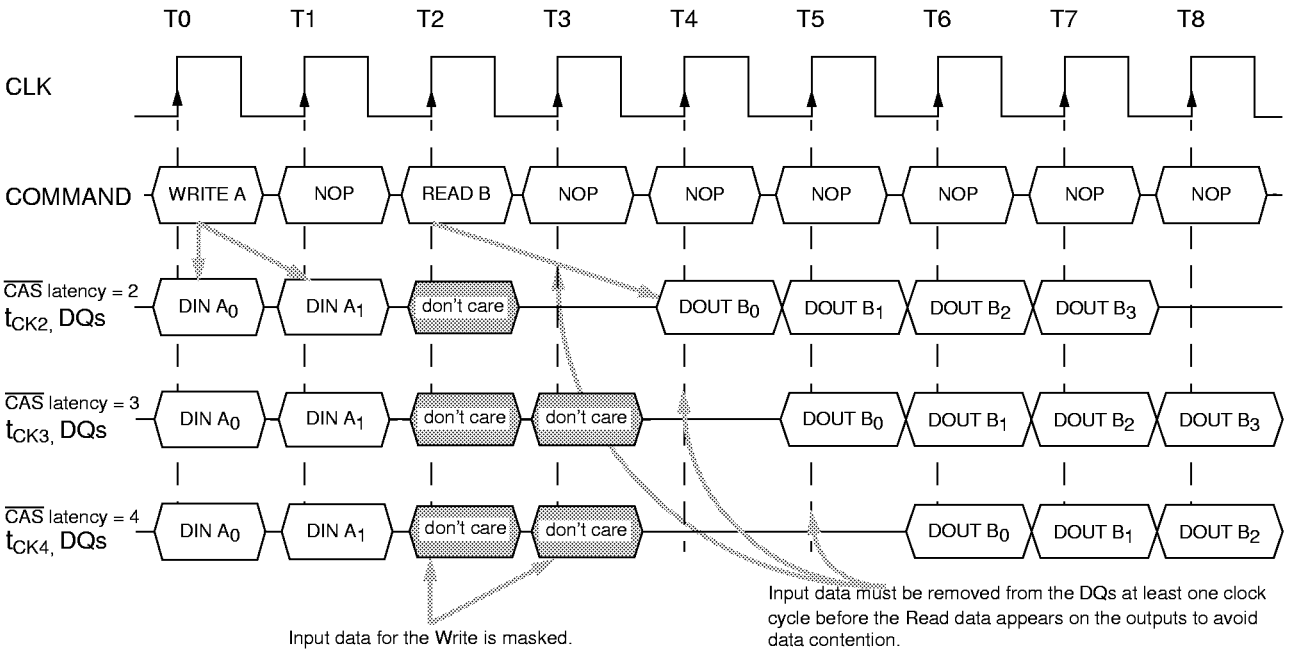
Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is registered. The DQs must be in the high impedance state at least one cycle before the interrupting read data appears on the outputs to avoid data contention. When the Read Command is registered, any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Read Command is initiated will actually be written to the memory.

Minimum Write to Read Interval (Burst Length = 4, CAS latency = 2, 3, 4)



Non-Minimum Write to Read Interval (Burst Length = 4, CAS latency = 2, 3, 4)



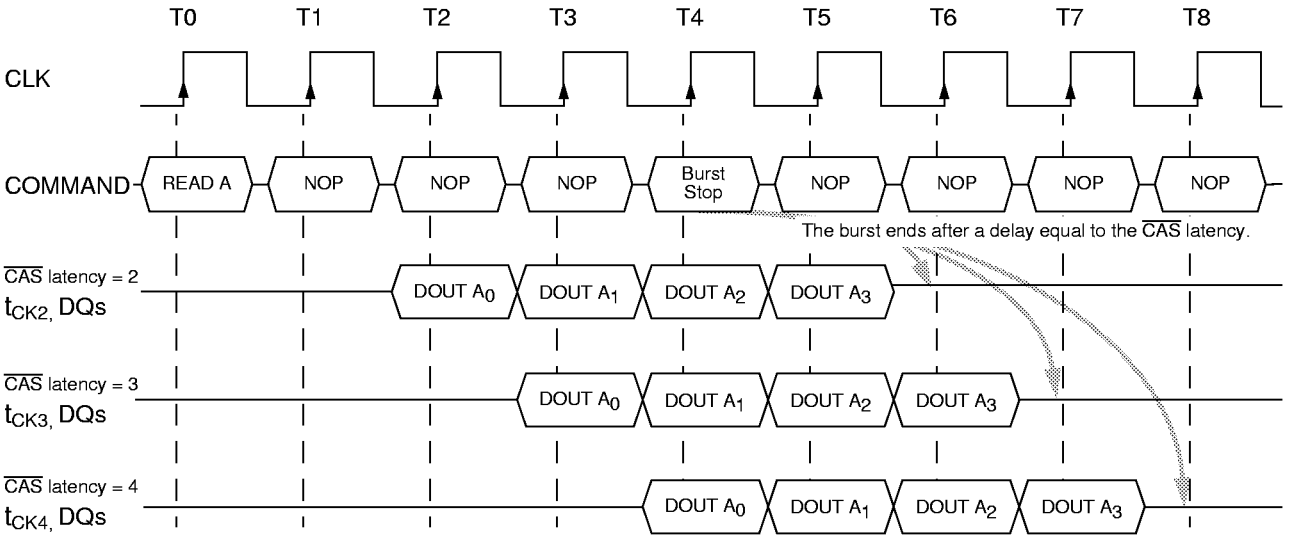
Burst Stop Command

Once a burst read or write operation has been initiated, there exist several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation or using a Precharge Command to interrupt a burst cycle and close the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention.

If the burst length is full page, the Burst Stop Command may also be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock.

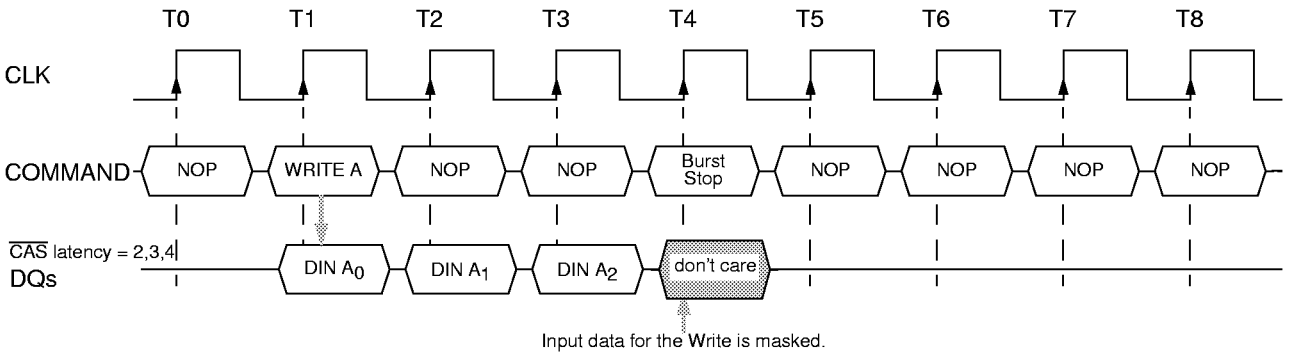
When using the Burst Stop Command during a burst read cycle, the data DQs go to a high impedance state after a delay which is equal to the $\overline{CAS}$ Latency set in the Mode Register.

Termination of a Burst Read Operation (Burst Length = Full Page, $\overline{CAS}$ Latency = 2, 3, 4)



If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Termination of a Burst Write Operation (Burst Length = Full Page, CAS latency = 2, 3, 4)

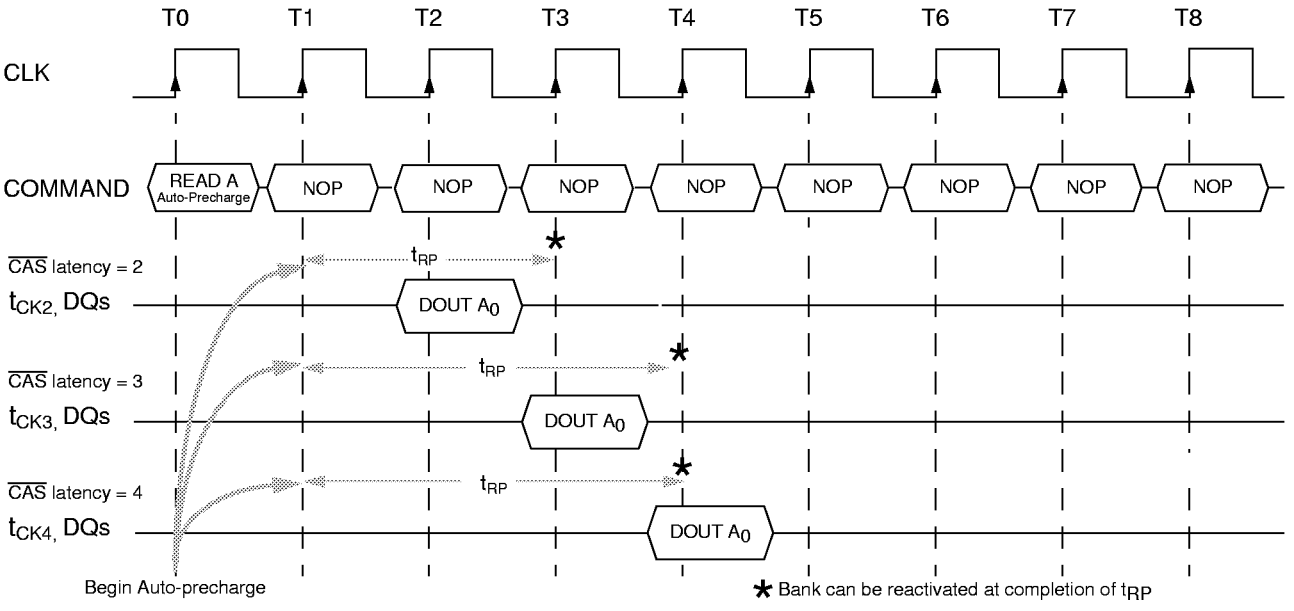


Auto-Precharge Operation

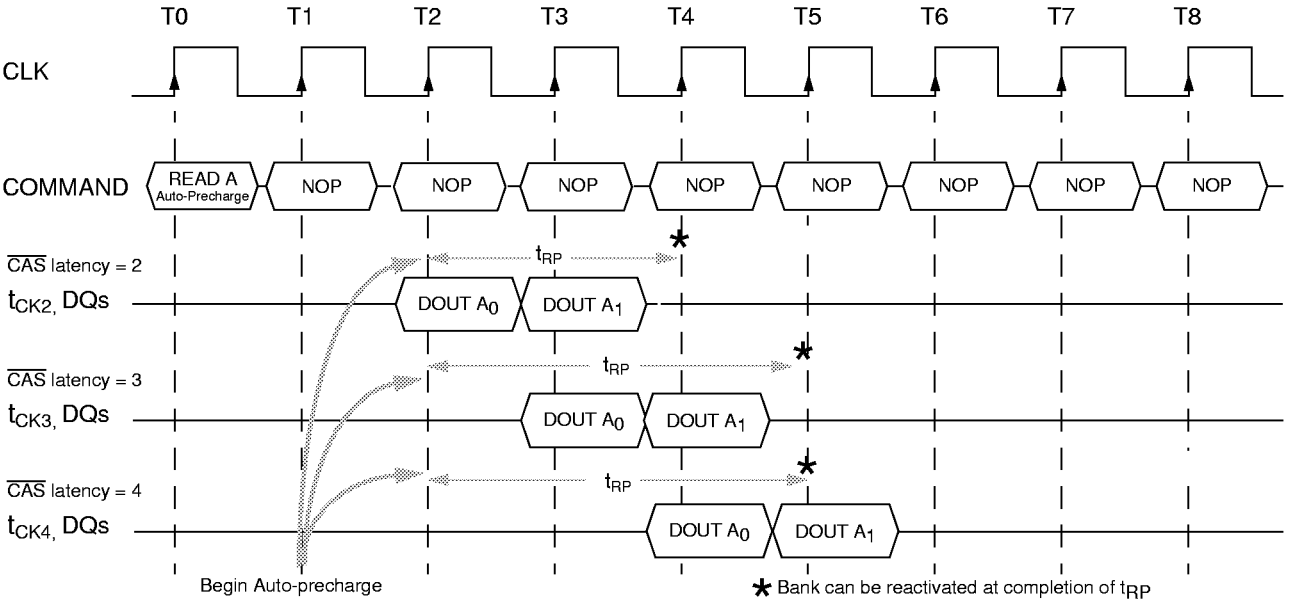
Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge before all burst read cycles have been completed. It will begin to precharge after a delay equal to the burst length, expressed in clocks. This feature allows the precharge operation to be partially or completely hidden during the burst read cycles (dependent upon $\overline{CAS}$ latency) thus improving system performance for random data access. Auto-precharge can also be implemented during Write commands although precharge can not begin any sooner than is possible by issuing the Precharge Command directly to the device.

A Read or Write Command without auto-precharge can be terminated in the midst of a burst operation. However, a Read or Write Command with auto-precharge can not be interrupted before the entire burst operation is completed. Therefore use of a Read, Write, or Precharge Command is prohibited during a read or write cycle with auto-precharge. Once the precharge operation has started the bank cannot be reactivated until the Precharge time (t_{RP}) has been satisfied. It should be noted that the device will not respond to the Auto-Precharge command if the device is programmed for full page burst read or write cycles, or full page burst read cycles with single write operation.

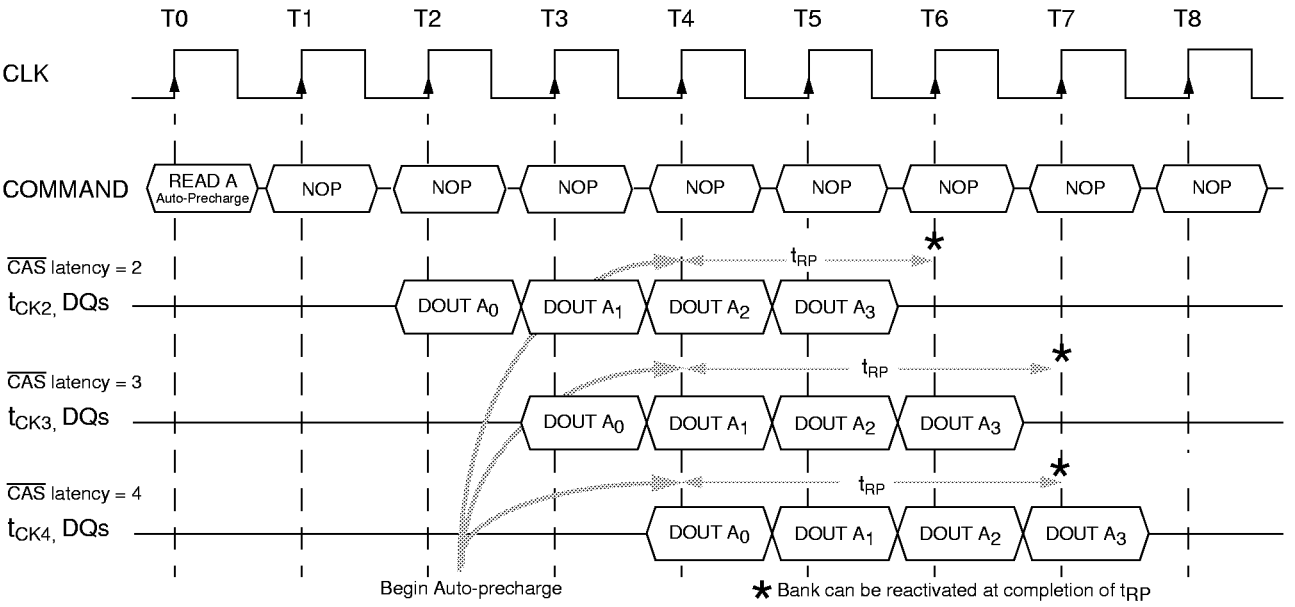
Burst Read with Auto-precharge (Burst Length = 1, $\overline{CAS}$ Latency = 2, 3, 4)



Burst Read with Auto-precharge (Burst Length = 2, $\overline{CAS}$ Latency = 2, 3, 4)

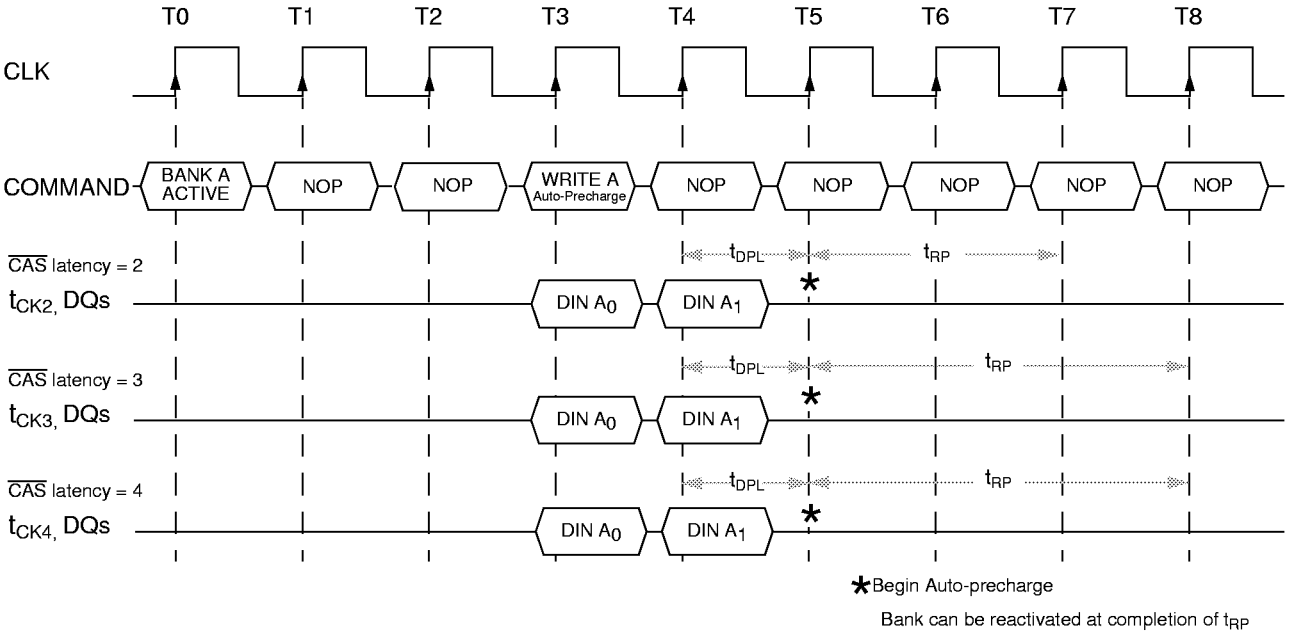


Burst Read with Auto-precharge (Burst Length = 4, $\overline{CAS}$ Latency = 2, 3, 4)



If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation one clock delay from the last burst write cycle. This delay is referred to as t_{DPL}. The bank undergoing auto-precharge can not be reactivated until t_{DPL} and t_{RP} are satisfied. This is referred to as t_{DAL}, Data-in to Active delay ($t_{DAL} = t_{DPL} + t_{RP}$).

Burst Write with Auto-Precharge (Burst Length = 2, $\overline{CAS}$ Latency = 2, 3, 4)



When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy $t_{RAS(min)}$. If this interval does not satisfy $t_{RAS(min)}$ then t_{RCD} must be extended.

Precharge Command

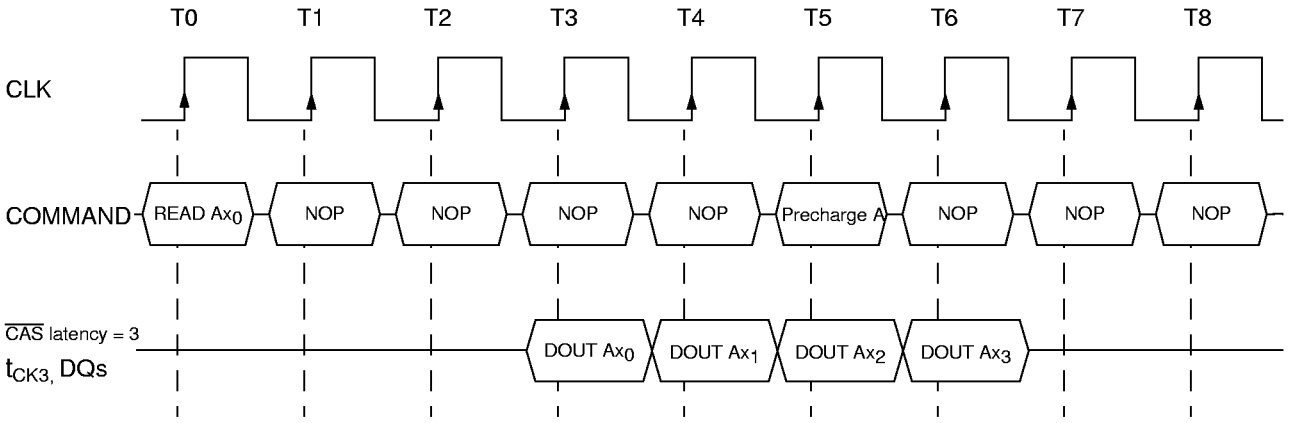
The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Three address bits, A10, A12, and A13, are used to define which bank(s) is to be precharged when the command is issued.

Bank Selection for Precharge by Address Bits

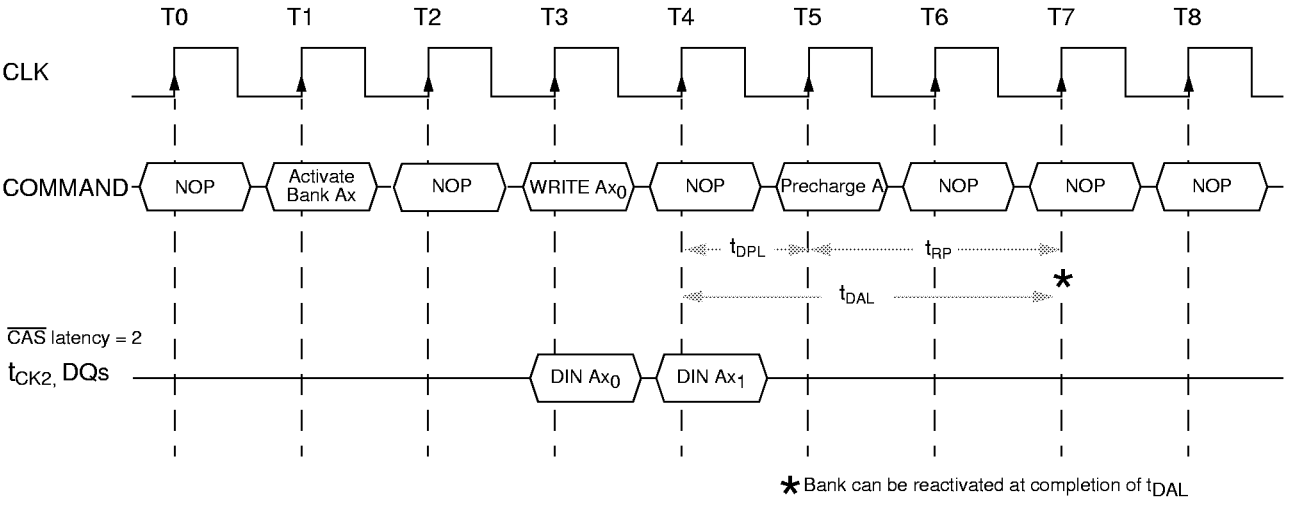
A10	Bank Select	Precharged Bank(s)
LOW	BS0, BS1	Bank defined by BS0, BS1 only
HIGH	DON'T CARE	All Banks

After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

Burst Read followed by the Precharge Command (Burst Length = 4, $\overline{CAS}$ Latency = 3)



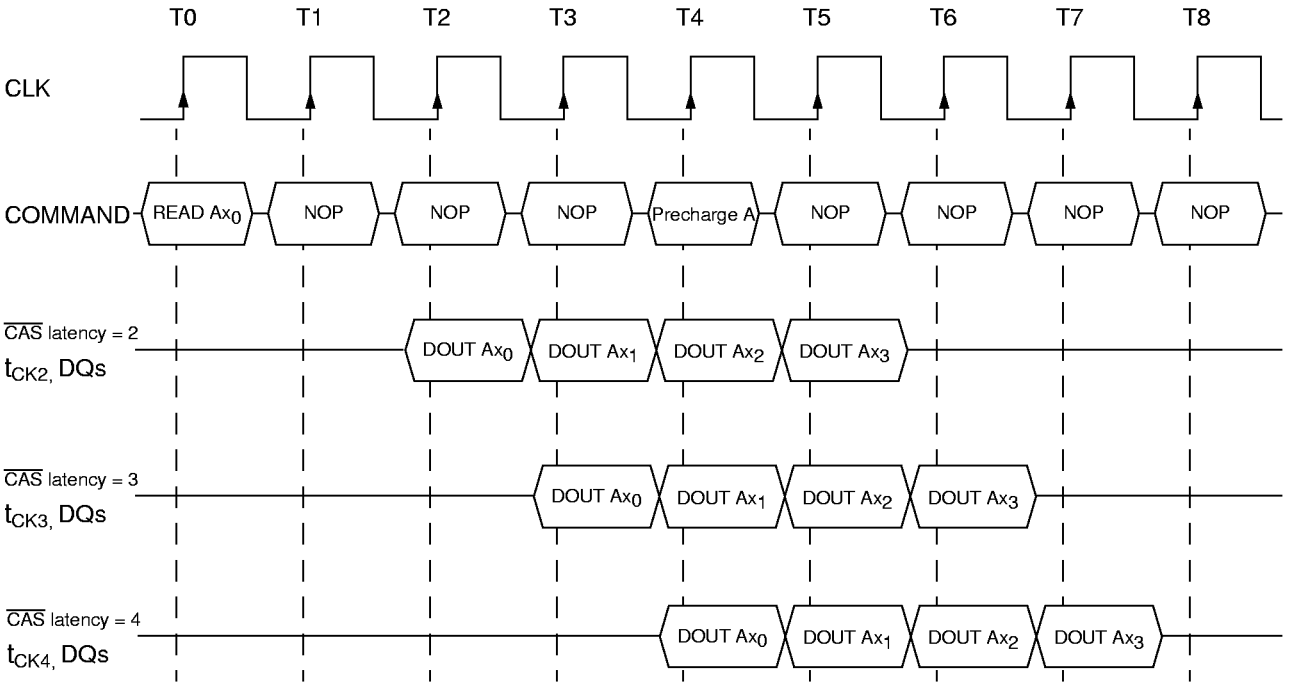
Burst Write followed by the Precharge Command (Burst Length = 2, $\overline{CAS}$ Latency = 2)



Precharge Termination

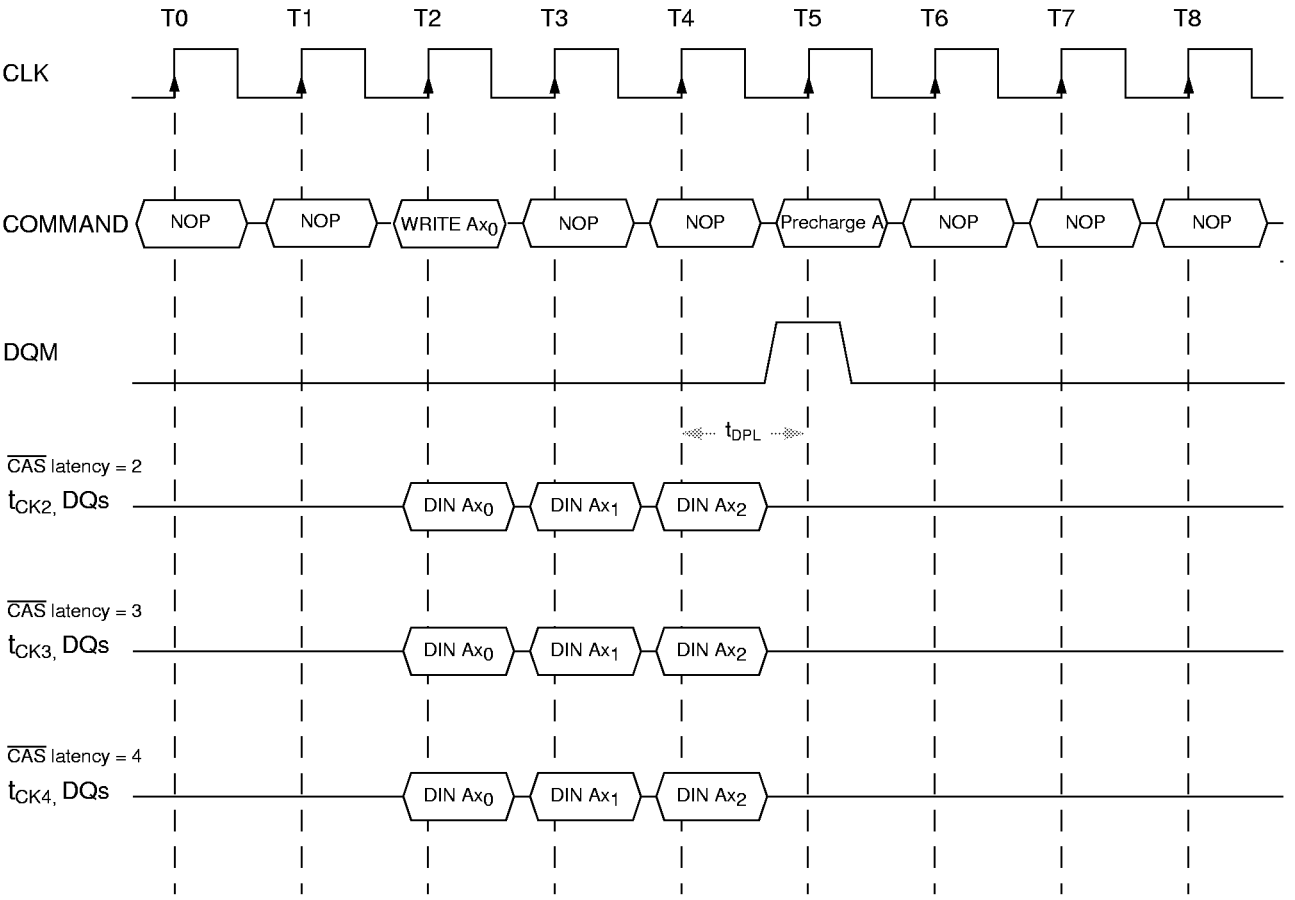
The Precharge Command may be used to terminate either a burst read or burst write operation. When the Precharge command is issued, the burst operation is terminated and bank precharge begins. For burst read operations, valid data will continue to appear on the data bus as a function of $\overline{CAS}$ Latency.

Burst Read Interrupted by Precharge (Burst Length = 8, $\overline{CAS}$ Latency = 2, 3, 4)



Burst write operations will be terminated by the Precharge command. The last write data that will be properly stored in the device is that write data that is presented to the device on the clock cycle prior to the Precharge command.

Precharge Termination of a Burst Write (Burst Length = 8, CAS Latency =2, 3, 4)



Automatic Refresh Command ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low with CKE and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). All banks of the SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto Refresh Command (CBR) can be applied. An address counter, internal to the device provides the address during the refresh cycle. No control of the external address pins is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the $\overline{RAS}$ cycle time (t_{RC}).

Self Refresh Command

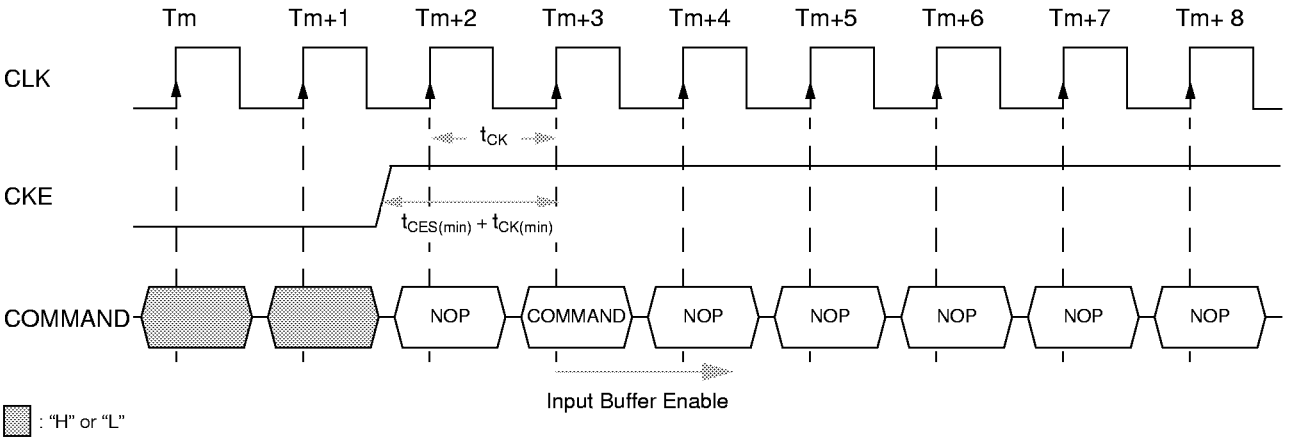
The SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit Self Refresh operation. Once the clock is cycling, the device will exit Self Refresh operation after CKE is returned high. A minimum delay time is required when the device exits Self Refresh Operation and before the next command can be issued. This delay is equal to the $\overline{RAS}$ cycle time (t_{RC}) plus the Self Refresh exit time (t_{SREX}).

Power Down Mode

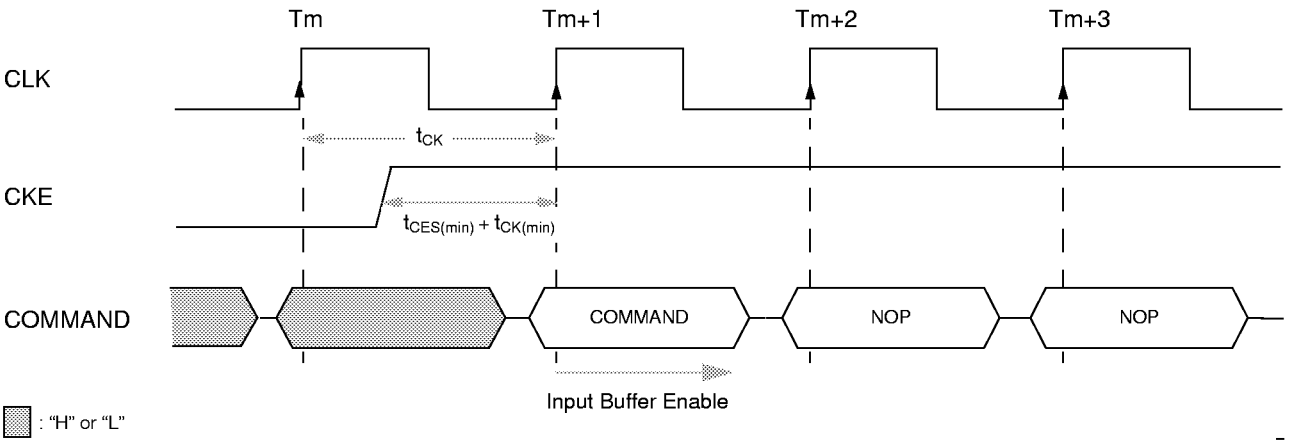
In order to reduce standby power consumption, a power down mode is available. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on t_{CK}. The input buffers need to be enabled with CKE held high for a period equal to $t_{CES(min)} + t_{CK(min)}$. (See below.)

Power Down Mode Exit Timing ($t_{CK} < t_{CES(min)} + t_{CK(min)}$)



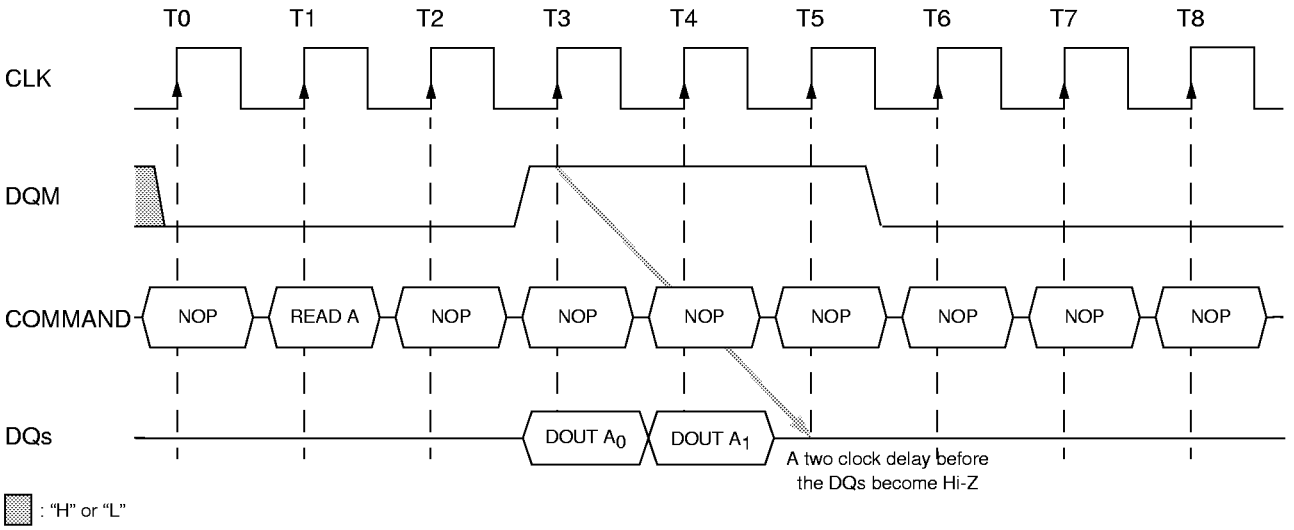
Power Down Mode Exit Timing ($t_{CK} \geq t_{CES(min)} + t_{CK(min)}$)



Data Mask

The SDRAM has a Data Mask function that can be used in conjunction with data read and write cycles. When the Data Mask is activated (DQM high) during a write cycle, the write operation is prohibited immediately (zero clock latency). If the Data Mask is activated during a read cycle, the data outputs are disabled and become high impedance after a two clock delay, independent of $\overline{CAS}$ latency.

Data Mask Activated During a Read Cycle (Burst Length = 4, $\overline{CAS}$ Latency = 2)



No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

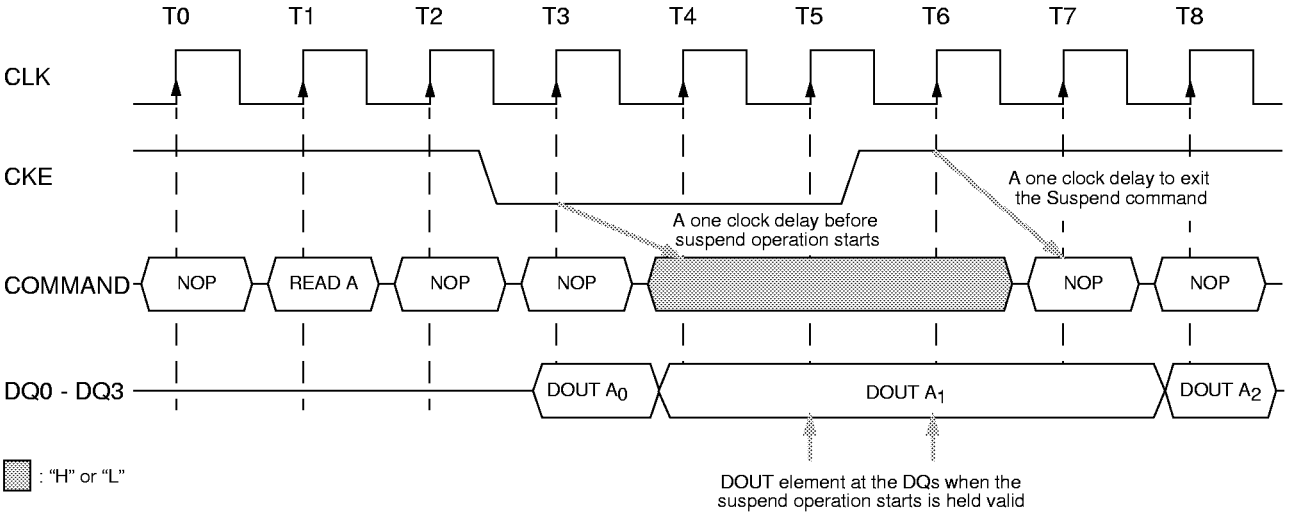
The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

Clock Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends or “freezes” any clocked operation that was currently being executed. There is a one clock delay between the registration of CKE low and the time at which the SDRAM’s operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

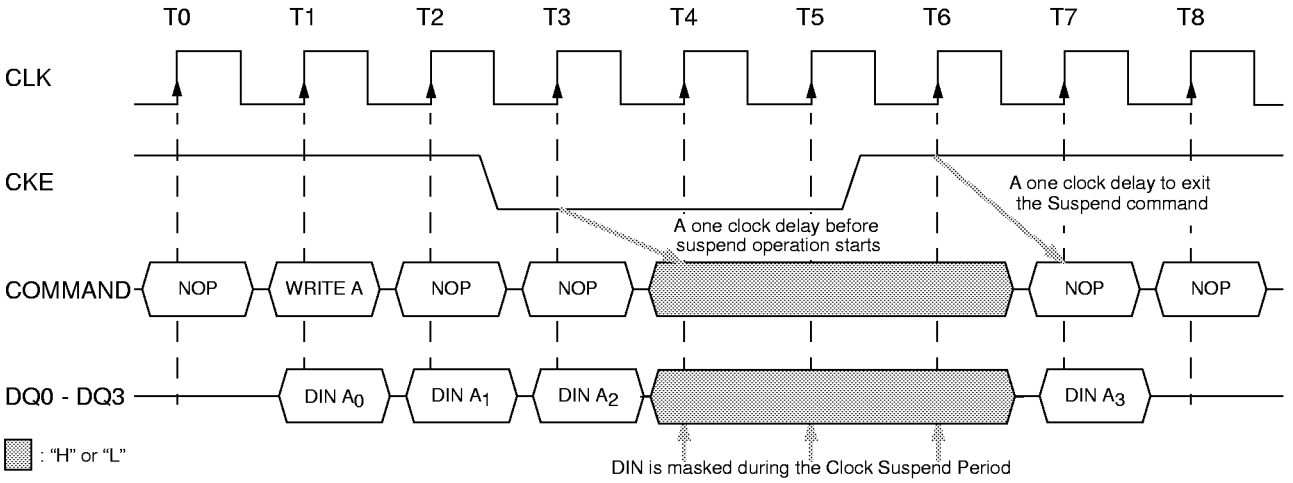
When the operation of the SDRAM is suspended during the execution of a Burst Read operation, the last valid data output onto the DQ pins will be actively held valid until Clock Suspend mode is exited.

Clock Suspend During a Read Cycle (Burst Length = 4, $\overline{CAS}$ Latency = 2)



If Clock Suspend mode is initiated during a burst write operation, then the input data is masked and ignored until the Clock Suspend mode is exited.

Clock Suspend During a Write Cycle (Burst Length = 4, $\overline{CAS}$ Latency = 2)



Command Truth Table (Notes: 1)

Function	Device State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A12, A13	A10	A11, A9-A0	Notes
		Previous Cycle	Current Cycle									
Mode Register Set	Idle	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	Idle	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	Idle	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	Idle (Self-Refresh)	L	H	H	X	X	X	X	X	X	X	
				L	H	H	X					
Single Bank Precharge	Any	H	X	L	L	H	L	X	BS	L	X	2
Precharge all Banks	Any	H	X	L	L	H	L	X	X	H	X	
Bank Activate	Idle	H	X	L	L	H	H	X	BS	Row Address		2
Write	Active	H	X	L	H	L	L	X	BS	L	Column	2
Write with Auto-Precharge	Active	H	X	L	H	L	L	X	BS	H	Column	2
Read	Active	H	X	L	H	L	H	X	BS	L	Column	2
Read with Auto-Precharge	Active	H	X	L	H	L	H	X	BS	H	Column	2
Burst Termination	Active	H	X	L	H	H	L	X	X	X	X	3, 8
No Operation	Any	H	X	L	H	H	H	X	X	X	X	
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	Active	H	X	X	X	X	X	H	X	X	X	
Power Down Mode Entry	Idle/Active	H	L	H	X	X	X	X	X	X	X	6, 7
				L	H	H	X					

1. All of the SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and DQM at the positive rising edge of the clock.
2. Bank Select (BS0, BS1): BS0, BS1 = 0,0 selects bank 0; BS0, BS1 = 0,1 selects bank 1; BS0, BS1 = 1,0 selects bank 2; BS0, BS1 = 1,1 selects bank 3.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the $\overline{CAS}$ latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode.(If this command is issued during a burst operation, the device state will be clock suspend mode.)The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
7. If $\overline{CS}$ is low, then when CKE returns high, no command is registered into the chip for one clock cycle.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

Command Truth Table (Notes: 1)

Function	Device State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A12, A13	A10	A11, A9-A0	Notes
		Previous Cycle	Current Cycle									
Power Down Mode Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X	6, 7
				L	H	H	X					

1. All of the SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and DQM at the positive rising edge of the clock.
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7. If $\overline{CS}$ is low, then when CKE returns high, no command is registered into the chip for one clock cycle.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Power Supply Voltage	-0.3 to +4.6	V	1
VDDQ	Power Supply Voltage for Output	-0.3 to +4.6	V	1
V_{IN}	Input Voltage	-0.3 to VDD+0.3	V	1
V_{OUT}	Output Voltage	-0.3 to VDD+0.3	V	1
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

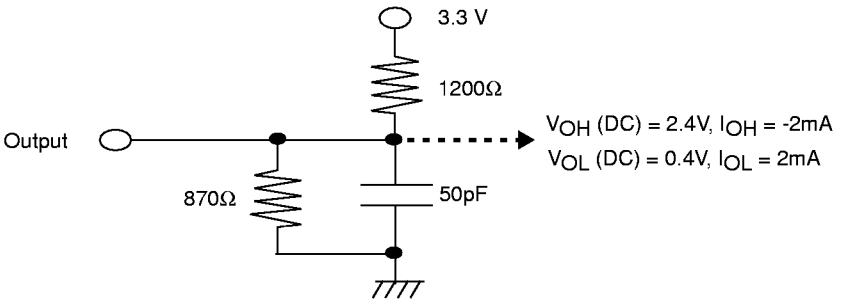
Recommended DC Operating Conditions (T_A= 0 to 70˚C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	3.0	3.3	3.6	V	1
VDDQ	Supply Voltage for Output	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	VDD + 0.3	V	1, 2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1, 3

1. All voltages referenced to V_{SS} and VSSQ.
2. V_{IH} (max) = VDD/VDDQ + 1.2V for pulse width ≤ 5ns.
3. V_{IL} (min) = VSS/VSSQ - 1.2V for pulse width ≤ 5ns.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Min.	Max.	Units	Notes
C_I	Input Capacitance (A0-A11, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, DQM)		4.0	pF	
	Input Capacitance (CLK)		6.0	pF	
C_O	Output Capacitance (DQ0 - DQ15)		5.0	pF	



DC Output Load Circuit

Output Characteristics (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ VDD), All Other Pins Not Under Test = 0V	-5	+5	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ VDDQ)	-5	+5	µA	
V_{OH}	Output Level (LVTTL) Output "H" Level Voltage (I_{OUT} = -2.0mA)	2.4	—	V	
V_{OL}	Output Level (LVTTL) Output "L" Level Voltage (I_{OUT} = +2.0mA)	—	0.4	V	

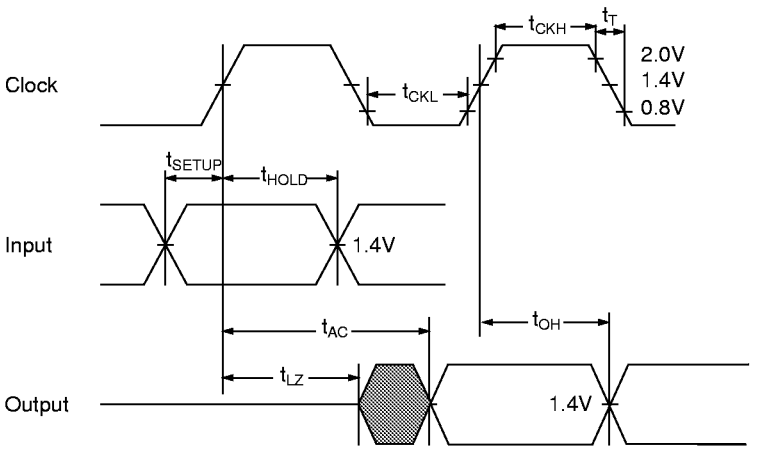
Operating, Standby and Refresh Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

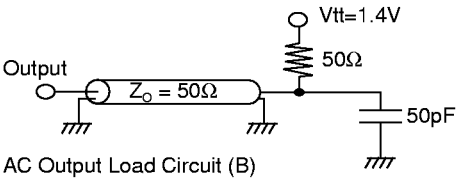
Parameter	Symbol	Test Condition	Speed			Units	Notes
			-80	-10	-12		
Operating Current $t_{RC} = t_{RC}$(min), t_{CK} = min Active-Precharge command cycling without burst operation	I_{CC1}	1 bank operation	100	80	70	mA	1
	I_{CC1B}	4 bank interleave operation	140	120	105	mA	
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{CS}$ =V_{IH}(min)	1	1	1	mA	1
	I_{CC2PS}	CKE ≤ V_{IL}(max), t_{CK} = Infinity, $\overline{CS}$ =V_{IH}(min)	1	1	1	mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC2}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH} (min)	35	30	28	mA	1
	I_{CC2S}	CKE ≥ V_{IH}(min), t_{CK} = Infinity, $\overline{CS}$ =V_{IH} (min)	12	12	12	mA	
No Operating Current (Active state: 4 bank)	I_{CC3}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH} (min)	40	35	33	mA	
	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{CS}$ =V_{IH} (min) (Power Down Mode)	2	2	2	mA	
Burst Operating Current	I_{CC4}	t_{CK} = min, Read/ Write command cycling	145	125	115	mA	1, 2
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, CBR command cycling	120	100	90	mA	1
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	1	1	1	mA	

1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed once during t_{CK}(min).
2. The specified values are obtained with the output open.

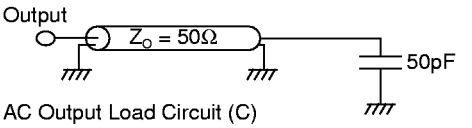
AC Characteristics (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 200µs, with DQM and CKE held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point.





AC Output Load Circuit (B)



AC Output Load Circuit (C)

3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume t_T=1.2ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Clock and Clock Enable Parameters

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK4}	Clock Cycle Time, $\overline{CAS}$ Latency = 4	8	1000	10	1000	12	1000	ns	
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	8	1000	10	1000	12	1000	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	10	1000	12	1000	15	1000	ns	
$t_{AC4\ (C)}$	Clock Access Time, $\overline{CAS}$ Latency = 4	—	6	—	7	—	8	ns	1
$t_{AC3\ (C)}$	Clock Access Time, $\overline{CAS}$ Latency = 3	—	6	—	7	—	8	ns	1
$t_{AC2\ (C)}$	Clock Access Time, $\overline{CAS}$ Latency = 2	—	6	—	8	—	9	ns	1
$t_{AC4\ (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 4	—	5	—	6	—	7	ns	1
$t_{AC3\ (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 3	—	5	—	6	—	7	ns	1
$t_{AC2\ (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 2	—	5	—	7	—	8	ns	1
t_{CKH}	Clock High Pulse Width	3	—	3	—	3	—	ns	2
t_{CKL}	Clock Low Pulse Width	3	—	3	—	3	—	ns	2
t_{CES}	Clock Enable Set-up Time	2	—	2.5	—	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	1	—	1	—	ns	
t_{SB}	Power down mode Entry Time	0	8	0	10	0	12	ns	

1. Access time is measured at 1.4V. See AC output load circuit.
2. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Clock and Clock Enable Parameters

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_T	Transition Time (Rise and Fall)	0.5	10	0.5	10	0.5	10	ns	

1. Access time is measured at 1.4V. See AC output load circuit.
2. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Common Parameters

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CS}	Command Setup Time	2	—	2.5	—	3	—	ns	
t_{CH}	Command Hold Time	1	—	1	—	1	—	ns	
t_{AS}	Address and Bank Select Set-up Time	2	—	2.5	—	3	—	ns	
t_{AH}	Address and Bank Select Hold Time	1	—	1	—	1	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	—	24	—	30	—	ns	1
t_{RC}	Bank Cycle Time	72		90		108		ns	1
t_{RAS}	Active Command Period	48	100000	60	100000	72	100000	ns	1
t_{RP}	Precharge Time	20	—	24	—	30	—	ns	1
t_{RRD}	Bank to Bank Delay Time	20	—	20	—	20	—	ns	1
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	—	1	—	1	—	CLK	

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Mode Register Set Cycle Time	16	—	20	—	24	—	ms	1

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	3	—	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0	—	0	—	0	—	ns	
t_{HZ}	Data Out to High Impedance Time	3	8	3	10	3	12	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	2	—	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Refresh Cycle

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	—	64	—	64	—	64	ms	1
t_{SREX}	Self Refresh Exit Time	10		10		10		ns	

1. 4096 cycles.

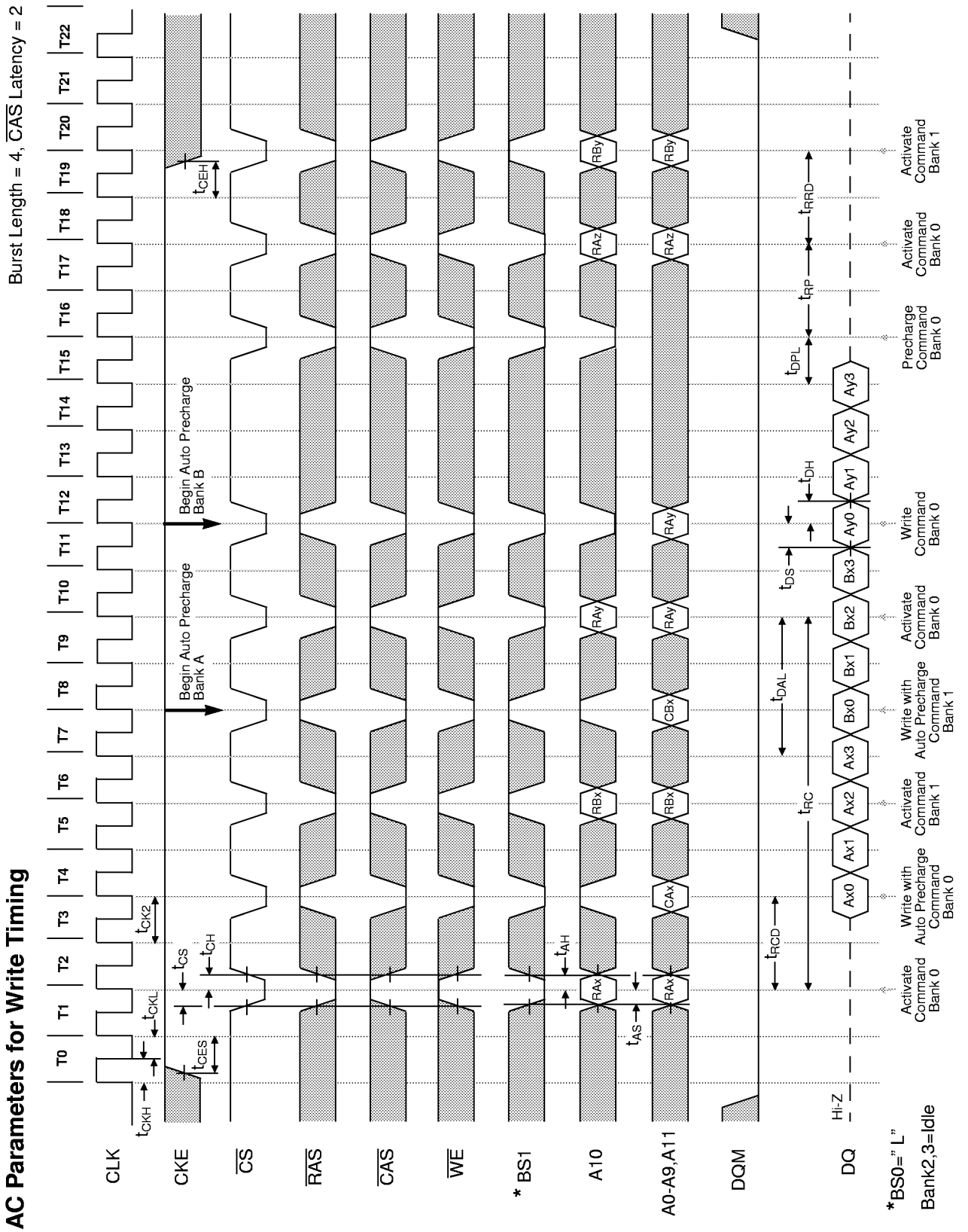
Write Cycle

Symbol	Parameter	-80		-10		-12		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{DS}	Data In Set-up Time	2	—	2.5	—	3	—	ns	
t_{DH}	Data In Hold Time	1	—	1	—	1	—	ns	
t_{DPL4}	Data input to Precharge	8	—	10	—	12	—	ns	
t_{DPL3}	Data input to Precharge	8	—	10	—	12	—	ns	
t_{DPL2}	Data input to Precharge	10	—	12	—	15	—	ns	
t_{DQW}	DQM Write Mask Latency	0	—	0	—	0	—	CLK	

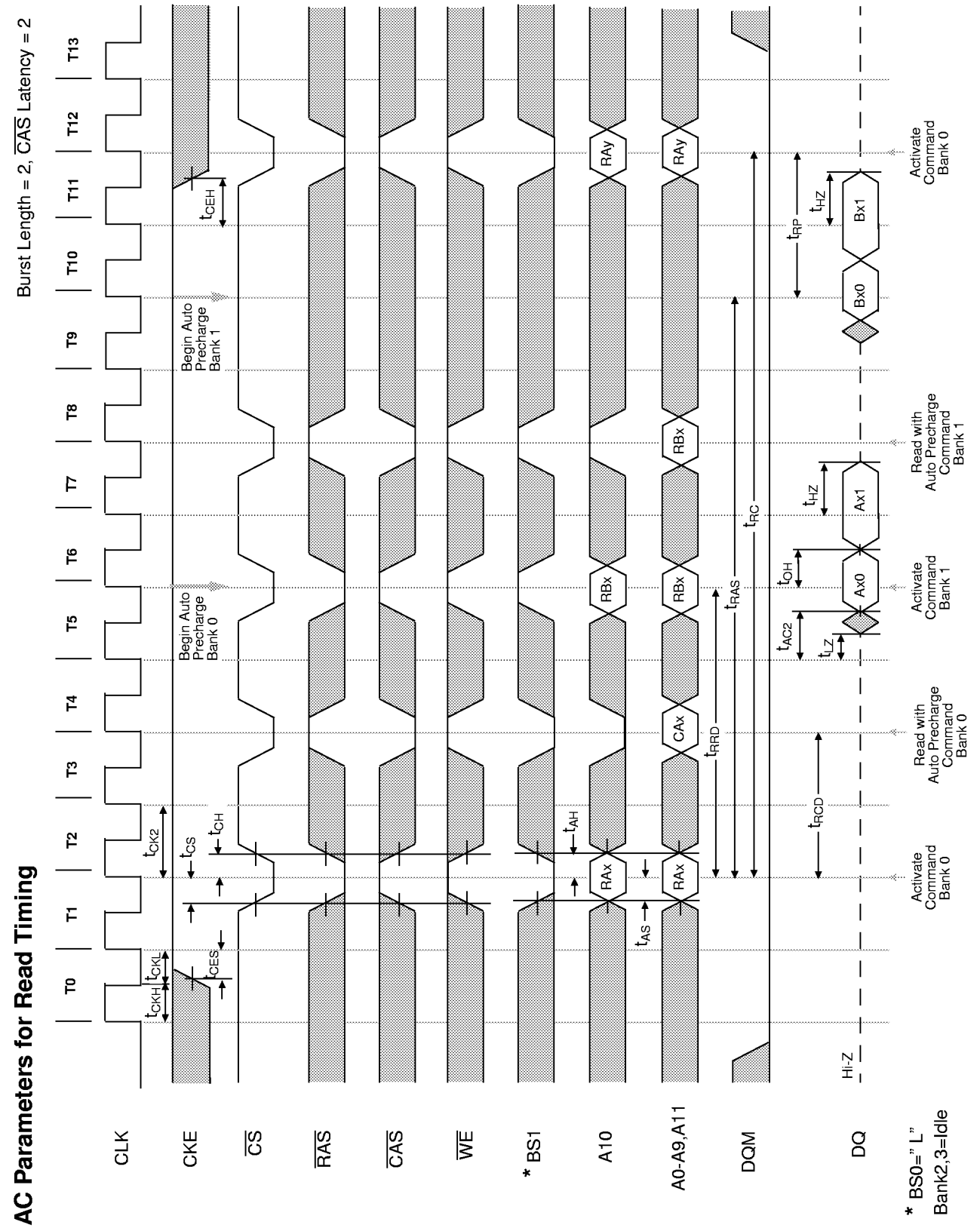
Timing Diagrams

Page

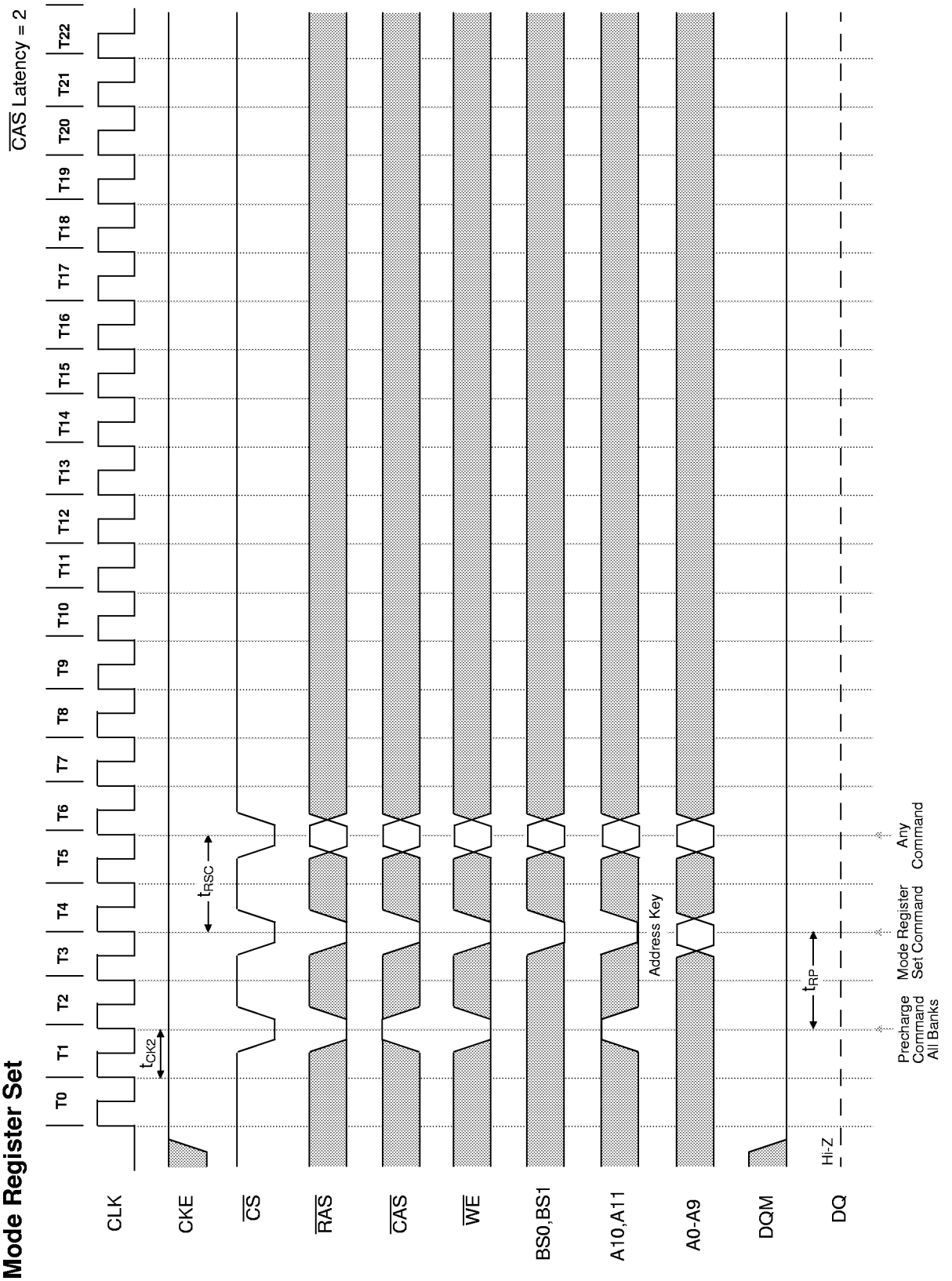
AC Parameters for Write Timing



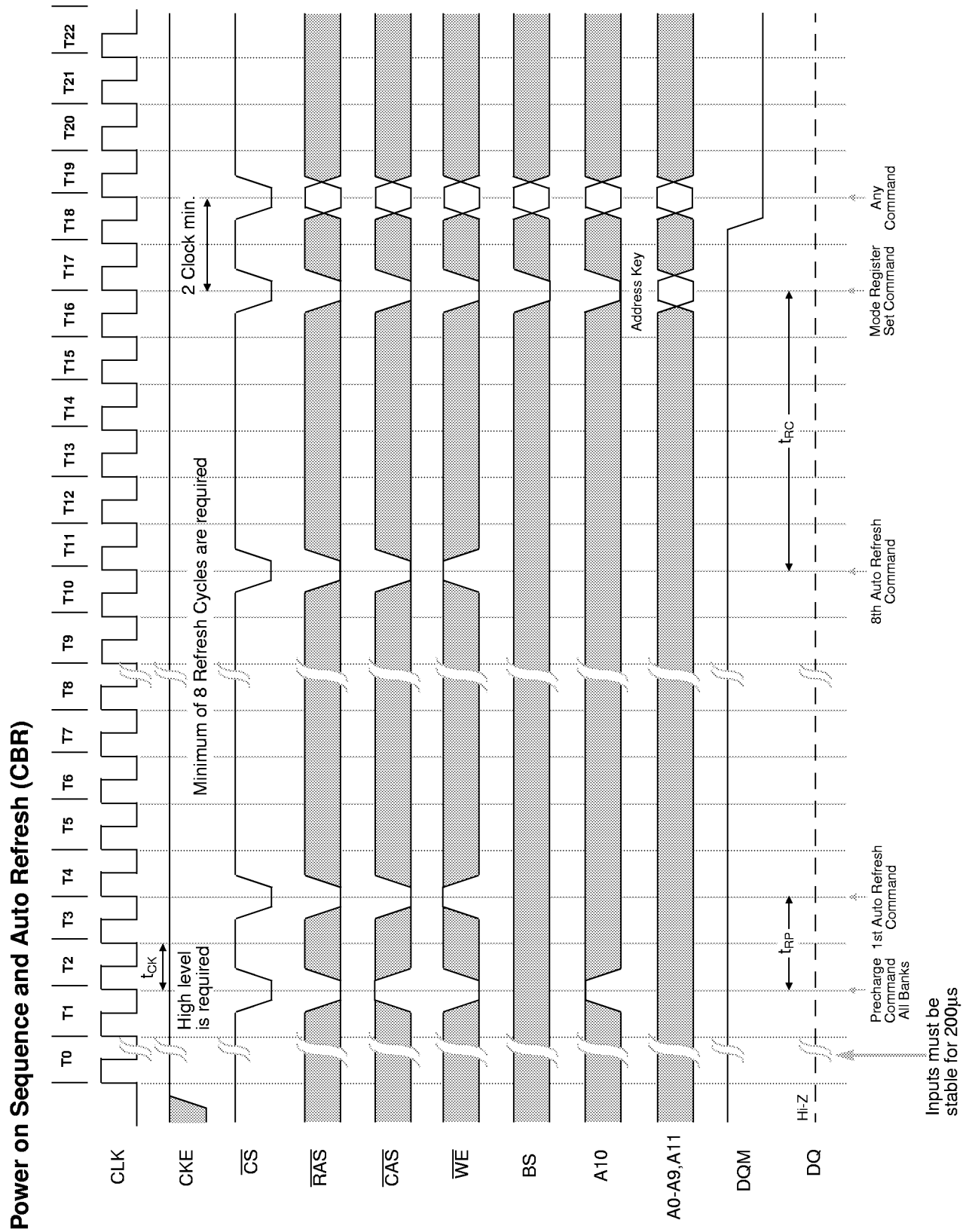
AC Parameters for Read Timing



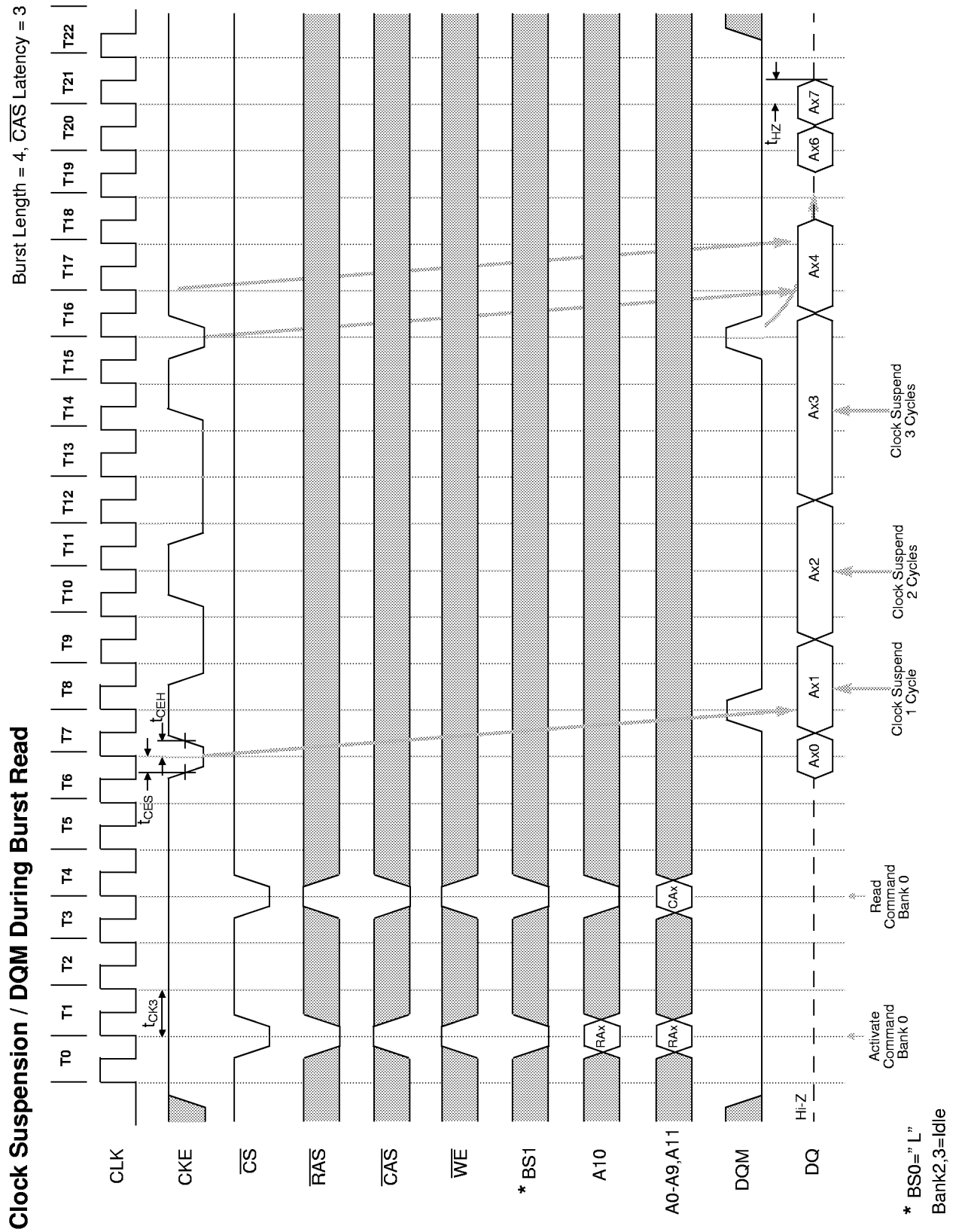
Mode Register Set



Power on Sequence and Auto Refresh (CBR)

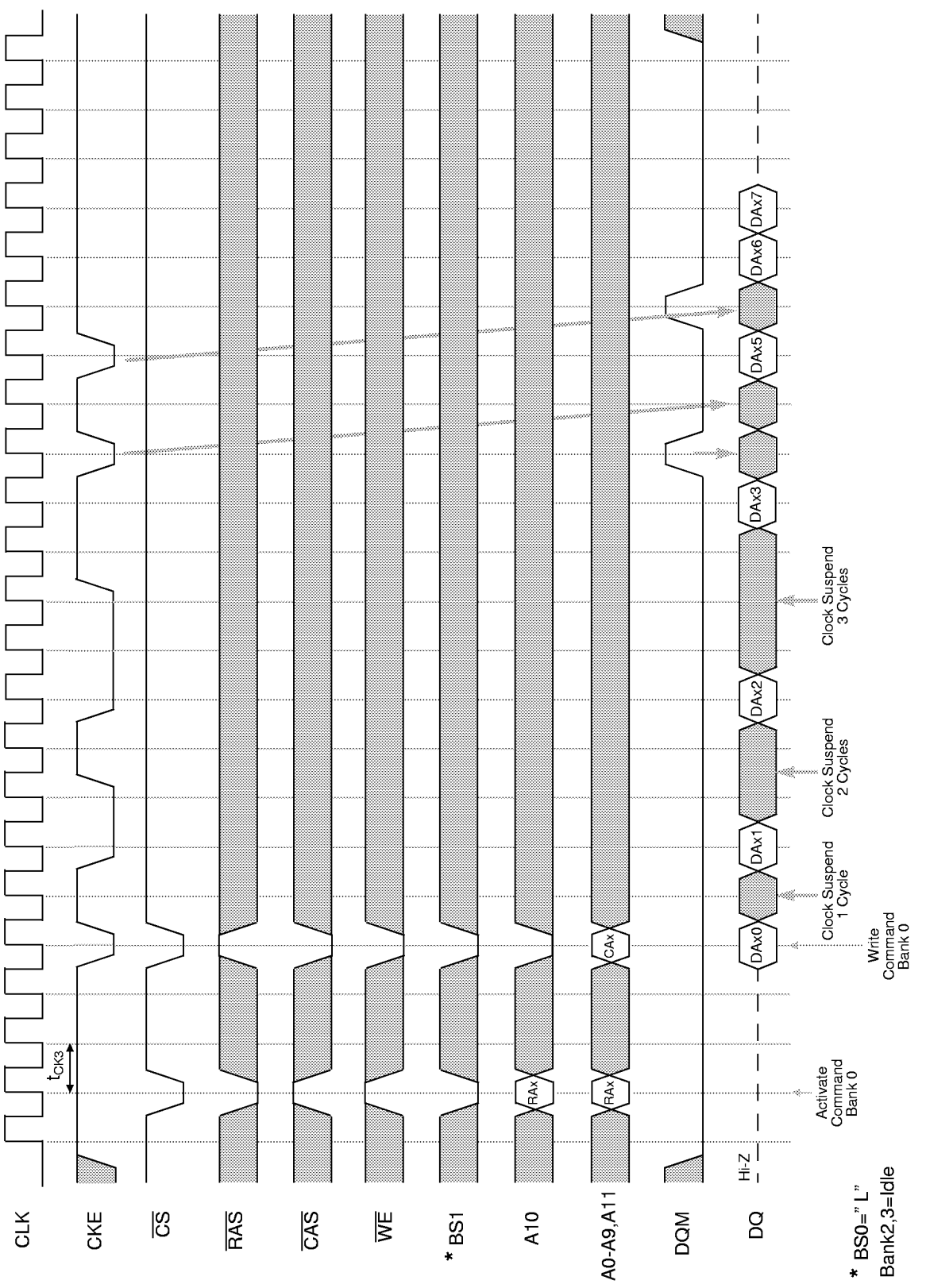


Clock Suspension / DQM During Burst Read

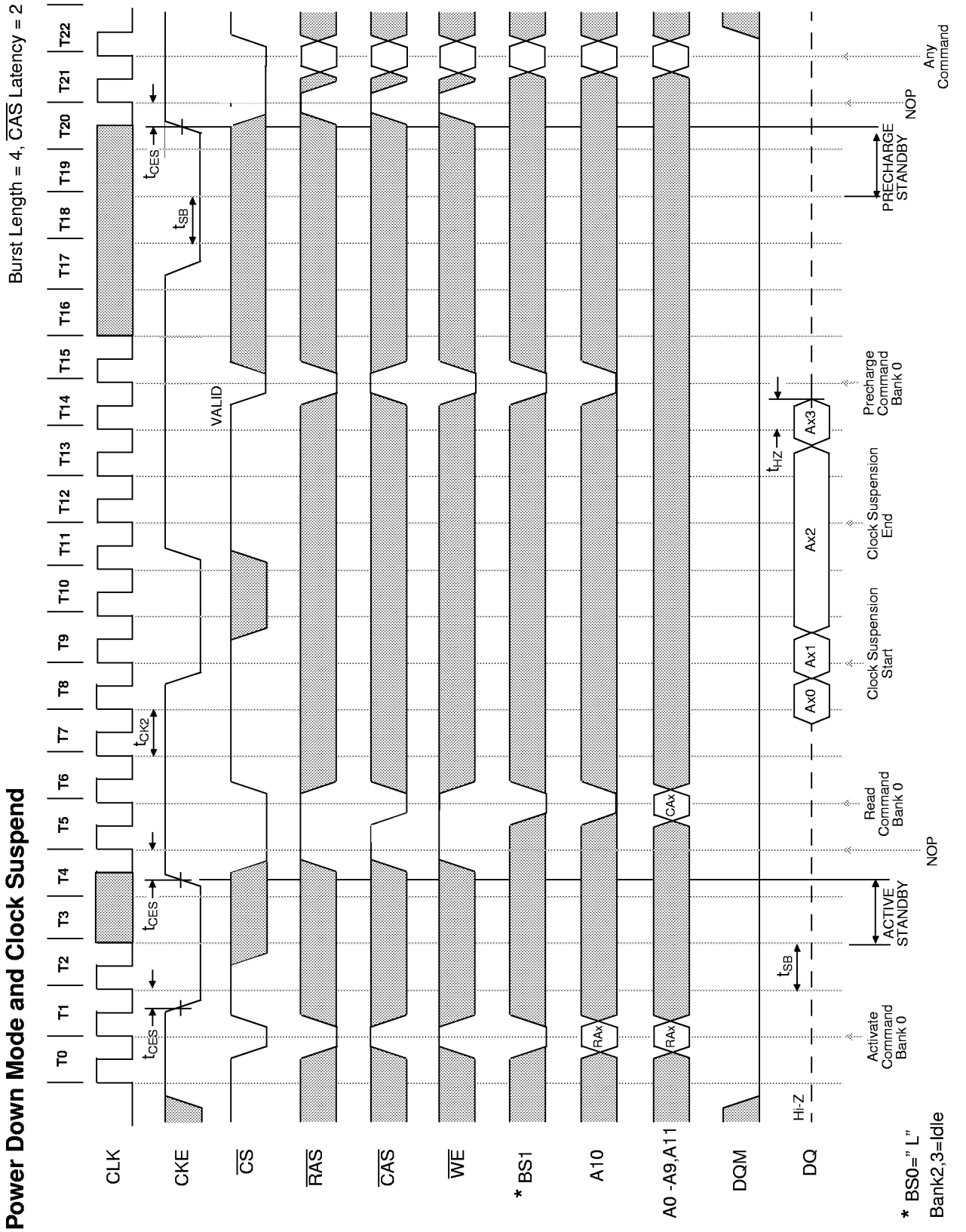


Clock Suspension / DQM During Burst Write

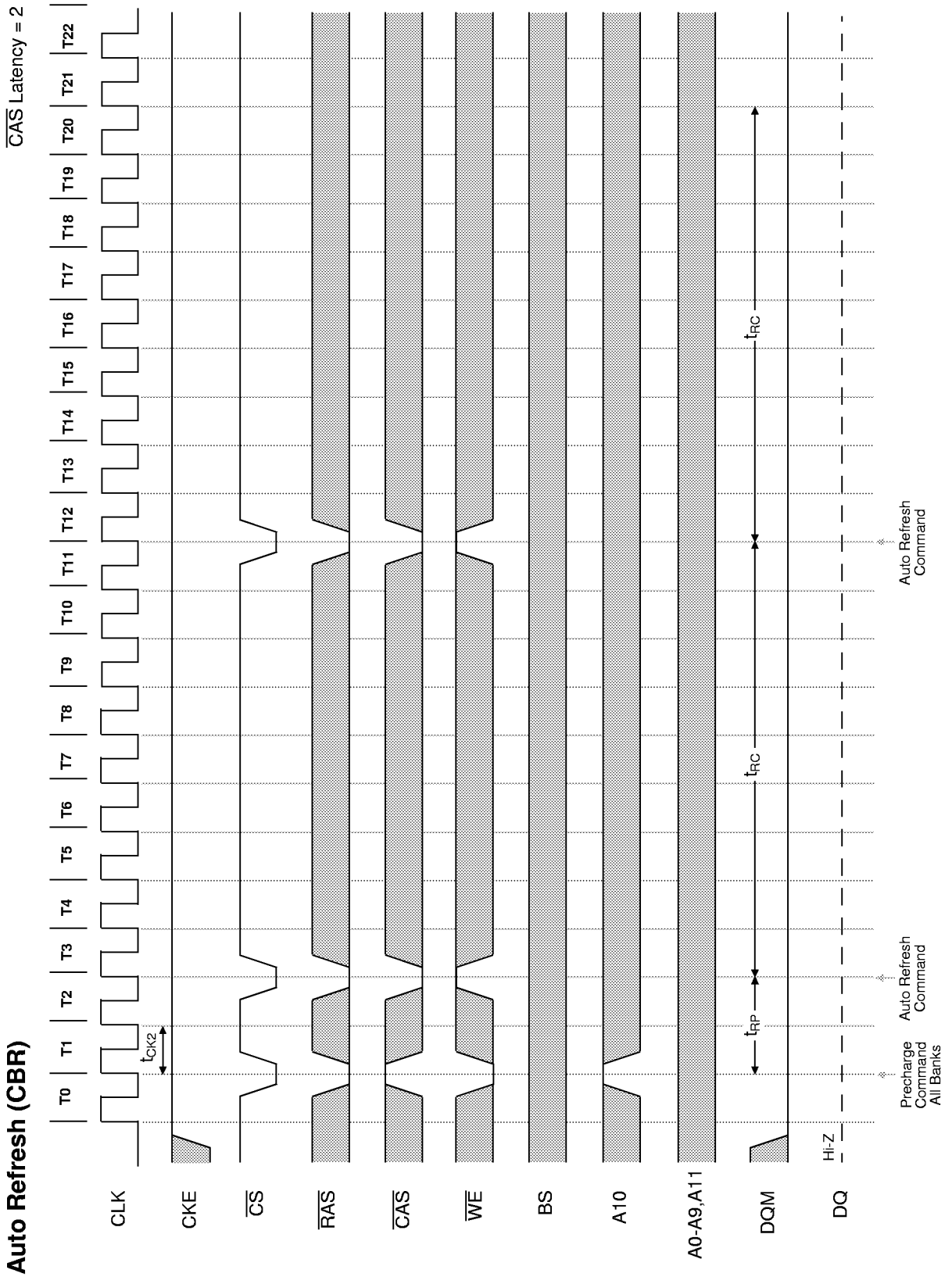
Burst Length = 8, $\overline{CAS}$ Latency = 3



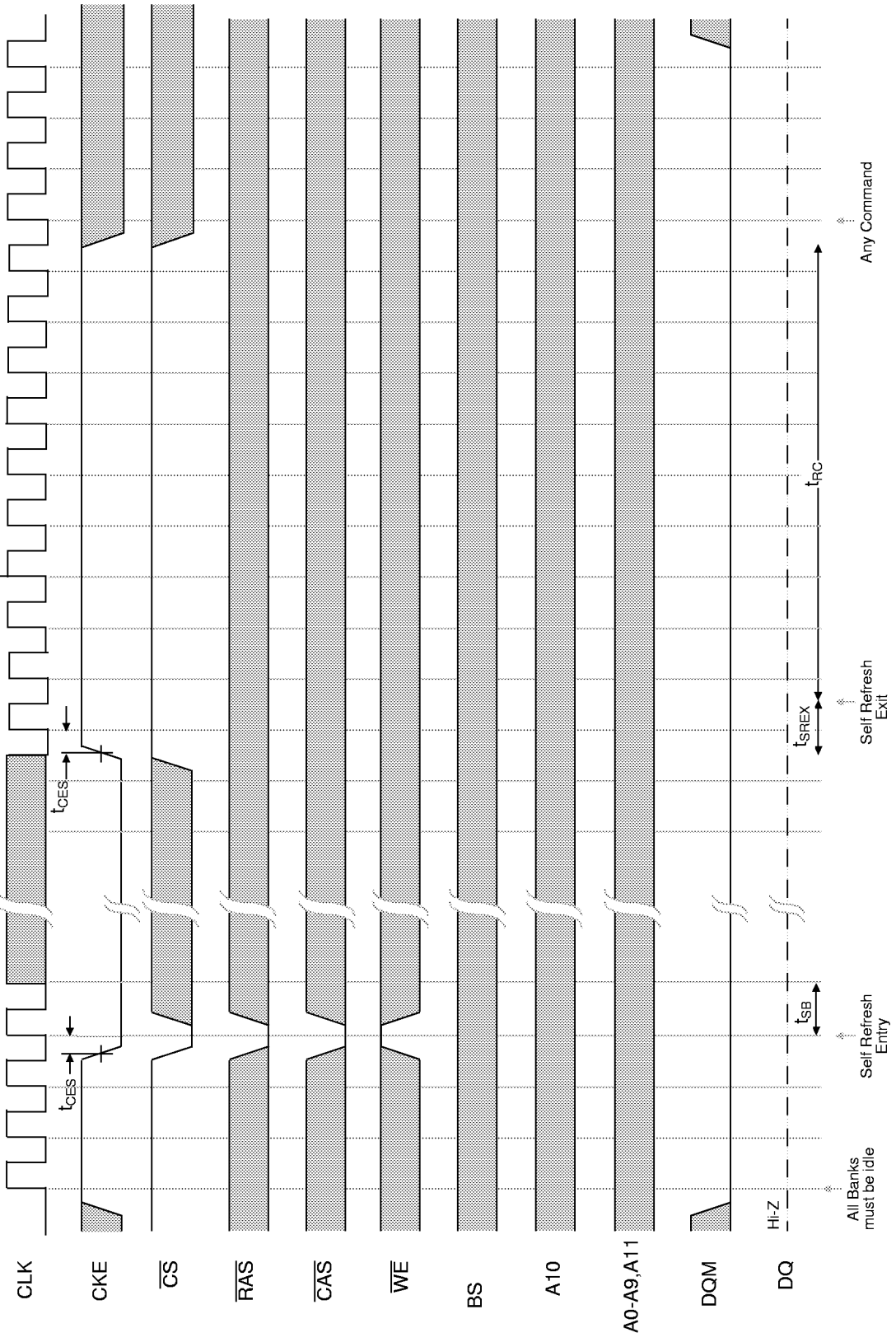
Power Down Mode and Clock Suspend



Auto Refresh (CBR)

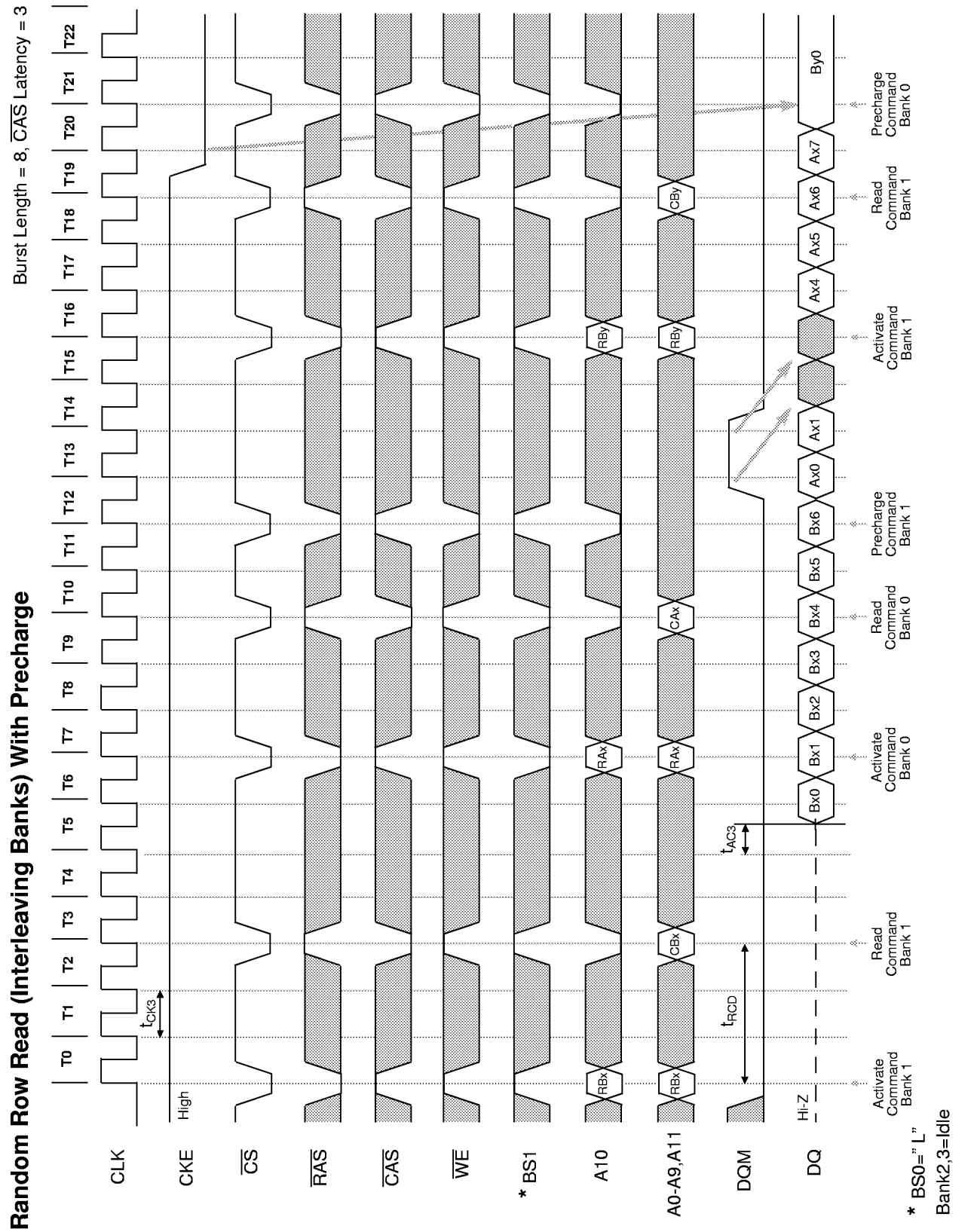


Self Refresh (Entry and Exit) ***Note: The CLK signal must be reestablished prior to CKE returning high.



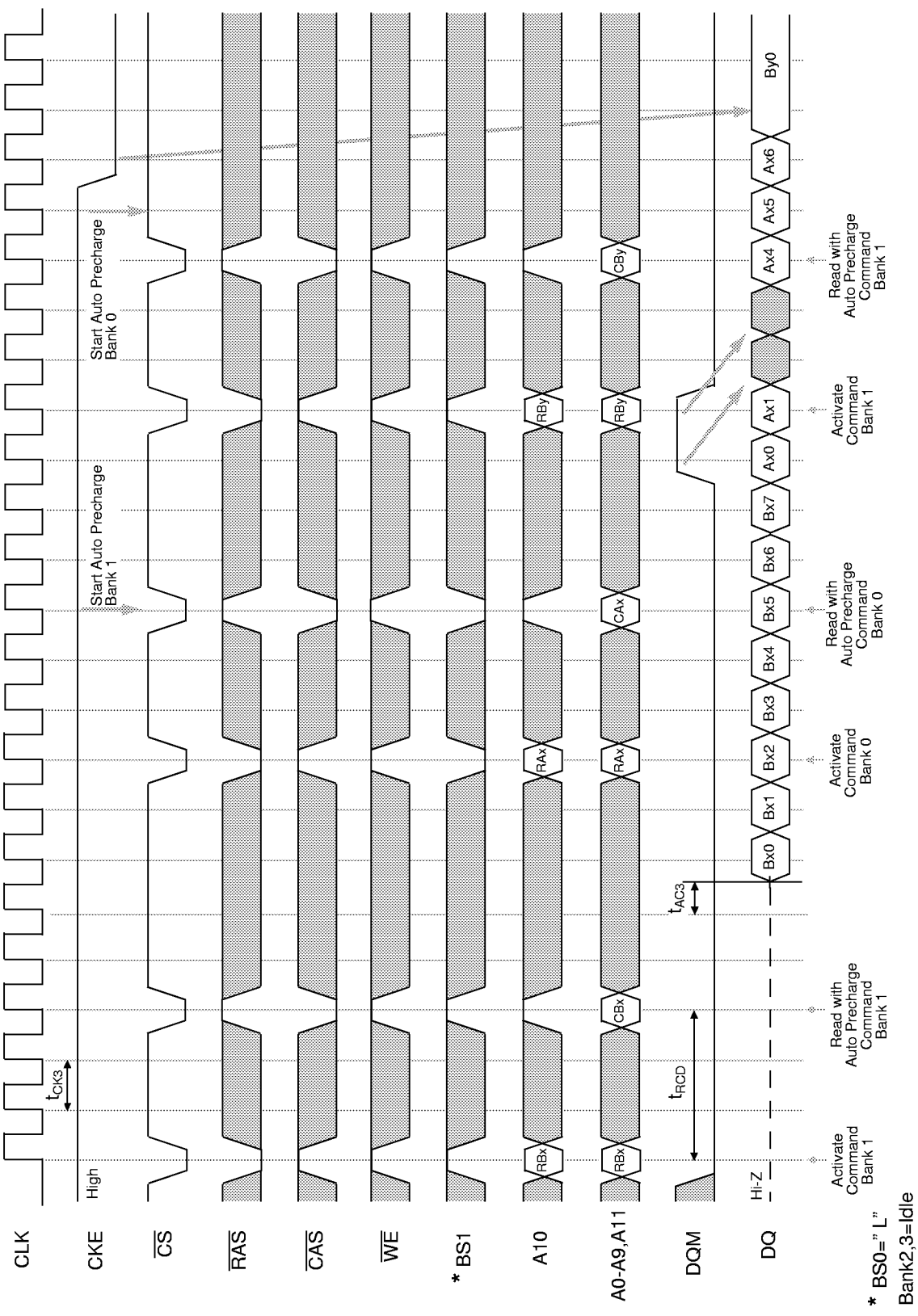
Random Row Read (Interleaving Banks) With Precharge

Burst Length = 8, $\overline{CAS}$ Latency = 3



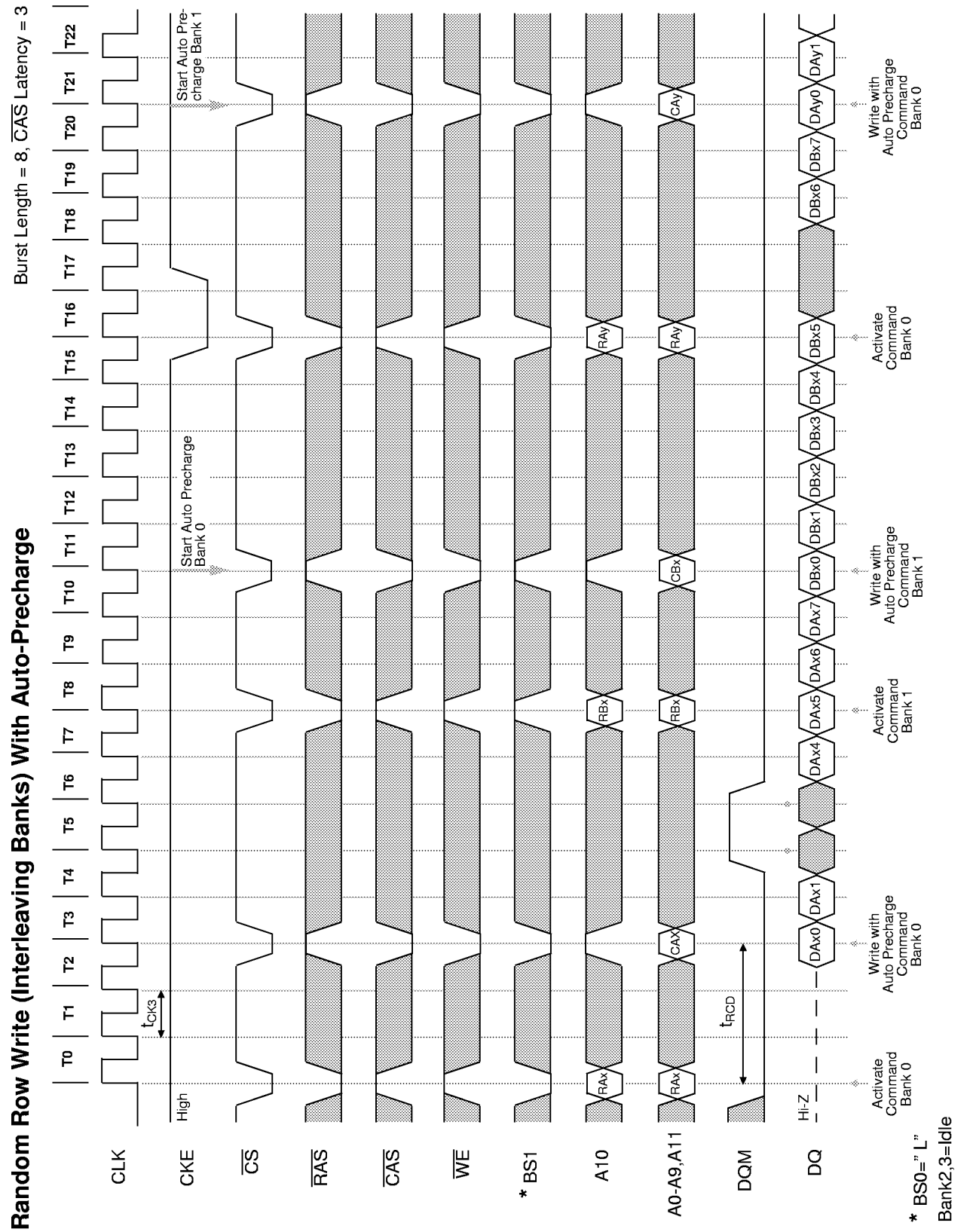
Random Row Read (Interleaving Banks) With Auto-Precharge

Burst Length = 8, $\overline{CAS}$ Latency = 3



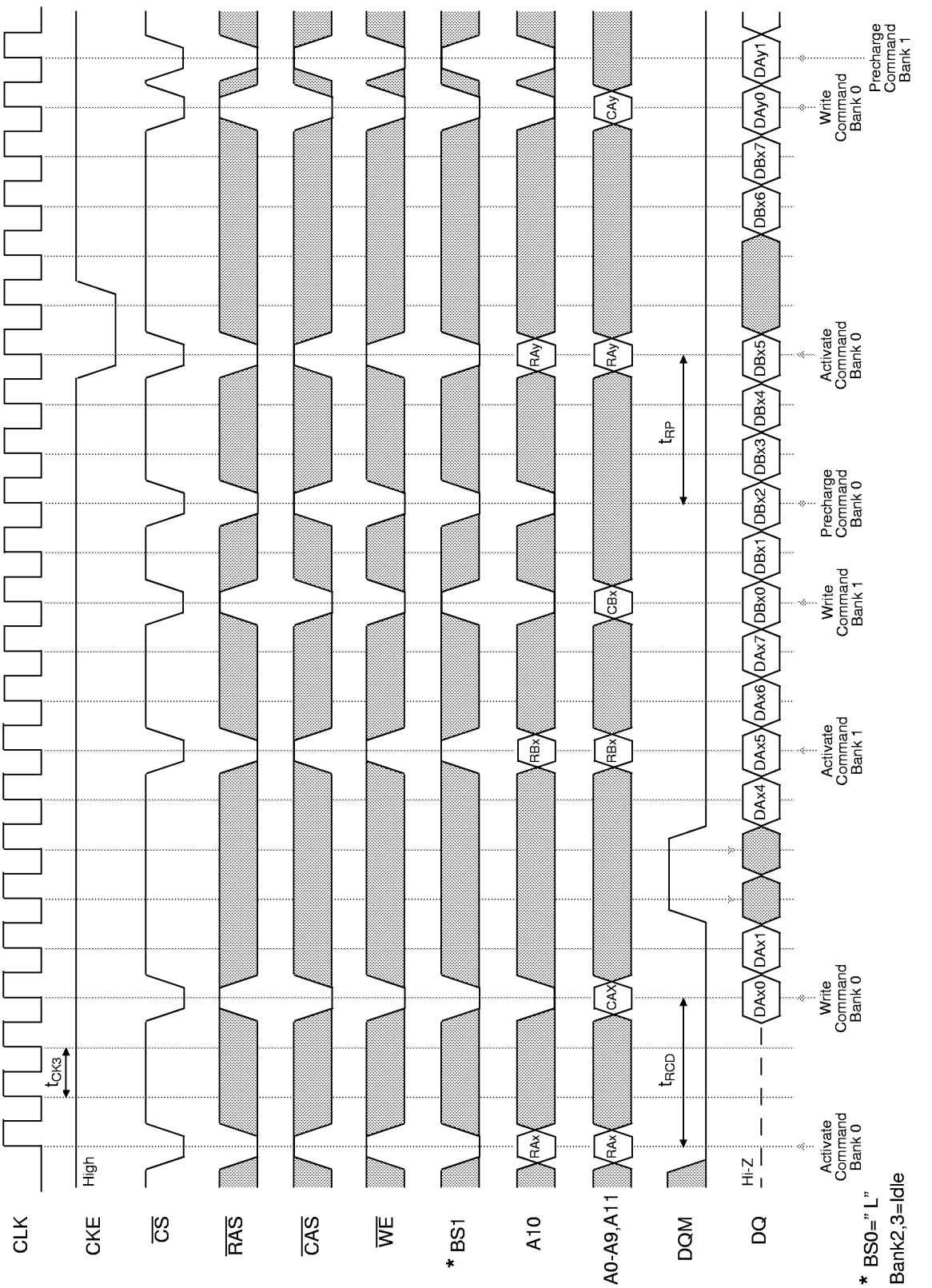
Random Row Write (Interleaving Banks) With Auto-Precharge

Burst Length = 8, $\overline{CAS}$ Latency = 3

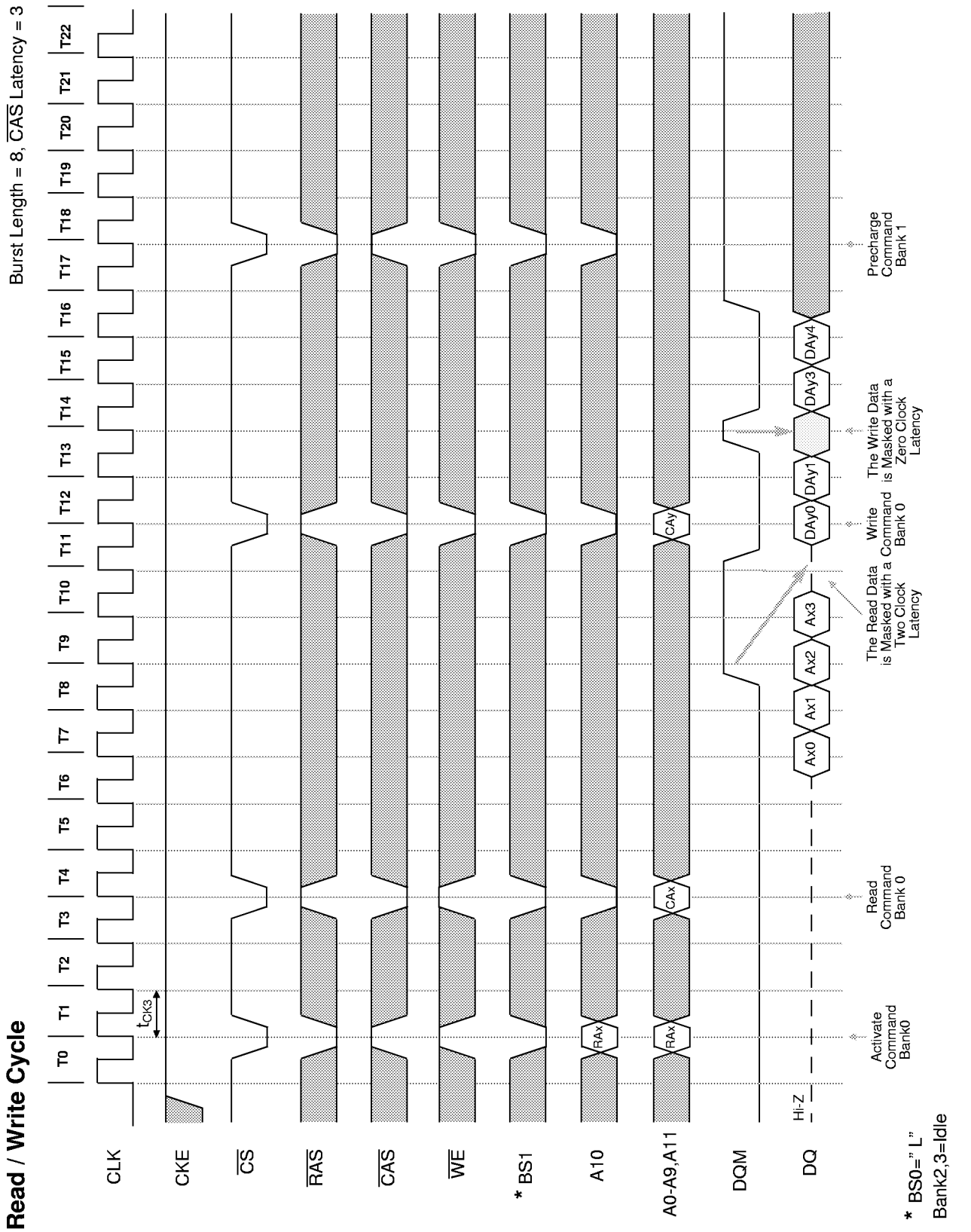


Random Row Write (Interleaving Banks) With Precharge

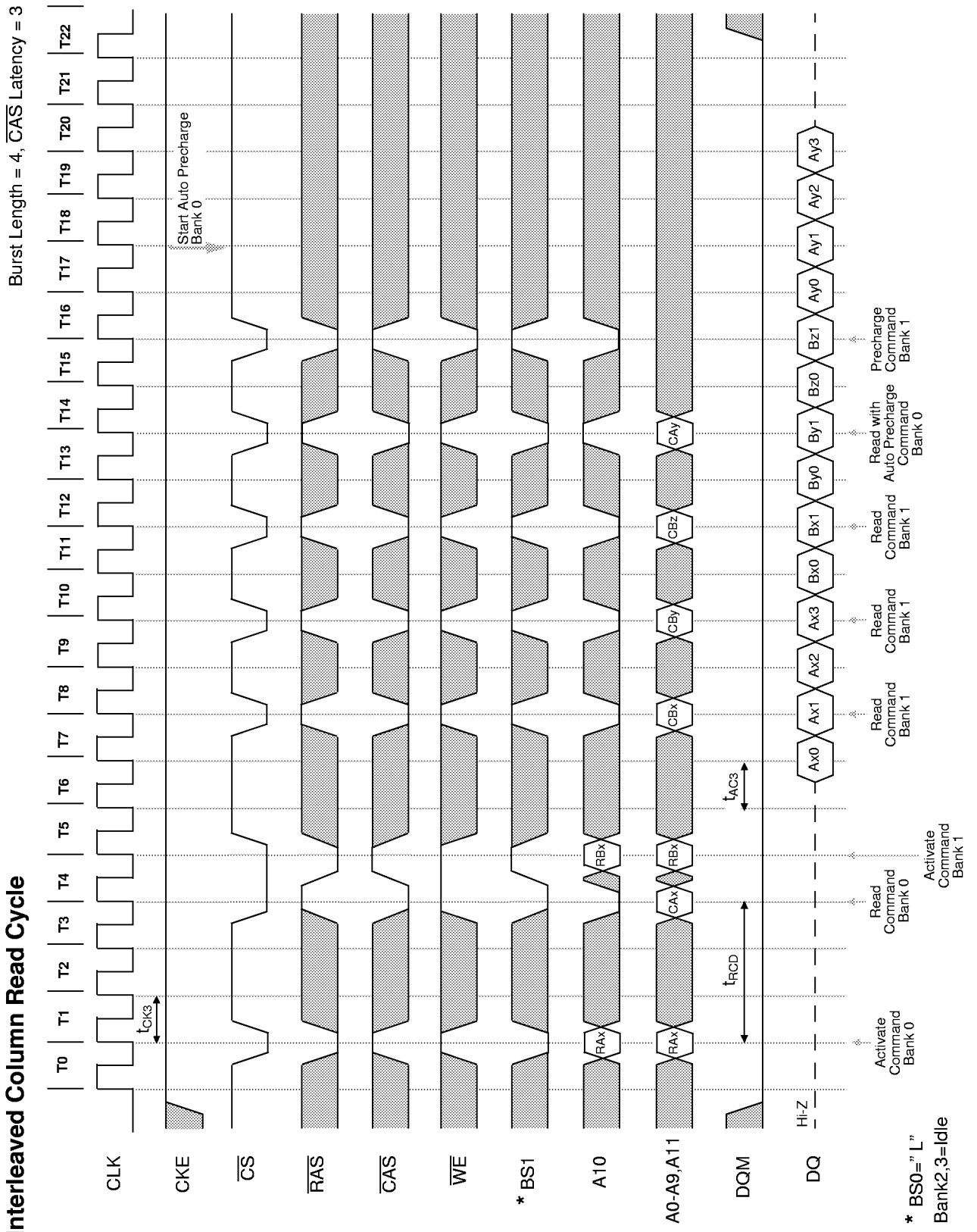
Burst Length = 8, $\overline{CAS}$ Latency = 3



Read / Write Cycle

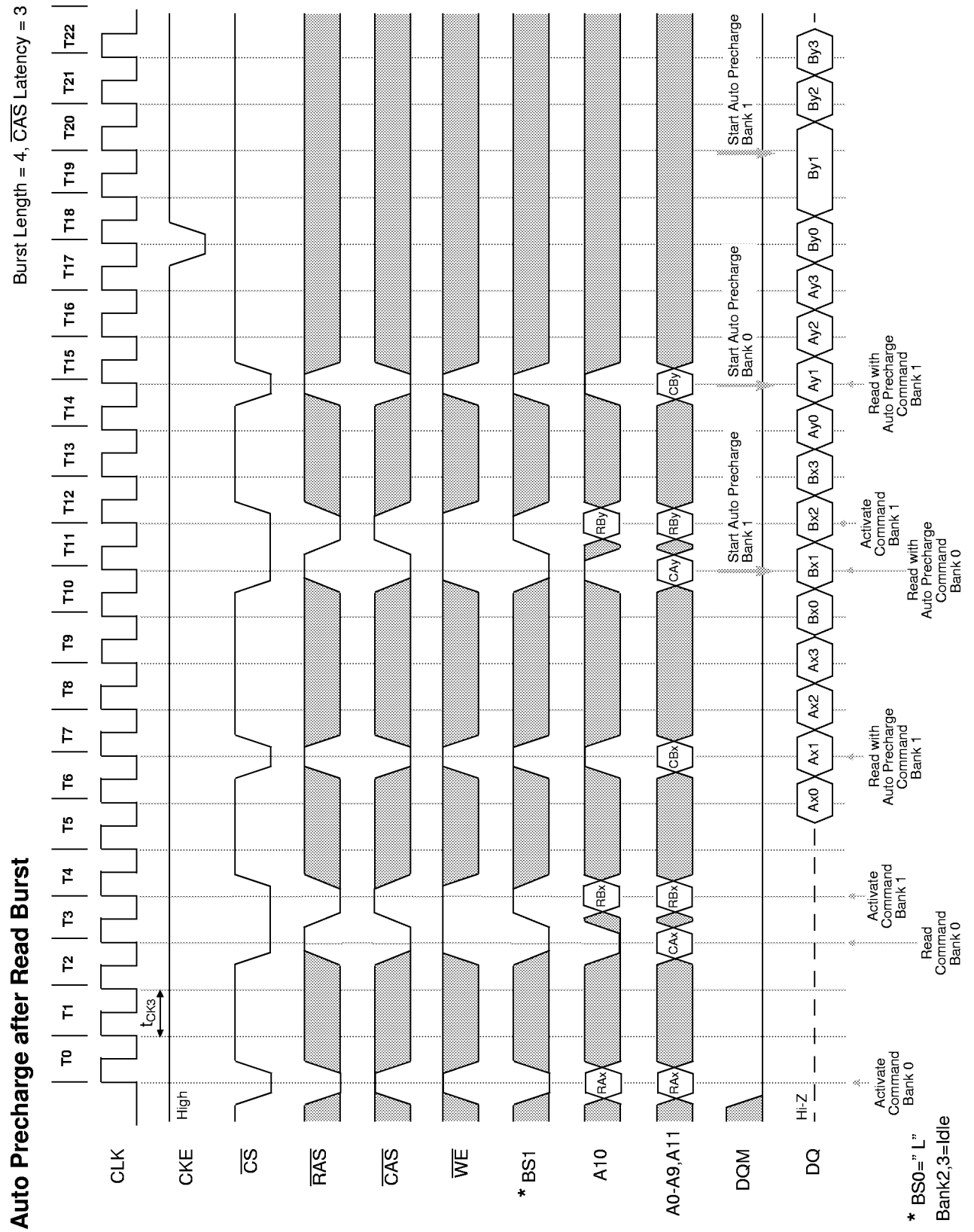


Interleaved Column Read Cycle



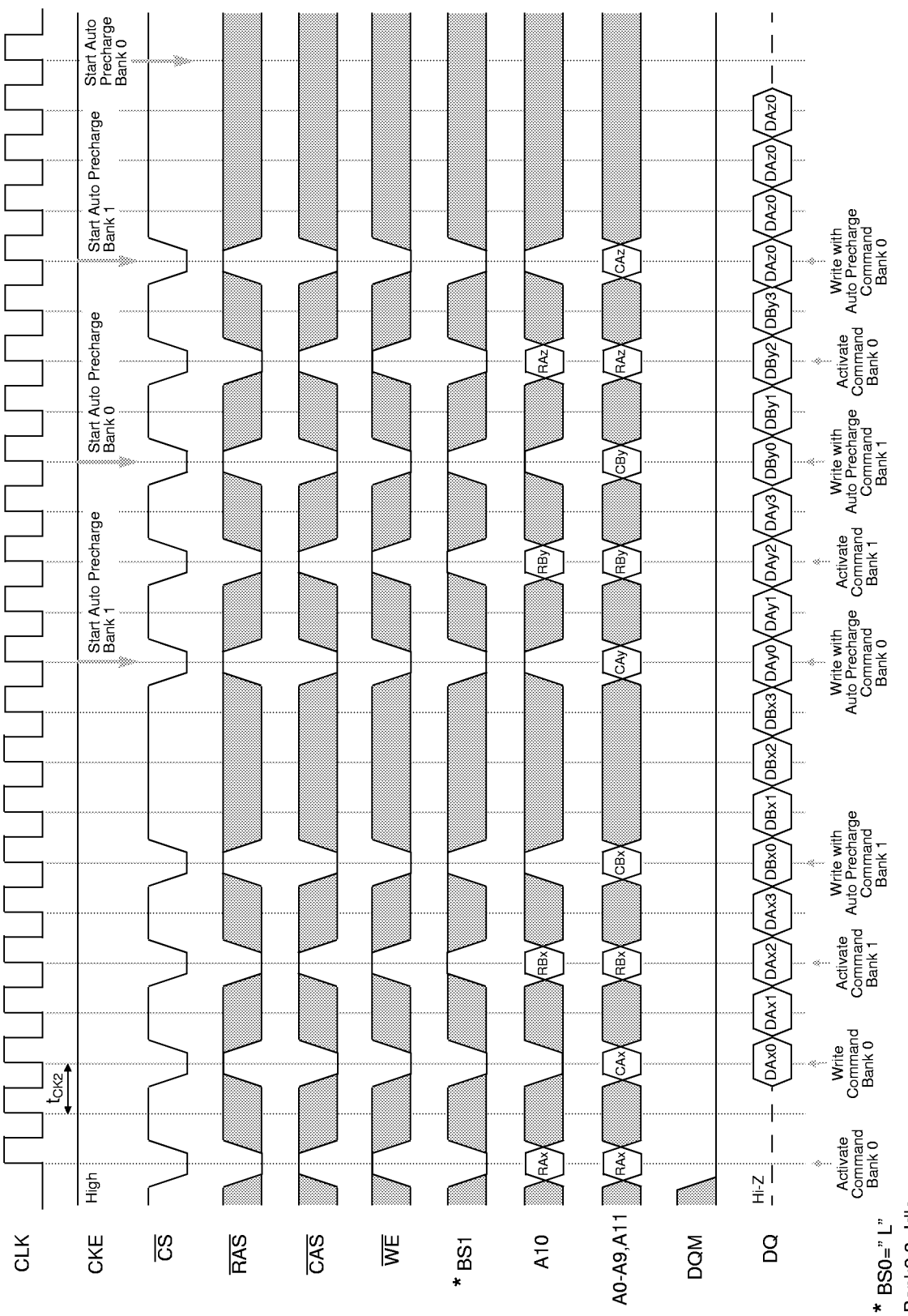
Auto Precharge after Read Burst

Burst Length = 4, $\overline{CAS}$ Latency = 3



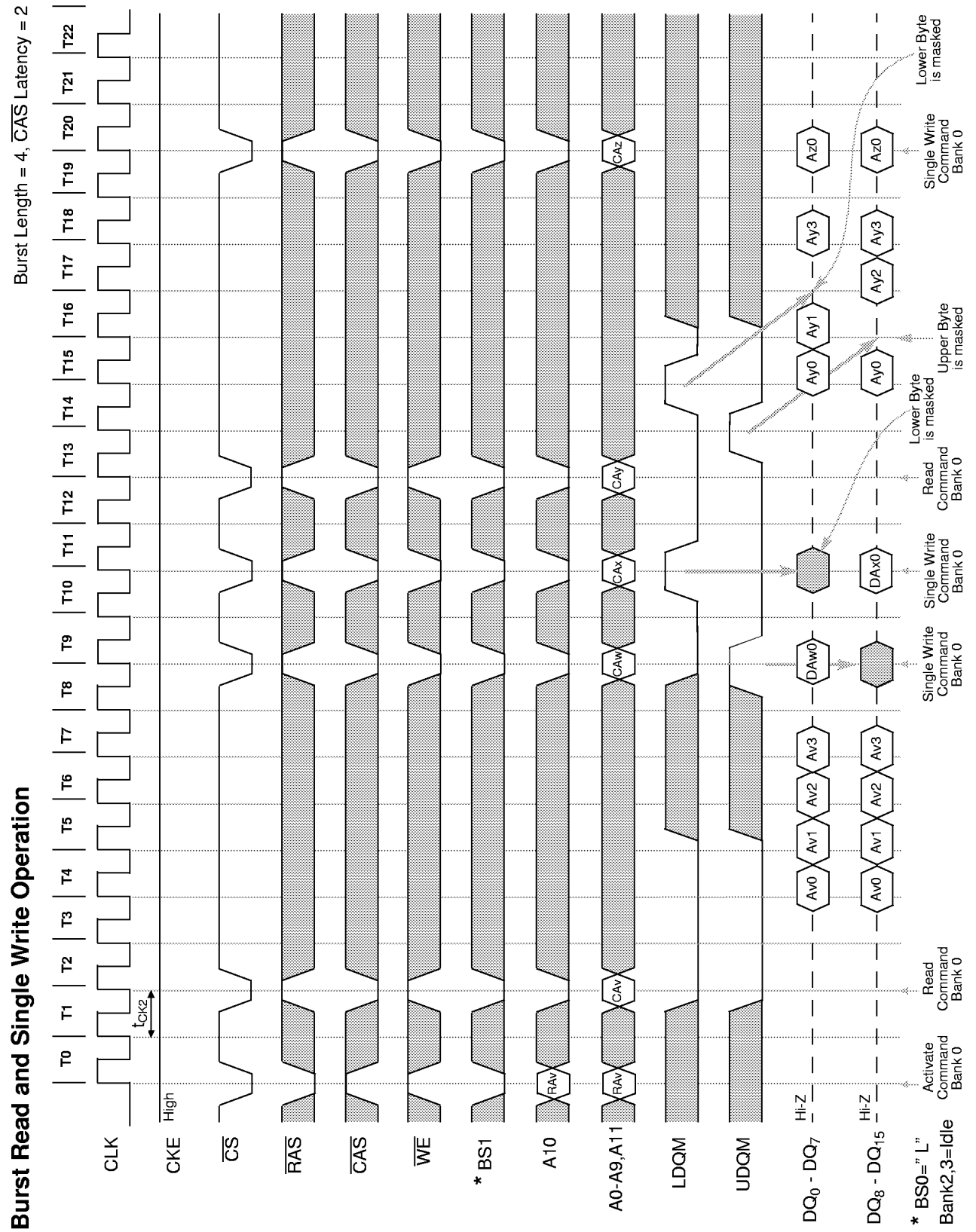
Auto Precharge after Write Burst

Burst Length = 4, $\overline{CAS}$ Latency = 2



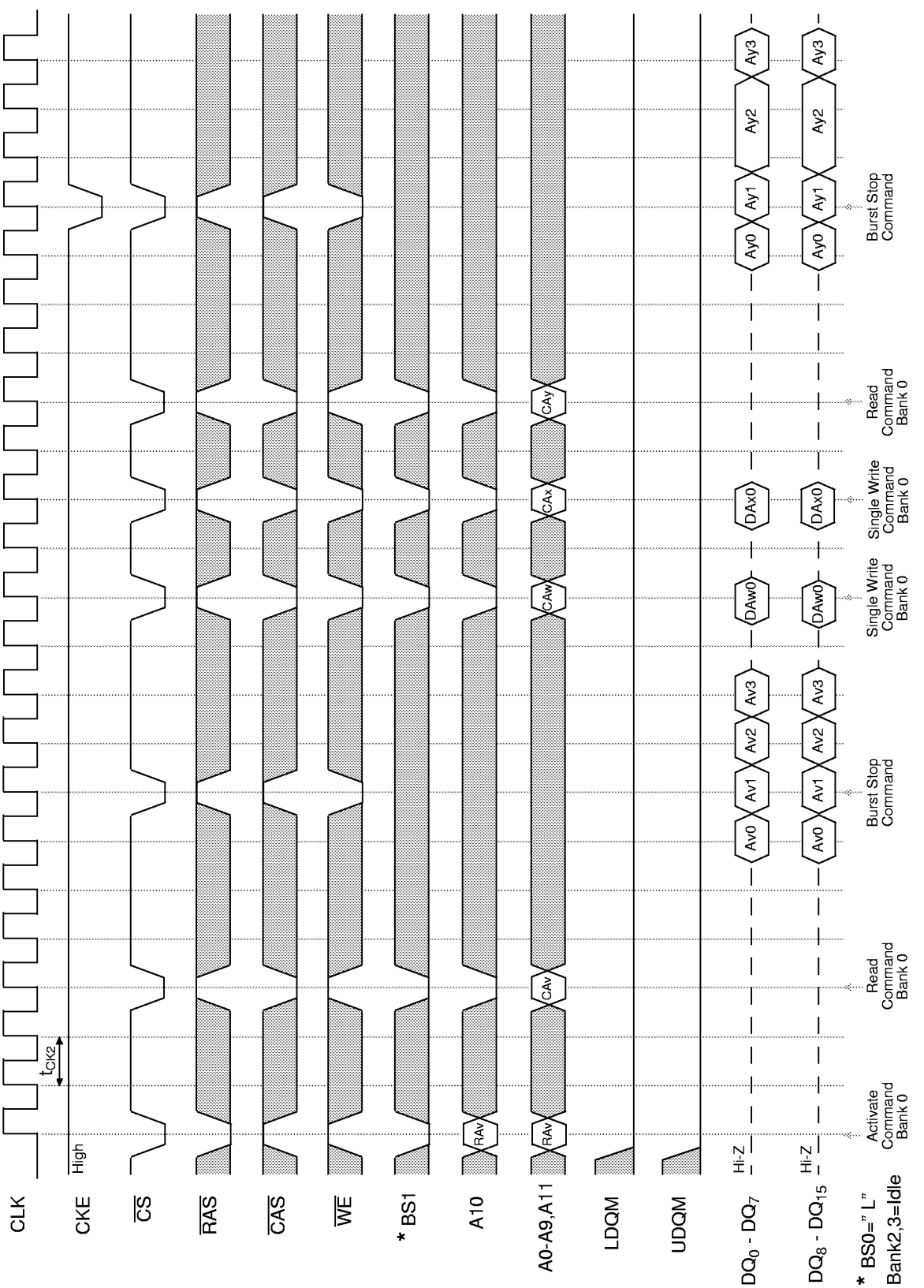
Burst Read and Single Write Operation

Burst Length = 4, $\overline{CAS}$ Latency = 2



Full Page Burst Read and Single Write Operation

Burst Length = Full Page, $\overline{CAS}$ Latency = 3



PACKAGE DIMENSIONS (400mil; 54 lead; Thin Small Outline Package)