Integrated Device Technology, Inc.

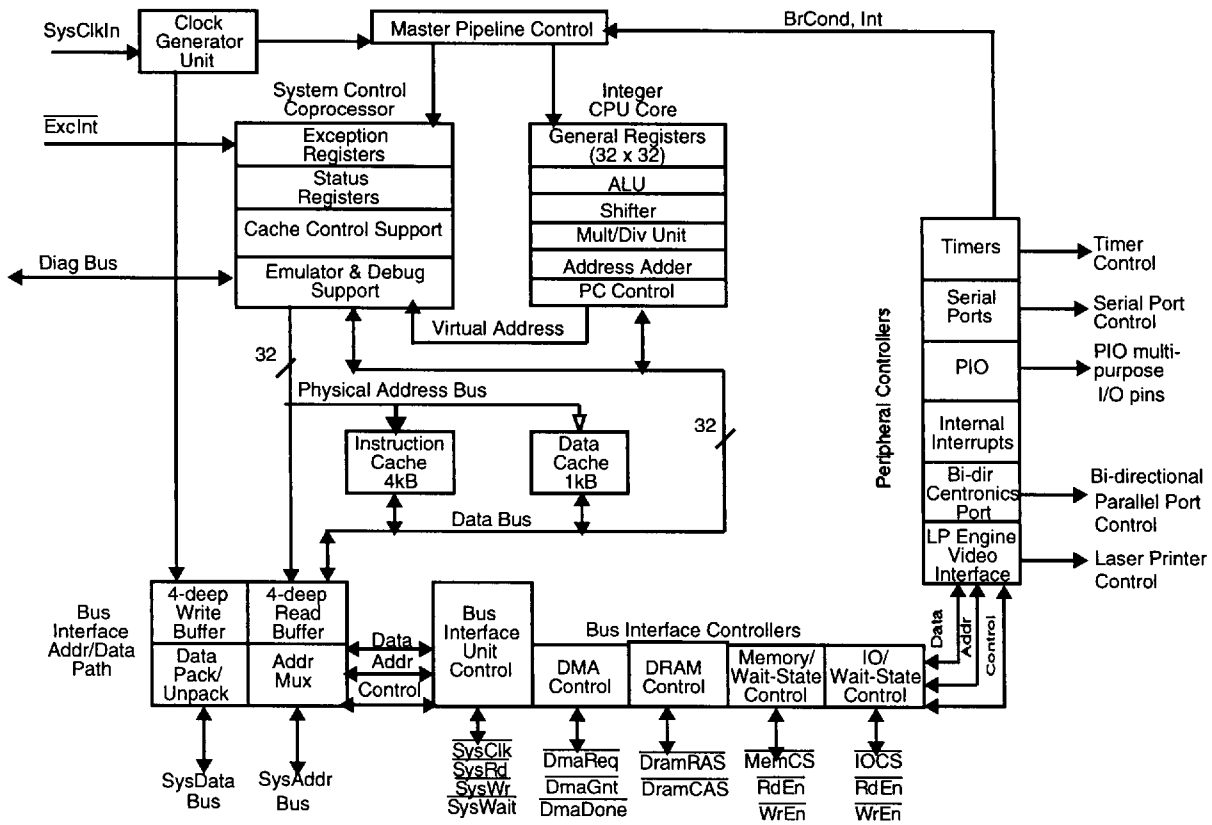
HIGHLY INTEGRATED RISController™

IDT79R36100™ Preliminary

FEATURES

- Instruction set compatible with the IDT RISController Family MIPS RISC CPUs
- System-level integration minimizes system cost
  - 32-bit RISC CPU
  - 4KB instruction cache on-chip
  - 1KB data cache on-chip
  - Memory, DMA and I/O controllers
  - System peripherals
- 24 MIPS/ 42K Dhrystone-2.1 at 25 MHz
- 31 MIPS/ 55K Dhrystone-2.1 at 33 MHz
- Improved cache control and cache locking
- Flexible bus interface allows simple, low cost designs
  - De-multiplexed address bus and data bus
  - On-chip 4-deep Read/Write buffer
  - Programmable bus width (8-,16-, and 32-bit)
- On-chip DRAM controller with Address Multiplexer
  - Supports optional interleaved DRAMs
- On-chip memory and I/O controller
  - Chip selects, wait-state generator
  - Supports optional interleaved ROMs
  - Supports PCMCIA Master protocol
- On-chip DMA controller
  - 4 internal channels, 2 external channelsOn-chip serial ports, timers, interrupt controller
- On-chip bi-directional IEEE 1284 Centronics™ Parallel Port interface
- On-chip laser printer video raster engine interface
- Built-in debug/emulator support
- 3.3V and 5V versions, MQUAD-208 and low cost PQFP-208 packaging

BLOCK DIAGRAM



DESCRIPTION

The IDT79R36100 is a highly integrated member of the IDT RISController family. The R36100 implements a "system on a chip," which includes the CPU core, cache memory, system logic functions, and application-specific peripherals. The 36100 is well-suited to a wide variety of cost sensitive and board space constrained embedded applications. The 36100's high level of integration greatly reduces system design challenges, substantially decreasing design risk and time to market.

The R36100 Integrated RISController is based upon the general purpose R3000A MIPS RISC CPU core and integrates substantial amounts of on-chip instruction cache and data cache memory. In addition to the CPU core and cache memory, the R36100 integrates on-chip all necessary system logic functions, including DRAM, ROM, I/O and DMA controllers; counter/timers; interrupt controllers; general purpose parallel I/O and debug support circuitry. The R36100 also integrates printer and data communication peripherals including an IEEE 1284 parallel port, laser printer video rasterizer, and two serial communications ports.

The R36100 Integrated RISController is software compatible with all members of the IDT RISController family, including the family of low-cost 32-bit R30xx RISControllers and the Orion family of high-performance 64-bit embedded controllers. The common instruction set architecture (ISA) enables the same applications software to be used across a wide variety of price/performance points.

The R36100 Integrated RISController has four on-chip bus controllers, which allows seamless interface with a wide variety of standard memories and peripherals, including:

- Standard page mode DRAM
- EPROM, FLASH, SRAM, Dual-Port SRAM
- FIFO, SCSI, A/D, and other I/O peripherals
- Ethernet, data compression, and other coprocessors

The R36100 Integrated RISController integrates an IEEE 1284 Centronics parallel port, RS-232C and Local Talk serial ports, and a laser printer video rasterizer to serve printer system applications, including:

- Monochrome laser and ink-jet printers
- Host-based printer cards
- Multi-function laser/fax printer systems

In addition, the R36100 Integrated RISController integrates asynchronous and synchronous serial controller channels and multiple timers to serve data communications applications, such as:

- Local Area Network (LAN) interface cards
- CSU/DSU SDLC/HDLC line driver cards
- Router, switcher, and data compression cards

HARDWARE OVERVIEW

The R36100 can be viewed as a "system on a chip"—a discrete system built around the R3000A CPU. By integrating the system functionality onto a single chip, dramatic reductions in cost, size, and power are achieved, reducing overall system complexity and minimizing system development time.

A block diagram of the R36100's functional units is included on page 1.

CPU Core

The R36100 Integrated RISController is based on the R3000A CPU core. The R3000A is a full 32-bit RISC integer execution engine, capable of sustaining a peak single cycle execution rate by using its five-stage pipeline. The CPU core contains an integer ALU unit and bit shifter with a separate integer multiplier/divider unit, address adder and program counter generator, and 32 orthogonal 32-bit registers. The R36100 execution core implements the MIPS-I instruction set architecture (ISA). Thus, the R36100 is binary compatible with all other MIPS CPU engines, including both the low-cost R30xx family and the high-speed R4600 ORION family.

System Control Co-Processor

The R36100 Integrated RISController also integrates a System Control Co-processor (CP0) on chip. CP0 manages the exception handling capability of the R36100, the virtual-to-physical address memory mapping of the R36100, and the various programmable bus-to-cache interface capabilities of the R36100. These topics are discussed in detail in the *IDT79R36100 Integrated RisController Hardware User's Manual.*

The R36100 does not include the optional Translation Lookaside Buffer (TLB) found in other members of IDT's RISController family, but it does perform the same virtual-to-physical address mapping as the base versions of the R30xx family. These base version devices support distinct kernel and user mode operation without requiring page management software or an on-chip TLB, thus allowing a simpler operating system software model and a lower cost processor.

Clock Generator Unit

The R36100 Integrated RISController is driven from a single, double frequency input clock. An on-chip clock generator manages the interaction between the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line that was required in discrete R3000A- based systems.

Instruction Cache

The R36100 Integrated RISController integrates 4KB of on-chip instruction cache, which is organized with a line size of 16 bytes (four 32-bit entries). This relatively large cache contributes substantially to the high performance available in the R36100, and allows even low-cost

memory systems, when based on the R36100, to achieve high performance. The cache is implemented as a direct mapped cache, capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switches.

To improve real-time performance, the R36100 instruction cache supports a cache locking mechanism. Each cache can be split into two halves or four quarters, allowing each half or quarter to service a different area of the large address space. This feature enables the system software to "lock" time-critical code—such as router address hash-table lookup algorithms and interrupt service routines—into one of the halves or quarters, while allowing use of the unused portions without affecting the locked time-critical code. This technique allows software to perform instruction cache locking and ensures deterministic response.

Data Cache

The R36100 Integrated RISController incorporates an on-chip data cache of 1KB, which is organized as a line size of 4 bytes (one word). This relatively large data cache contributes substantially to the high performance inherent in the R36100. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write-through cache to insure that main memory is always consistent and coherent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer that captures address and data at the processor execution rate. This feature allows data to be retired to main memory at a much slower rate without impacting the performance of the internal CPU pipeline.

The R36100 supports data cache locking with the same mechanism used to support instruction cache locking. The 36100 allows the data cache to be split into two halves or quarters, each half or quarter servicing a different area of the large address space. This enables the system software to lock time-critical data—such as routing address information tables and the interrupt stack—into one of the halves or quarters, while allowing other tasks to utilize the unused portions without disrupting the critical data. This technique allows software to perform data cache locking without requiring memory management support.

Bus Interface Unit

The R36100 Integrated RISController uses its large internal caches to provide the majority of its memory bandwidth requirements to/from the execution engine. The execution engine pipeline can access both one instruction and one data load/store per clock cycle. The R36100 requires access to main memory only on write operations and the relatively rare cache miss. Thus, the R36100 can utilize a simple bus interface that connects to slow memory devices without sacrificing performance.

The R36100 bus interface utilizes a de-multiplexed address and data bus. This interface readily connects to memory subsystems that are 8-, 16-, or 32-bits wide, and/or interleaved.

The R36100 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture the processor's address and data information during internal store operations, storing them as FIFO at a rate of up to one store per clock. The write buffer then presents the bus interface write transactions at the rate the memory system can accommodate.

During main memory writes, the R36100 can break large data—such as a 32-bit word—into a series of smaller transactions—such as bytes—according to the width of the memory port being written. This operation is transparent to the software that initiated the store, and insures that the same software can run across multiple platforms that have different memory system configurations.

The R36100 read interface performs both single data reads and quad word reads. In order to accommodate slower reads, the R36100 incorporates a 4-deep read buffer FIFO, so that the external interface can queue data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R36100 can perform on-chip data packing when performing large data reads—such as quad words—from narrower memory systems—such as 16-bit. Once again, this operation is transparent to the actual software, which simplifies migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, the R36100 easily supports 8-, 16-, 32-bit, or interleaved boot PROMs.

Memory Controller

The R36100 Integrated RISController uses the on-chip memory controller to gluelessly attach external ROM (including FLASH) and/or SRAM in a number of system configurations. For example, the memory controller supports interleaved ROM and/or SRAM, 8-bit boot ROM, 32-bit burst ROMs, and a simple 32-bit wide EPROM array. The memory controller integrates all of the control signals as well as managing the access timing and wait-state generation for multiple banks, all under the control of boot software.

DRAM Controller

The R36100 Integrated RISController integrates an on-chip DRAM controller. The DRAM controller directly

controls up to four banks of standard page mode DRAMs in a number of configurations, including systems with varying densities of DRAM, interleaved DRAM, and 16- and 32-bit wide DRAM subsystems.

I/O Controller

The R36100 Integrated RISController has an on-chip I/O controller that performs all necessary address decoding and wait-state generation for external I/O devices. In addition, the on-chip I/O controller readily interfaces as a master to PCMCIA, including support of the large address space required and the PCMCIA chip-select protocol and timing.

DMA Control

The R36100 Integrated RISController provides on-chip DMA control for internal peripherals, external peripherals, and external memory. Multiple internal channels allow block moves of data between any combination of memory and I/O. Each channel can also be interrupt controlled, which allows an I/O peripheral, such as the serial port, to regulate the individual transactions of a block move.

The R36100 Integrated RISController also supports external DMA masters, which take over the external system bus via a bus request and grant handshake. Once in control of the system bus, the external DMA master can read and write to memory, I/O, and internal peripherals via the R36100's bus controllers.

Counter/Timers

The R36100 Integrated RISController contains three general purpose timers. Each timer consists of a 16-bit count register as well as a 16-bit compare register. The count register resets to zero and then counts upward until it equals the compare register. When the count register equals the compare register, the TCN output is asserted and the count is reset to zero. To support intervals longer than 2^{16} ticks, the timers use a common 16-bit prescaler counter. Each timer can be programmed to select a power-of-2 divisor of the prescaler. Using these features, each timer can be utilized as a general purpose real-time clock, bus timeout timer, watch-dog timer, PWM/square wave/baud rate generator or gated clock external event counter.

PIO Interface

For controlling multi-purpose utility pins, the R36100 Integrated RISController has a Parallel Input/Output (PIO) interface. The PIO pins can be programmed to act as general purpose inputs or outputs. Each PIO pin is also multiplexed with other controllers' inputs or outputs. This flexible arrangement allows system designers to customize the R36100's resources according to their needs. Thus, designs needing a special purpose controller—such as the laser printer video controller—can allocate the laser printer video pins for that purpose. Applications that do not require the laser printer video—such as data communications—can use those pins for general purpose inputs or outputs.

Serial Communications Controller

The R36100 Integrated RISController integrates a dual channel serial port. This peripheral controller can perform a variety of synchronous and asynchronous protocols, including RS-232C, LocalTalk, SDLC, and HDLC. To maximize throughput, there is an option to service the on-chip serial port by the auto-initiated on-chip DMA controller, which can perform automatic block moves of data to and from the port.

Interrupt Controller

The R36100 Integrated RISController integrates an on-chip interrupt controller to manage both external interrupts and interrupts that are signaled from the on-chip peripherals. The interrupt controller improves internal interrupt servicing speed, assists in interrupt prioritization and nesting, and interfaces with the auto-initiated DMA.

IEEE 1284 Bi-directional Parallel Port

The R36100 Integrated RISController includes an internal IEEE1284 Centronics parallel port peripheral, which implements a true bi-directional port. Features include:

- 8-bit input target compatible protocol, for backward compatibility with legacy PCs
- nibble and byte mode output protocol, for backward compatibility with most PCs
- ECP protocol, for the emerging Laser Printer PC standard
- EPP protocol, for datacom applications
- External transceiver interface control pins
- Auto-initiated DMA via internal interrupts

Laser Printer Video Interface

The R36100 Integrated RISController integrates an on-chip laser printer video/control interface. This peripheral provides support for the following:

- 1-bit serial stream laser printer or raster engine interface
- On-chip FIFO
- Programmable margin widths and page lengths
- Auto-initiated DMA via internal interrupts

PERFORMANCE OVERVIEW

The following features allow the R36100 Integrated RISController to achieve a high performance level:

- An efficient execution engine. The CPU performs ALU operations and store operations in a single cycle, has an effective load time of 1.3 cycles and branch execution rate of 1.5 cycles based on the ability of the compilers to avoid software interlocks. Thus, the R36100 achieves over 24 dhrystone MIPS performance at 25MHz.
- Large on-chip caches. The R36100 contains caches that are substantially larger than most embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R36100 to achieve actual sustained performance that is very close to its peak execution rate, even with low cost memory systems.
- Autonomous multiply and divide operations. The R36100 features an on-chip integer multiplier/divide unit that is separate from the other ALU. This allows the R36100 to perform multiply or divide operations in parallel with other integer operations by using a single multiply or divide instruction rather than "step" operations.
- Integrated write buffer. The R36100 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires them to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support. The R36100 enables the system designer to utilize page, static, or nibble mode RAMs when performing read operations. This minimizes the main memory read penalty and increase the effective cache hit rates.
- Tightly coupled memory system. System resources can be accessed and managed efficiently for the needs of the execution core when memory controllers are integrated on-chip.

SELECTABLE FEATURES

Boot-time selectable features are:8/16 or 32-bit PROM support and Big/Little Endian selection. Other selectable, register-configurable features are:

- Number of wait states for different memory and I/O controllers
- Memory and I/O map configuration
- 16 or 32-bit DRAM and 8/16 or 32-bit memory and I/O
- Interleaved or non interleaved memory/DRAM
- Programmable control signals timing for all controllers
- Selectable PIO
- Selectable transceivers type for all controllers (FCT 260/FCT245/FCT543)
- Selectable I/O style (Motorola/Intel/PCMCIA)

DEVELOPMENT SUPPORT

The R36100 is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis and emulator tools, and sub-system modules.

Figure 1 presents an overview of the system development process that is typically used when developing R36100 applications. The R36100 family is supported in all phases of project development. The following list of tools allow timely, parallel development of hardware and software for R36100 based applications:

- IDT/c compiler, based on the GCC/GNU tool chain.
- Cross development tools, available for a variety of development environments.
- High-performance IDT floating point emulation library software.
- IDT Evaluation Boards, which include RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT laser printer system boards, which directly drive a low-cost print engine.
- Adobe PostScript Page Description Language running on the IDT R3051 family.
- IDT/sim PROM Monitor, which implements a full PROM monitor, including diagnostics, remote debug support, and peek/poke.
- IDT/kit™ (Kernel Integration Toolkit), which provides library support and a framework for the system run-time environment.
- Logic analyzer and in-circuit emulator support for fast debugging and hardware/software integration.

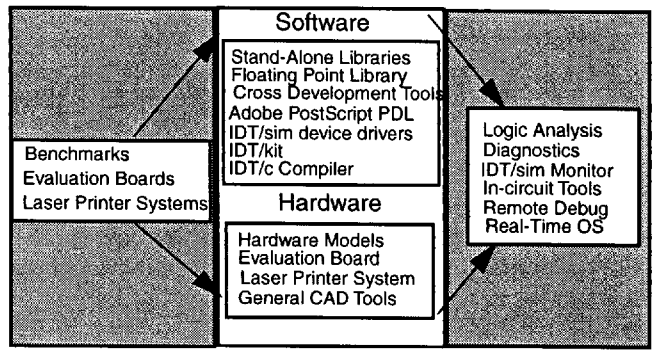


Figure 1. Development Support

SYSTEM USAGE

The IDT79R36100 Integrated RISController is specifically designed to easily implement low-cost memory systems. Typical low-cost memory systems use EPROMs and DRAMs, as well as application specific peripherals. Some embedded systems also optionally contain or substitute DRAM with static RAMs.

Figure 2 demonstrates the low-system cost inherent in the R36100. In this example system, which is typical of a low-cost laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. Other embedded systems could optionally use an 8-bit or a 16-bit PROM, or even an interleaved 64-bit interface. A 16-bit font cartridge interface is provided through PCMCIA for add-in cards and a 32-bit page buffer DRAM is used for high-resolution.

In this example, a field or manufacturing upgrade to a larger page buffer is supported by the boot software and DRAM controller. Such a system features a very low entry price, with a range of field upgrade options. Note that the performance of the R36100 allows software frame buffer compression to be effective in reducing system DRAM while maintaining expected performance.

THERMAL CONSIDERATIONS

The R36100 utilizes special packaging techniques to improve the thermal properties of high-speed processors. These packages effectively dissipate the power of the CPU, increasing device reliability.

The lowest cost packaging available uses a standard cavity-down, injection molded PQUAD package (the "PF" package). This package, coupled with the power reduction techniques employed in the R36100's design, allows operation at speeds to 25MHz; however, at higher speeds, additional thermal care must be taken.

For this reason, the R36100 is also available in the MQUAD package (the "MS" package), which is an all-aluminum package with the die attached to a normal copper lead frame mounted to the aluminum casing.

Due to the heat-spreading effect of the aluminum, the MQUAD package allows for a more efficient thermal transfer between the die and the case. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation.

The R36100 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures (where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device):

$$T_A = T_C - P * \varnothing_{CA}$$

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 1.

	$\varnothing_{CA}$					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
MQUAD	20	12	9	8	7	6
PQFP	38	31	28	26	25	24

Table 1. Thermal Resistance ($\varnothing_{CA}$) at Various Airflows

Note: The R36100 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79R36100 Integrated RISController Hardware User's Manual*, Version 1.1.

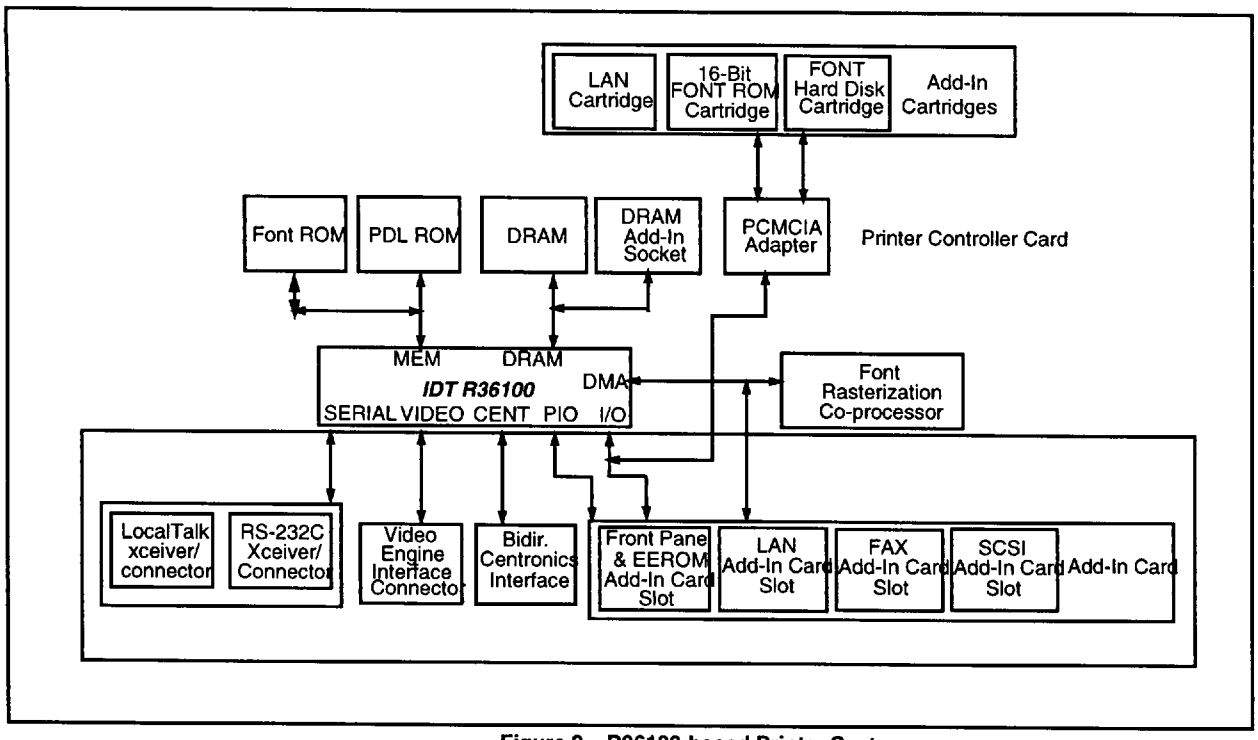


Figure 2. R36100-based Printer System

DATA SHEET REVISION HISTORY

This is the first revision of the data sheet.

Changes to version dated January 1996:

Features:
- Added 33 MHz Dhrystone data

System Usage:
- In Figure 2, clarified directional arrows.

AC Timing Characteristics:
- Reorganized table according to Symbol parameter column

AC Electrical Characteristics:
- Added tsys parameter info to table.
- In Figure 3, ClkIn label changed to Clk.

DC Electrical Characteristics:
- Added 3.3V table.

Valid Combinations:
- Added 2-letter package identifier to each item.

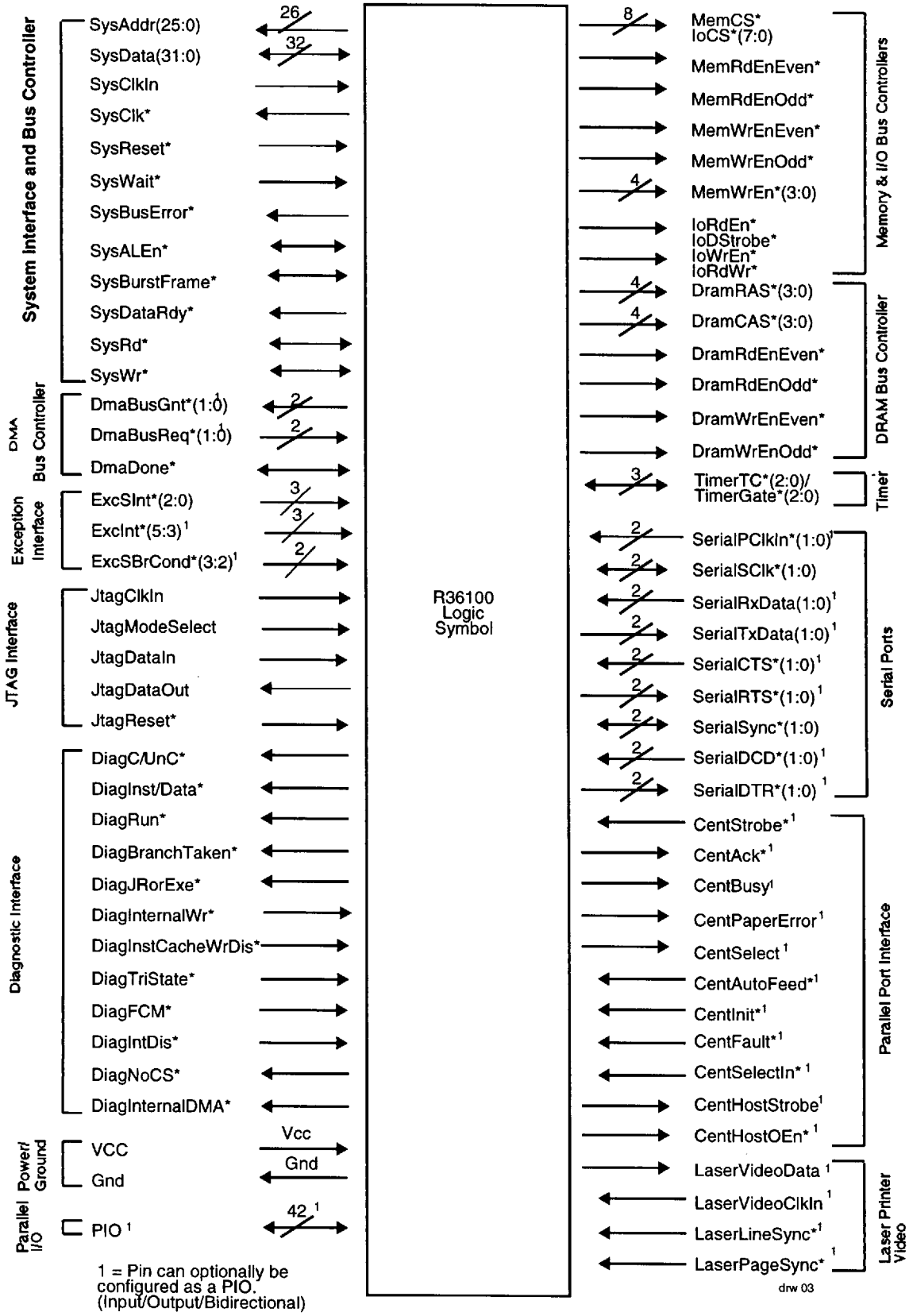
Changes to version dated April 1996:

Logic symbol diagram:
- Signal name corrections: SysALEn*, SysBurstFrame*, and SysDataRdy*.

Package Pin-out:
- Pin name changes: Pin 1 = N/C, Pin 96 = DramWrEnEven*, Pin 100 = DramWrEnOdd*, Pin 104 = N/C, Pin 139 = LaserVideoClkIn, Pin 166 = SerialPClkIn*, and Pin 167 = SerialSClk*.

PIN INFORMATION —R36100

Logic Symbol



1 = Pin can optionally be configured as a PIO. (Input/Output/Bidirectional)

PIN DESCRIPTIONS

The following is a list of interface, interrupt, and miscellaneous pins available on the R36100. Pin names marked with an asterisk (*) are active when low.

Pin Name	Type	Description
System Bus Interface Pins		
SysAddr(25:0)	Output	System Address Bus. Also serves as the DramAddr(13:2) Bus.
SysData(31:0)	Input/Output	System Data Bus.
SysClkIn	Input	System Clock Input. Twice (2x) the internal CPU frequency.
SysClk*	Output	System Clock Output. All other outputs are referenced to this system clock.
SysReset*	Input	System Reset. Initializes entire chip, except for JTAG circuitry.
SysWait*	Input	System Way. Extends current bus transaction.
SysBusError*	Input	System Bus Error. Terminates current bus transaction.
SysALEn*	Output/Input(DMA)	System Address Latch Enable. Indicates valid address at the beginning of a bus transaction.
SysBurstFrame*	Output/Input(DMA)	System Burst Frame. First indicates the beginning of a bus transaction. Then indicates if the bus transaction is a burst and if the next data is the last data.
SysData Rdy*	Output	System Data Ready. Indicates valid data during each data of a bus transaction (except when SysWait is asserted).
SysRd*	Output/Input(DMA)	System Read. Indicates current bus transaction is a read.
SysWr*	Output/Input(DMA)	System Write. Indicates current bus transaction is a write.
DRAM Controller Pins		
DramRAS*(3:0)	Output	DRAM Row Address Strobe.
DramCAS*(3:0)	Output	DRAM Column Address Strobe.
DramRDEnEven*	Output	DRAM Read Enable for Even FCT245/543 Type Banks. On FCT260 type banks, it is the read enable for both.
DramRdEnOdd*	Output	DRAM Read Enable for Odd FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
DramWrEnEven*	Output	DRAM Write Enable for Even Banks.
DramWrEnOdd*	Output	DRAM Write Enable for Odd Banks.

Pin Name	Type	Description
Memory Controller Pins		
MemCS/IoCS*(7:0)	Output	Memory or I/O Chip Selects. MemCS(0) and optionally MemCS(1) are reserved for the Boot PROM. IoCS(6) and/or IoCS(7) are optionally reserved for the Centronics Port if used.
MemRdEnEven*	Output	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type banks, it is the read enable for both even and odd banks.
MemRdEnOdd*	Output	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
MemWrEn*(3:0)	Output	Memory Write Enable for each byte lane. Memories can directly connect their byte write enables to the R36100 MemWrEn*(3:0) signals. During 16-bit accesses, either MemWrEn*(3:2) or MemWrEn*(1:0) are used, both pairs are equivalent.
IoRdEn/DStrobe*	Output	I/O Read Enable or I/O Data Strobe.
IoWrEn/RdWr*	Output	I/O Write Enable or I/O Read/Write.
DMA Controller Pins		
DmaBusGnt*(1:0)	Output	DMA Bus Grant Indicates that the CPU has tri-stated the bus and other DMA related signals.
DmaBusReq*(1:0)	Input	DMA Bus Request. Indicates that external DMA agent would like control of the bus and other DMA related signals.
DmaDone*	Input/Output	DMA transaction done
Serial Port Pins		
SerialPClkIn*(1:0)	Input	Optional Primary Serial Clock Input.
SerialSClk*(1:0)	Input/Output	Optional Secondary Serial Clock Input or Output.
SerialRxData(1:0)	Input	Serial Receiver Data Stream.
SerialTxData(1:0)	Output	Serial Transmitter Data Stream.
SerialCTS*(1:0)	Input	Serial Clear To Send.
SerialRTS*(1:0)	Output	Serial Request To Send.
Serial Sync*(1:0)	Input/Output	Serial Frame Sync.
Serial DCD*(1:0)	Input	Serial Data Carrier Detect.
SerialDTR*(1:0)	Output	Serial Data Terminal Ready.
Timer Pins		
TimerTC*(2:0) /TimerGate*(2:0)	Input/Output	Timer Terminal count output or Timer Count Gate Enable input. Terminal count asserts when Timer Count equals 0. Timer Gate enables counter to count upward or to stop.
PIO Pins		
PIO(41:0)	Input/Output	Parallel Inputs or Parallel Outputs. Parallel inputs and parallel outputs are multiplexed with various peripheral inputs and peripheral outputs. If the peripheral is unused, the input or output pin can be reconfigured to be a general purpose input or output, respectively.

Pin Name	Type	Description
Bi-Directional Centronics Interface Pins		
CentStrobe*	Input	Centronics Strobe. In compatible mode, strobes data into the printer. Has other uses for other modes.
CentAck*	Output	Centronics Acknowledge. In compatible mode, acknowledges a strobe. Has other uses for other modes.
CentBusy	Output	Centronics Busy. In compatible mode, delays the host from sending more data. Has other uses for other modes.
CentPaperError	Output	Centronics Paper Out/Jam Error. In Compatible mode, indicates that the printer has a paper error when asserted with CentFault. Has other uses for other modes.
CentSelect	Output	Centronics Select. In Compatible mode, used to indicate that this printer is on-line. Has other uses for other modes.
CentAutoFeed*	Input	Centronics Auto Page Feed. In compatible mode, sends a paper feed to the printer. Has other uses for other modes.
CentInit*	Input	Centronics Initialization/Reset. In Compatible mode, resets the printer. Has other uses for other modes.
CentFault*	Output	Centronics Fault. In Compatible mode, indicates that the printer has a problem. Has other uses for other modes.
CentSelectIn*	Input	Centronics Select In. In Compatible mode, indicates that the Host wants to select this printer on a shared cable. Has other uses for other modes
CentHostStrobe	Output	Centronics Host Strobe. Used to latch Host data on the external FCT952/374 data transceiver during a Host write.
CentHostOEn*	Output	Centronics Host Output Enable. Used to enable the external FCT952/374 data transceiver during a Host read.
Laser Engine Interface Pins		
LaserVideoData	Output	Laser Video Data Stream.
LaserVideoClkIn	Input	Laser Video Clock Input. Accepts either the (1x) Video Data Stream frequency or 8 times (8x) the PLL frequency.
LaserLineSync*	Input	Laser Line Sync. Indicates that the laser drum is ready to start accepting data for a new line.
LaserPageSync*	Input	Laser Page Sync. Indicates that the laser drum is ready to start a new page.

Pin Name	Type	Description
Debug/Emulator Interface Pins		
JtagClkIn	Input	JTAG Clock Input (TCK). Test mode serial boundary scan input clock.
JtagModeSelect	Input	JTAG Mode Select (TSEL). Test mode serial boundary scan command data. In normal operating mode, JtagModeSelect should be left unasserted high.
JtagDataIn	Input	JTAG Data In (TDI). Test mode serial boundary scan register data input.
JtagDataOut	Output	JTAG Data Out (TDO). Test mode serial boundary scan register data output.
JtagReset*	Input	TAG Reset (TRES*). Resets the JTAG test circuitry. Does not reset any other chip functions.In normal operating mode, JtagReset should be left asserted low.
Diagnostic Pins		
DiagC/UnC*	Output	Diagnostic Cached versus Uncached. On read bus transactions indicates whether the read is cached or uncached.
DiagInst/Data*	Output	Diagnostic Instruction versus Data. On read bus transactions indicates whether the read is for instructions or data.
DiagRun*	Output	Diagnostic Run. Indicates an internal pipeline run cycle. This pin has iso-synchronous timing.
DiagBranchTaken*	Output	DiagBranchTaken Indicates that a branch, jump, or exception has been taken. This pin has asynchronous timing.
DiagJRorExe*	Output	Diagnostic Jump Register or Exception occurring. Indicates that a jump register or exception is executing. This pin has asynchronous timing.
DiagInternalWr*	Output	Diagnostic Internal Write. Indicates that a MTCO to CP0 register $3 is occurring.
DiagInstCacheWrDis*	Output	Diagnostic Cache Write Disable. Disables writes to the instruction and data cache. This pin has iso-synchronous timing and is not recommended for functional use.
DiagTriState*	Input	Diagnostic Tri-State all outputs. All outputs are tri-stated including SysClk. This pin is asynchronous such that tri-stating asserts or de-asserts output enables immediately.
DiagFCM*	Input	Diagnostic Force Cache Miss. This pin has iso-synchronous timing. If used for functional board tests, it is recommended that it be (de-)asserted statically at reset time and left (de-)asserted.
DiagIntDis*	Input	Diagnostic Interrupt Disable.
DiagNoCS*	Output	Diagnostic No Chip Select. No internal or external chip select has occurred for the current bus transaction, therefore an external state machine should handle the bus transaction.
DiagInternalDMA*	Output	Diagnostic Internal DMA. Asserts whenever any of the Internal DMA channels is generating the current bus transaction.

Pin Name	Type	Description
Exception Handling Pins		
ExcSInt*(2:0)	Input	Exception Synchronized Interrupts. Also used as the reset initialization vector for 2:Boot16, 1:Boot8, and 0:BigEndian modes.
ExcInt*(4:3)	Input	Exception Interrupts.
ExcSBrCond(3:2)	Input	Exception Synchronized Branch Condition inputs.
Power/Ground Pins		
Vcc	Input	Power pin. All power pins must be connected. 5V or 3.3V depending on part type.
Gnd	Input	Ground pin (VSS). All ground pins must be connected. 0V.

AC TIMING CHARACTERISTICS — R36100

(Tc=0°C to +85°C, Vcc = +3.3V±5% and +5V±5%)

Signal	Symbol	Reference Clock Edge	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
System Bus Interface									
SysData(31:0), SysRd*, SysWr*, SysALEn*, SysBurstFrame*, SysWait*, SysBusError	Tsetup	Sysclk rising	13	--	11	--	9	--	ns
SysData(31:0), SysRd*, SysWr*, SysALEn*, SysBurstFrame*, SysDataRdy*	Tpd	Sysclk rising	--	16	--	14	--	12	ns
SysData(31:0), SysRd*, SysWr*, SysALEn*, SysBurstFrame*, SysWait*, SysBusError*	Thold[a]	Sysclk rising	1	--	1	--	1	--	ns
SysAddr(25:0)	Tpdaddr	Sysclk rising	—	13	—	11	—	9	ns
DRAM Controller									
DramRAS(3:0)*, DramCAS(3:0)*, DramRdEnEven* DramRdEnOdd*, DramWrEnEven*, DramWrEnOdd*	Tpd	Sysclk rising	—	16	—	14	—	12	ns
Memory Controller									
MemCS/IoCS(7:0)*, MemRdEnEven*, MemRdEnOdd*, MemWrEnEven*, MemWrEOdd*, MemWrEn*, IoRdEn/Dstrobe*, IoWrEn/RdWr*	Tpd	Sysclk rising	—	16	—	14	—	12	ns
DMA Controller									
DmaBusGnt*, DmaDone*	Tpd	Sysclk rising	—	16	—	14	—	12	ns
DmaBusReq(1:0)*, DmaDone*	Tsetup	Sysclk rising	13	--	11	--	9	--	ns
DmaBusReq(1:0)*, DmaDone*	Thold[a]	Sysclk rising	1	--	1	--	1	--	ns
Serial Port									
SerialPClkIn(1:0)*,SerialRxData(1:0),SerialDCD(1:0), SerialCTS(1:0)*, SerialSClk(1:0)*, SerialSync(1:0)*	Tsetup	Sysclk rising	13	--	11	--	9	--	ns
SerialPClkIn(1:0)*,SerialRxData(1:0),SerialDCD(1:0), SerialCTS(1:0)*, SerialSClk(1:0)*, SerialSync(1:0)*	Thold[a]	Sysclk rising	1	--	1	--	1	--	ns
SerialSClk(1:0)*, SerialSync(1:0)*, SerialTxData(1:0), SerialRTS(1:0), SerialDTR(1:0	Tpd	Sysclk rising	—	16	—	14	—	12	ns
Timer									
TimerTC(2:0)/TimerGate(2:0)	Tsetup	Sysclk rising	13	--	11	--	9	--	ns
TimerTC(2:0)/TimerGate(2:0)	Tpd	Sysclk rising	--	16	--	14	--	12	ns

Signal	Symbol	Reference Clock Edge	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
TimerTC(2:0)/TimerGate(2:0)	Thold[a]	Sysclk rising	1	--	1	--	1	--	ns
PIO									
PIO(41:0)	Tsetup	SysClk rising	13	--	11	--	9	--	ns
PIO(41:0)	Tpd	SysClk rising	--	16	--	14	--	12	ns
PIO(41:0)	Thold[a]	SysClk rising	1	--	1	--	1	--	ns
Bidirectional Centronics Interface									
CentStrobe*, CentAutoFeed*,CentInit*, CentSelectIn*	Tsetup	Sysclk rising	13	--	11	--	9	--	ns
CentStrobe*, CentAutoFeed*,CentInit*, CentSelectIn*	Thold[a]	Sysclk rising	1	--	1	--	1	--	ns
CentAck*, CentBust,CentPaperError,CentSelect,CentFault, CentHostStrobe,CentHostOEn*	Tpd	Sysclk rising	—	16	—	14	—	12	ns
Laser Engine Interface									
LaserVideoData	Tpd	LaserVideo ClkIn rising (Pll off)	—	16	—	14	—	12	ns
LaserLineSync*,LaserPageSync*	Tsetup	LaserVideo ClkIn rising (Pll off)	13	--	11	--	9	--	ns
LaserLineSync*,LaserPageSync*	Thold[a]	LaserVideo ClkIn rising (Pll off)	0	--	0	--	0	--	ns
Debug/Emulator Interface									
JtagModeSelect, JtagDataIn, JtagReset*	Tsetup	JtagClkin rising	13	--	11	--	9	--	ns
JtagModeSelect, JtagDataIn, JtagReset*	Thold[a]	JtagClkin rising	0	--	0	--	0	--	ns
JtagDataout	Tpd	JtagClkin falling	—	16	—	14	—	12	ns
Exception Handling									
ExcSInt(2:0)*, ExcInt(4:3)*, ExcSBrCond(3:2)	Tsetup	Sysclk falling	13	--	11	--	9	--	ns
ExcSInt(2:0)*, ExcInt(4:3)*, ExcSBrCond(3:2)	Thold[a]	Sysclk rising	0	--	0	--	0	--	ns

a. There is no hold time required for inputs (Tholdin=0 min). Hold time on all output is 1 ns. (Tholdin=0 min, Tholdout = 1 ns max).

AC ELECTRICAL CHARACTERISTICS — R36100

(Tc=0°C to +85°C, Vcc = +3.3V±5%)

Symbol	Signal	Description	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
tclkh	clkIn	Pulse Width High	10	—	8	—	6.5	—	ns
tclkl	clkIn	Pulse Width Low	10	—	8		6.5	—	ns
tClk	clkIn	Clock Period	25	250	20	250	15	250	ns
tcold	Reset	Pulse Width From Vcc Valid	200	—	200	—	200	—	µs
twarm	Reset	Minimum Pulse Width	32	—	32	—	32	—	Sys
tsysh	SysClk	Clock High Time	tClk-2	tClk+2	tClk-2	tClk+2	tClk-2	tClk + 2	ns
tsysl	SysClk	Clock Low Time	tClk-2	tClk+2	tClk-2	tClk+2	tClk-2	tClk+ 2	ns
tsys	SysClk	System Clock Period	2^n+Clk	tClk+2	tClk-2	tClk+2	tClk-2	tClk+ 2	ns

Note: For timing diagrams of the ClkIn,. Reset, and SysClk signals, see Figure 3 through Figure 6 on the following page.

Timing Diagrams for ClkIn, Reset, and SysClk Signals — R36100

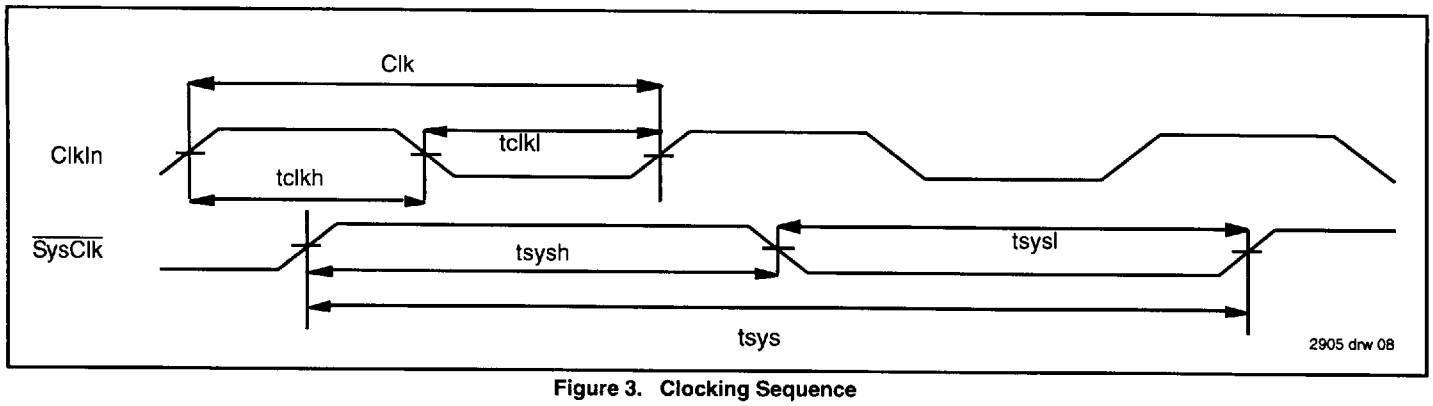


Figure 3. Clocking Sequence

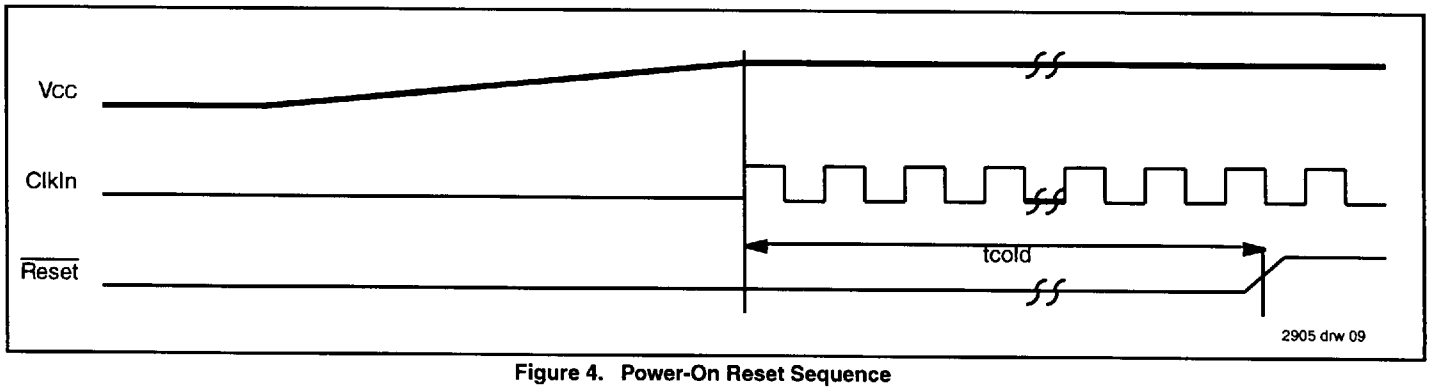


Figure 4. Power-On Reset Sequence

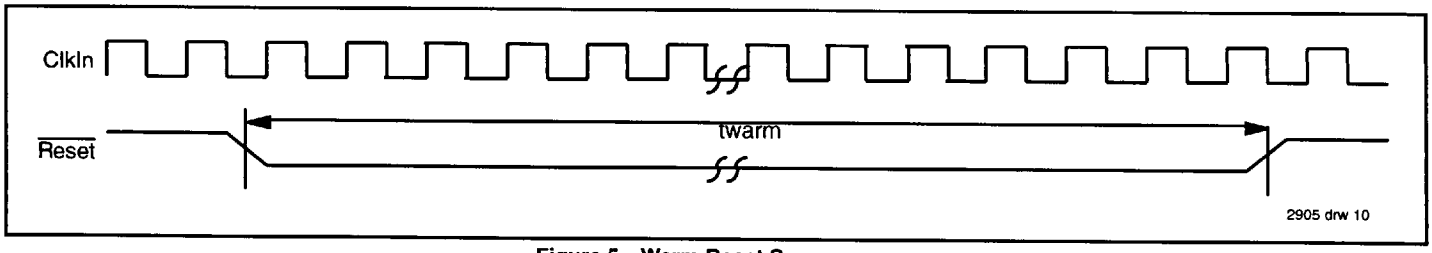


Figure 5. Warm Reset Sequence

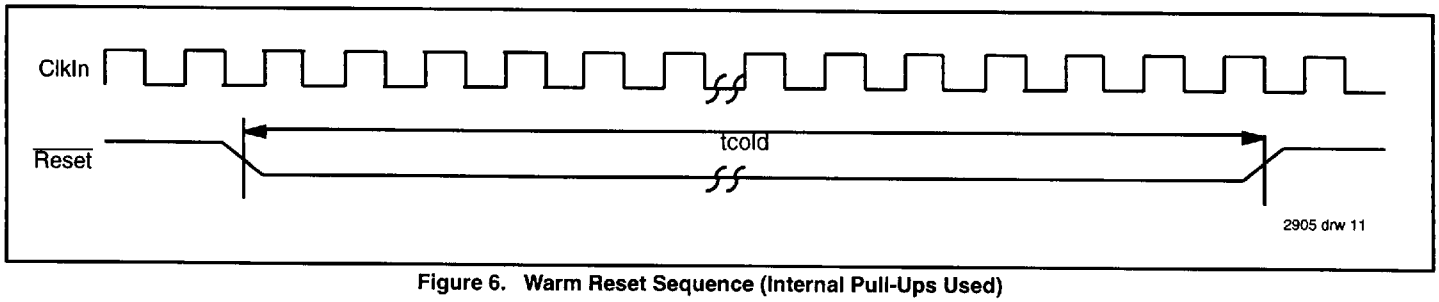


Figure 6. Warm Reset Sequence (Internal Pull-Ups Used)

DC ELECTRICAL CHARACTERISTICS — R36100

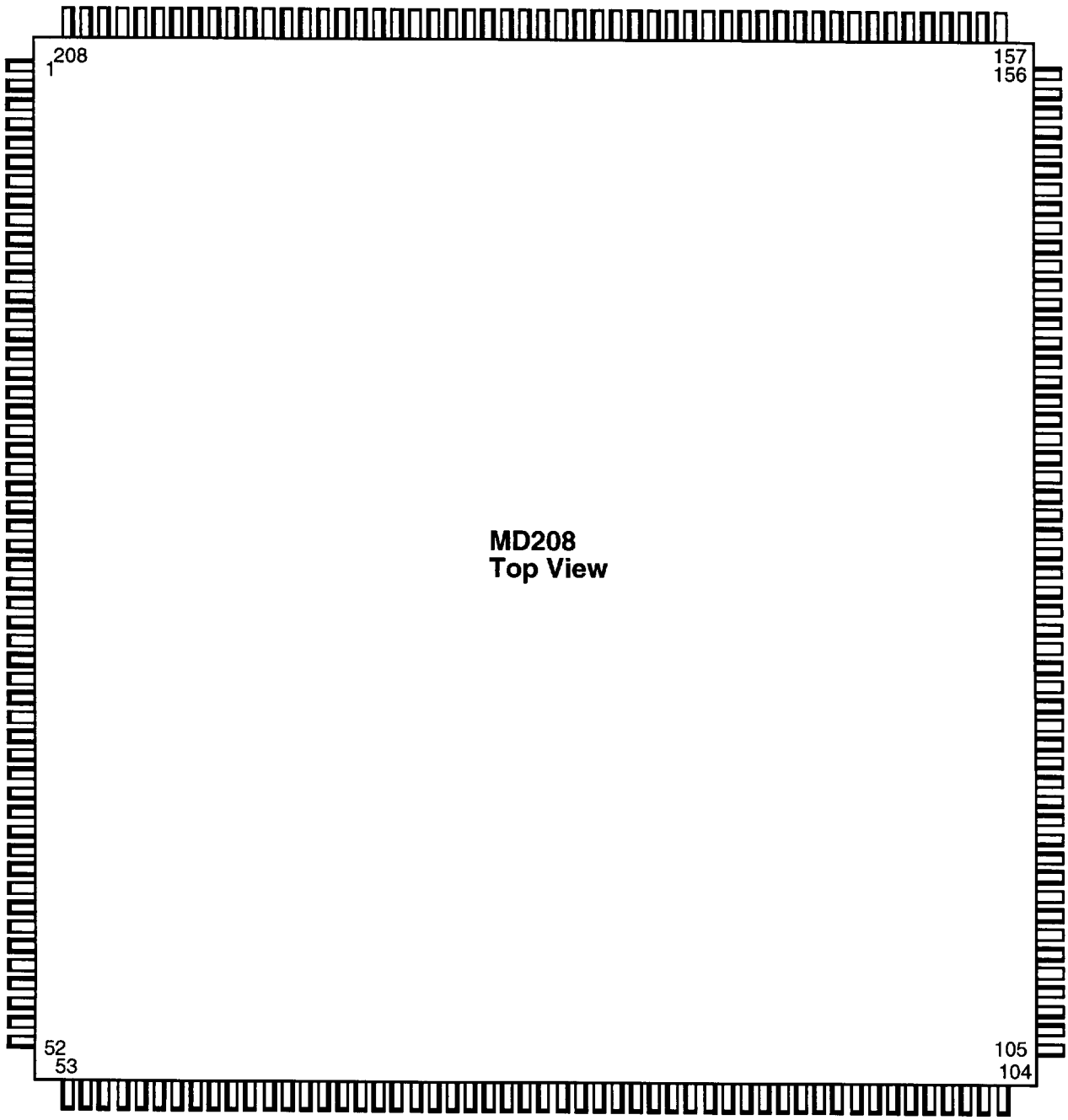
(Tc=0°C to +85°C, Vcc = +5.0V±5%)

Symbol	Parameter	Test Conditions	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{cc} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{cc} = 5V, TC = 25°C	—	400	—	500	—	600	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-100	—	-100	—	-100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-100	100	-100	100	-100	100	µA

(Tc=0°C to +85°C, Vcc = +3.3V±5%)

Symbol	Parameter	Test Conditions	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{cc} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	2.8	—	2.8	—	2.8	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{cc} =3.3V, TC = 25°C	—	210	—	270	—	360	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-100	—	-100	—	-100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-100	100	-100	100	-100	100	µA

PHYSICAL SPECIFICATIONS — MQUAD R36100



MD208
Top View

PACKAGE PIN-OUT — R36100

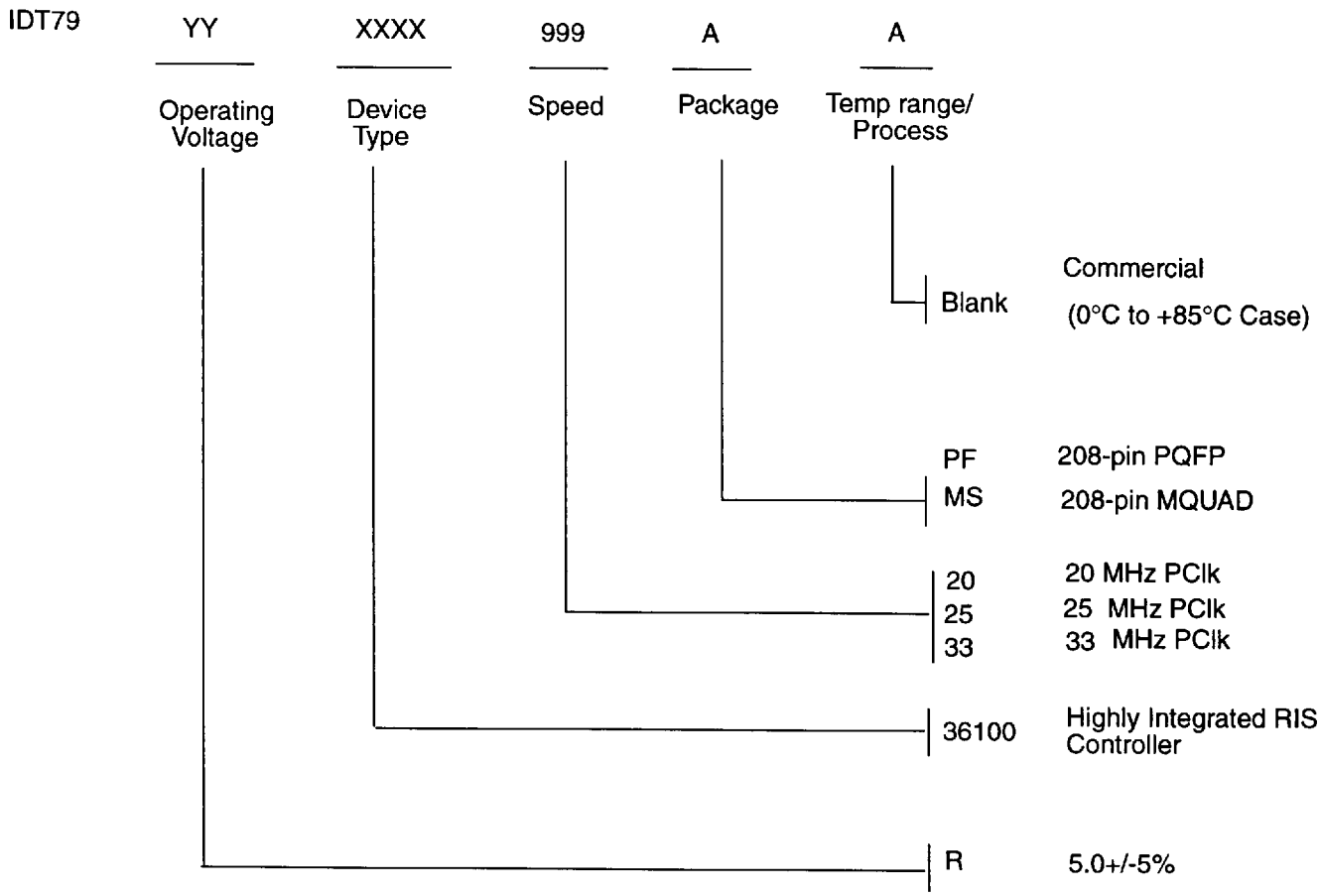
Last in Chain

Pin	Function		Pin	Function		Pin	Function		Pin	Function	
1	↑N/C	38	53	JtagDataOut		105	N/C	122	157	SerialTxData(0)	80
2	SysAddr(0)	37	54	SysData(0)	163	106	DramRAS*(2)	121	158	SerialCTS*(0)	79
3	SysAddr(1)	36	55	SysData(1)	162	107	DramRAS*(3)	120	159	SerialRTS*(0)	78
4	DiagC_UnC*	35	56	SysData(2)	161	108	DramCAS*(0)	119	160	SerialSClk*(0)	77
5	SysAddr(2)	34	57	SysData(3)	160	109	DramCAS*(1)	118	161	SerialSycn*(0)	76
6	Vcc		58	Vcc		110	Vcc		162	Vcc	
7	Vss		59	Vss		111	Vss		163	Vss	
8	SysAddr(3)	33	60	SysData(4)	159	112	DramCAS*(2)	117	164	SerialDTR*(0)	75
9	SysAddr(4)	32	61	SysData(5)	158	113	DramCAS*(3)	116	165	SerialDCD*(0)	74
10	DiagRun*	31	62	SysData(6)	157	114	DramRdEnEven*	115	166	SerialPClkIn*(1)	73
11	DiagBranchTaken*	30	63	SysData(7)	156	115	DramRdEnOdd_Tr*	114	167	SerialSClk*(1)	72
12	DiagJRorExe*	29	64	SysData(8)	155	116	MemCS*_IoCS*(0)	113	168	SerialSync*(1)	71
13	DiagInternalWr*	28	65	SysData(9)	154	117	MemCS*_IoCS*(1)	112	169	SerialRxData(1)	70
14	SysAddr(5)	27	66	SysData(10)	153	118	MemCS*_IoCS*(2)	111	170	SerialTxData(1)	69
15	SysAddr(6)	26	67	SysData(11)	152	119	MemCS*_IoCS*(3)	110	171	SerialCTS*(1)	68
16	Vcc		68	Vcc		120	Vcc		172	Vcc	
17	Vss		69	Vss		121	Vss		173	Vss	
18	SysAddr(7)	25	70	SysData(12)	151	122	MemCS*_IoCS*(4)	109	174	SerialRTS*(1)	67
19	SysAddr(8)	24	71	SysData(13)	150	123	MemCS*_IoCS*(5)	108	175	SerialDCD*(1)	66
20	↑DiagInstCacheWrDis*	23	72	SysData(14)	149	124	MemCS*_IoCS*(6)	107	176	SerialDTR*(1)	65
21	↑DiagTriState*	22	73	SysData(15)	148	125	MemCS*_IoCS*(7)	106	177	TimerTC*(0)	64
22	↑DiagFCM*	21	74	SysData(16)	147	126	MemRdEnEven*	105	178	TimerTC*(1)	63
23	↑DiagIntDis*	20	75	SysData(17)	146	127	MemRdEnOdd*	104	179	TimerTC*(2)	62
24	SysAddr(9)	19	76	SysData(18)	145	128	MemWrEn*(0)	103	180	CentStrobe*	61
25	SysAddr(10)	18	77	SysData(19)	144	129	MemWrEn*(1)	102	181	CentAck*	60
26	Vcc		78	Vcc		130	Vcc		182	Vcc	
27	Vss		79	Vss		131	Vss		183	Vss	
28	SysAddr(11)	17	80	SysData(20)	143	132	MemWrEn*(2)	101	184	CentBusy	59
29	SysAddr(12)	16	81	SysData(21)	142	133	MemWrEn*(3)	100	185	CentPaperError	58
30	DiagNoCS*	15	82	SysData(22)	141	134	IoRdEn*_DStrobe*	99	186	CentSelect	57
31	Diaginst_Data*	14	83	SysData(23)	140	135	IoWrEn*_RdWr*	98	187	CentAutoFeed*	56
32	SysAddr(13)	13	84	SysData(24)	139	136	N/C	97	188	CentInit*	55
33	SysAddr(14)	12	85	SysData(25)	138	137	N/C	96	189	CentFault*	54
34	SysAddr(15)	11	86	SysData(26)	137	138	LaserVideoData	95	190	CentSelectIn*	53
35	SysAddr(16)	10	87	SysData(27)	136	139	LaserVideoClkIn	94	191	CentHostStrobe	52
36	Vcc		88	Vcc		140	Vcc		192	Vcc	
37	Vss		89	Vss		141	Vss		193	Vss	
38	SysAddr(17)	9	90	SysData(28)	135	142	LaserLineSync*	93	194	CentHostOEn*	51
39	SysAddr(18)	8	91	SysData(29)	134	143	LaserPageSync*	92	195	DmaBusGnt*(0)	50
40	SysAddr(19)	7	92	SysData(30)	133	144	ExcSint*(0)	91	196	DmaBusGnt*(1)	49
41	SysAddr(20)	6	93	SysData(31)	132	145	ExcSint*(1)	90	197	DmaBusReq*(0)	48
42	SysAddr(21)	5	94	SysClkIn	131	146	ExcSint*(2)	89	198	DmaBusReq*(1)	47
43	SysAddr(22)	4	95	SysReset*	130	147	ExcInt*(3)	88	199	DmaDone*	46
44	SysAddr(23)	3	96	DramWrEnEven*	129	148	ExcInt*(4)	87	200	SysAlEn*	45
45	SysAddr(24)	2	97	N/C	128	149	DiagIntDma*	86	201	SysDataRdy*	44
46	Vcc		98	Vcc		150	Vcc		202	Vcc	
47	Vss		99	Vss		151	Vss		203	Vss	
48	SysAddr(25)	1	100	DramWrEnOdd*	127	152	SysWait*	85	204	SysRd*	43
49	↑JtagModeSelect		101	N/C	126	153	SysBusError*	84	205	SysWr*	42
50	↑JtagReset*		102	DramRAS*(0)	125	154	SysClk*	83	206	SysBurstFrame*	41
51	↑JtagClkIn		103	DramRAS*(1)	124	155	SerialPClkIn*(0)	82	207	ExcSBrCond(2)	40
52	↑JtagDataIn		104	↑N/C	123	156	SerialRxData(0)	81	208	ExcSBrCond(3)	39

First In Chain

↑ = Internal Pull Up

ORDERING INFORMATION



VALID COMBINATIONS

IDT79R36100 - 20, 25MHz PQFP package - PF
IDT79R36100 - 20, 25, 33MHZ MQUAD package - MS

Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (408) 727-6116 FAX 408-492-8674

PHYSICAL SPECIFICATIONS - 208-PIN PQFP