Integrated Device Technology, Inc.

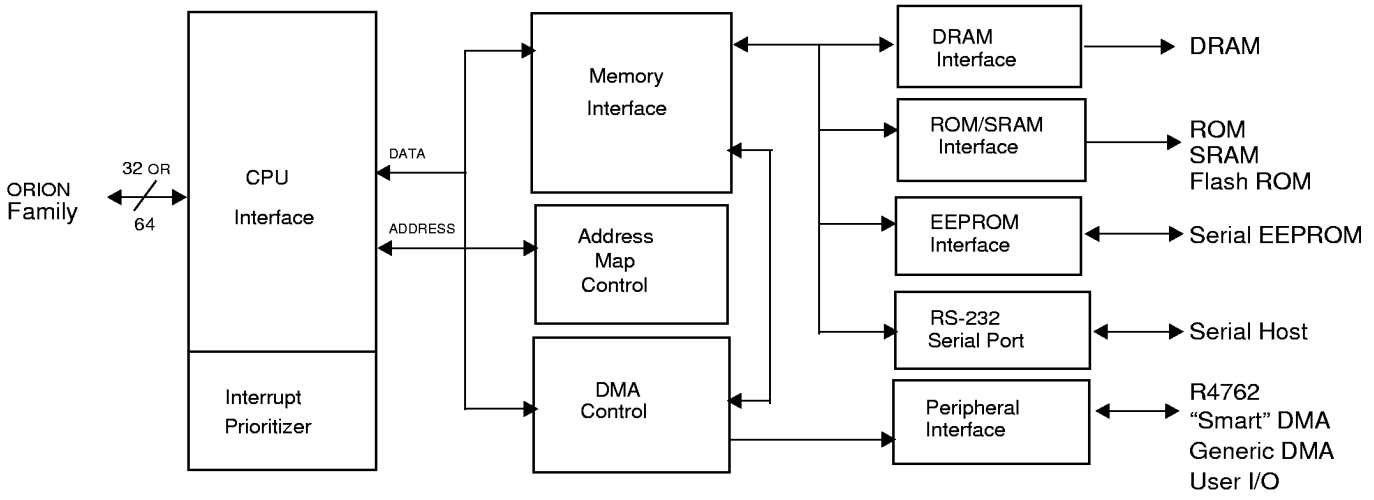
R4761 ORION FAMILY SYSTEM CONTROLLER

IDT79R4761™
Advance Information

FEATURES

- Direct interface to IDT ORION R4640/R4650/R4700/R5000 RISC microprocessors
  - 64-bit interface support for R4650/R4700/R5000
  - 32-bit interface support for R4640/4650
- Available at 5V and 3.3V
- 50 MHz bus frequency
- 1 GB address space
- Flexible DRAM interface
  - Direct interface to 512 MB
  - Available two-way interleaving
  - Transparent refresh
  - Supports 16 MBDRAMs
  - Individually programmable timing parameters,bank sizes
- RS-232 serial port (16450 UART compatible)
- Flexible ROM/SRAM interface
  - Direct interface to 64 MB
  - Available two-way interleaving
  - Each bank can be ROM, SRAM, or Flash ROM
  - Individually programmable timing parameters and bank sizes
- Serial EEPROM interface
  - Reads 256 configuration bits at power-on
  - Reads both 8- and 16-bit random values
- Peripheral interface
  - Four ports total
  - Three ports configurable as DMA
  - "Smart" DMA support
  - External intelligent agent (such as R4762)
  - interface support
  - Single and demand DMA protocol
  - Two "queued" DMA channels
  - Programmable timing parameters
- Memory-to-memory DMA channel
- Interrupt controller/prioritizer
  - Eight interrupt levels
  - Fixed or rotating prioritization
- Packaged in 208-pin PQFP

BLOCK DIAGRAM



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DESCRIPTION

The IDT79R4761 is a high-performance memory and peripheral controller designed to work with the IDT ORION R4700/R4640/R4650/R5000 RISC microprocessors. On-chip functions include an ORION-family interface, an R4762 (PCI bridge) interface, a serial EEPROM controller, a DRAM controller, a ROM/SRAM controller, a peripheral interface with DMA capability, an interrupt controller/prioritizer, and a serial interface (UART).

Functional Overview

CPU Interface

The CPU interface connects directly to the ORION R4640, R4650, R4700, and R5000 microprocessors and supports the R4650's 32-bit bus mode. "R4000-compatible write" and "write re-issue" modes are also supported. The R4761 manages all bus arbitration functions for the system, including those involving the R4762 PCI bridge device. Boot-mode initialization from the EEPROM is handled by the R4761—in conjunction with an external low-cost PAL—and can be expanded for future CPU versions. The interrupt prioritizer provides a single interrupt to the CPU.

R4762 Interface

The R4762 interface directly connects to the R4762 PCI bridge device. CPU access of R4762/PCI address space and R4762 access of system DRAM are supported. R4762 DMA transfers to DRAM, through 64 bytes, are also supported.

Serial EEPROM Interface

The serial EEPROM interface reads the 256-bit initialization stream from a standard 2K serial EEPROM at system power-on and cold resets. An external PAL assists in the sequence, allowing the R4761 to buffer only the first 16 bits. Once initialization is complete, the CPU can read either 8- or 16-bit values from the EEPROM.

Memory Controllers

The R4761's memory controllers are flexible and efficient. The DRAM controller directly interfaces to four non-interleaved banks or two interleaved banks, through a maximum of 512 MB. DRAM word depths up to 16MB are supported; each bank can have a different word depth.

Programmable timing parameters control the RAS/CAS and refresh timing. Both concurrent and staggered CAS-before-RAS refresh are supported. Sustained zero wait-state transfers are possible with interleaving; non-interleaved configurations use at least one wait-state.

ROM/SRAM Controller

The ROM/SRAM controller also controls four non-interleaved banks or two interleaved banks, through a maximum of 64 MB. Word depths from 16K to 2MB are allowed. Each bank can be read-only ROM, Flash ROM, or SRAM and has its own word depth and timing parameters. Interleaved banks can be intermixed with non-interleaved banks. Interleaving allows zero wait-state sustained transfers.

Peripheral Interface

A flexible peripheral interface provides four multi-functional ports for external devices using synchronous signal protocols. All of the ports can be configured as user I/O with edge- or level-sensitive interrupt capability on inputs. Port0 can support the R4762 PCI bridge device. Three of the ports can be configured for direct-memory access (DMA), including one "smart" peripheral that can use either Intel or Motorola bus mode arbitration. An internal memory-to-memory DMA channel is also included.

DMA devices can transfer to or from DRAM or ROM/SRAM at the full memory transfer rate of one doubleword per clock cycle for interleaved configurations and can be selected for use in single- or demand-transfer mode. Two of the DMA channels have an alternate address pointer, allowing queued buffer applications. The R4761 performs DMA arbitration using fixed or rotating priority.

Serial Interface

A serial interface compatible with a 16450 UART is included. The baud rate input clock can be selectively prescaled by 16, allowing flexibility in fine-tuning the exact frequencies desired. Baud rates from 50 to 38.5K bits-per-second are possible.

Interrupt Controller

An eight-level interrupt controller is contained in the R4761. Each of the four peripheral ports, the memory-to-memory DMA channel, UART, and internal R4761 exceptions make up the eight levels. Both fixed and rotating prioritization methods are available. A single interrupt signal is provided to the CPU.

Thermal Considerations

The R4761 uses special packaging techniques to improve the thermal properties of high-speed devices. The R4761 is packaged using cavity down packaging in a 208-pin PQFP package for devices with low peak power.

The R4761 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

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The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device.

The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 1.

	$\varnothing_{CA}$					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
208 PQFP	41	30	26	23	22	21

Table 1. Thermal Resistance at Various Airflows

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Pin Information

Logic Symbol

Signal names that end with an asterisk are active when low.

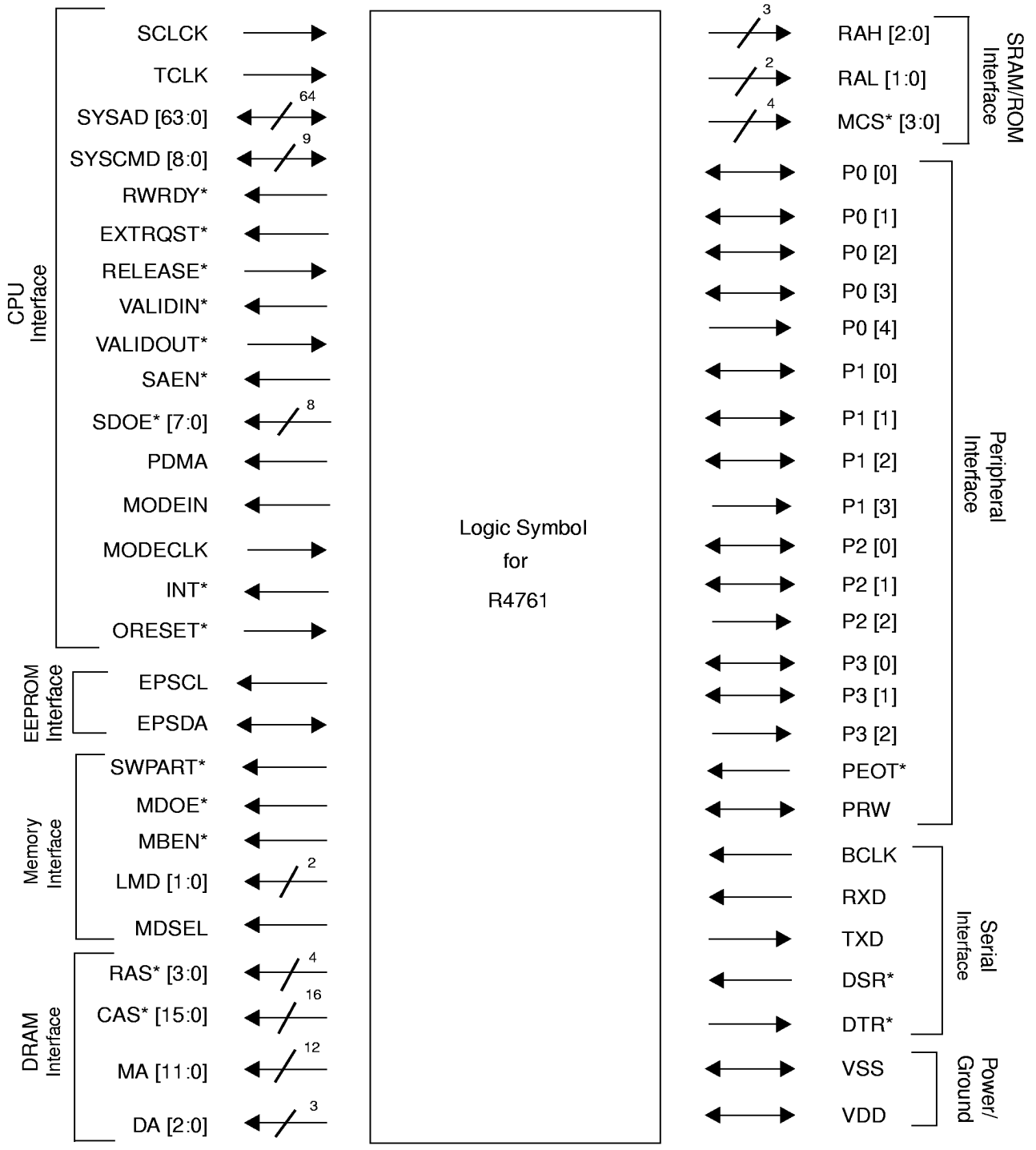

Figure 1. R4761 Logic Symbol Diagram

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PIN DESCRIPTIONS

The following is a list of pins available on the R4761. Pin names ending with an asterisk are active when low.

Pin Name	Type	Description
Processor Interface		
SCLK	I	Initialization Clock, from the crystal, always valid (not ORION's SCLK).
TCLK	I	Functional clock (ORION TCLK), valid after initialization.
SYSAD [63:0]	I/O	System address/data bus.
SYSCMD [8:0]	I/O	System command bus.
RWRDY*	O	Active Low. Combined CPU RDRDY* and WRRDY*.
EXTRQST*	O	Active Low. CPU external request.
RELEASE*	I	Active Low. CPU bus release.
VALIDIN*	O	Active Low. CPU valid data in.
VALIDOUT*	I	Active Low. CPU valid data out.
SAEN*	O	Active Low. External address register
SDOE* [7:0]	O	Active Low. External data register output enable, 1 per byte.
PDMA	O	Peripheral DMA override for SDOE*. Control of '241 buffer.
SWPART*	O	Active Low. SRAM write. Partial override for SDOE*. Control of '241 buffer.
MODEIN	O	CPU MODEIN. Input for serial init data.
MODECLK	I	CPU MODECLOCK. Output to sync serial init data.
INT*	O	Active Low. Interrupt Out. Connected to any of the CPU interrupt inputs.
ORESET*	I	Active Low. R4761 chip-wide reset. This is not the CPU RESET* signal.
Memory Interface		
EPSCL	O	EEPROM serial clock.
EPSDA	I/O	EEPROM serial data.
MDOE*	O	Active Low. Memory data output enable.
MBEN*	O	Active Low. Memory bus enable.
LMD [1:0]	O	Memory write data latch. Enable for odd and even banks/leaves.
MDSEL	O	Memory read data select between odd and even banks/leaves.
RAS* [3:0]	O	Active Low. Row address strobe for 4 DRAM banks/leaves.
CAS* [15:0]	O	Active Low. Column address strobe for each byte of 64-bit words maximum.
MA [11:3]	I/O	DRAM address up to 16M word depth using x4's, x8's, etc.
MA [2:0]	O	DRAM address up to 16M word depth using x4's, x8's, etc.
DA [2:0]	O	Interleaved DRAM leaf 1 lower address bits.
RAH [2:0]	O	ROM/SRAM leaf 1 or MS low address bits.
RAL [1:0]	O	ROM/SRAM leaf 0 or LS low address bits.
MCS* [3:0]	O	Active Low. Memory chip select for 4 ROM/SRAM banks/leaves.
Peripheral Interface		
P0 [0]	I/O	R4762 BUSREQ* in/P0 User I/O.
P0 [1]	I/O	R4762 VALIDIN2* out / P1 RDY*/ DSACK* out / P0 User I/O.
P0 [2]	I/O	R4762 VALIDOUT2* in P1 ADS*/AS* in P0 User I/O.
P0 [3]	I/O	R4762 BUSY* Input/ P0 User I/O.
P0 [4]	O	R4762 BUSACK* Output / P0 CS.
P1 [0]	I/O	P1 HOLD/BREQ* In / User I/O.

Table 2. R4761 Pin Descriptions (Page 1 of 2)

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Pin Name	Type	Description
P1 [1]	I/O	P1 HLDA/BGNT* Out / User I/O.
P1 [2]	I/O	P1 BGACK* In / User I/O.
P1 [3]	O	P1 CS
P2 [0]	I/O	P2 DREQ Input / User I/O.
P2 [1]	I/O	P2 DACK Output / User I/O.
P2 [2]	O	P2 CS
P3 [0]	I/O	P3 DREQ Input / User I/O.
P3 [1]	I/O	P3 DACK Output / User I/O.
P3 [2]	O	P3 CS
PEOT*	I	Active Low. Peripheral ports 1-3 common EOT* signal.
PRW	I/O	Peripheral ports 0-3 common R/W output signal. Input for P1operations.
Serial Interface		
BCLK	I	Serial interface baud clock input.
RXD	I	Serial interface receive data input.
TXD	O	Serial interface transmit data output.
DSR*	I	Active Low. Serial interface data set ready input.
DTR*	O	Active Low. Serial interface data terminal ready output.
Power and Ground		
VSS		Ground
VDD		Power (+5V)

Table 2. R4761 Pin Descriptions (Page 2 of 2)

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AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4761

(V_{CC}=5.0V ± 5%; T_{CASE} = 0°C to +85°C)

Capacitive load for all output timings is 50pF. Timings are measured from 1.5V of the clock to 1.5V of the signal.

System Interface Parameters—R4761

Signal	Type	Reference Clock Edge	R4761 50 MHz				Units
			Min	Max	Data Setup	Data Hold	
SYSAD[63:0]	Input/Output	TClock rising	N/A	7.5	3.5	1.5	ns
SYSCMD[8:0]	Input/Output	TClock rising	N/A	7.5	3.5	1.5	ns
VALIDIN*	Output	TClock rising	N/A	7.5	—	—	ns
SDOE*[7:0]	Output	TClock rising	N/A	6.5	—	—	ns
SAEN*	Output	TClock rising	N/A	7.5	—	—	ns
RWRDY*	Output	TClock rising	N/A	6.5	—	—	ns
EXTRQST*	Output	TClock rising	N/A	6.5	—	—	ns
MBEN*	Output	TClock rising	N/A	9.5	—	—	ns
LMD[1:0]	Output	TClock rising	N/A	6.5	—	—	ns
RAS*[3:0]	Output	TClock rising	N/A	6.0	—	—	ns
CAS*[15:0]	Output	TClock falling	N/A	6.5	—	—	ns
MA[11:0]	Output	TClock rising	N/A	9.5	—	—	ns
DA[2:0]	Output	TClock rising	N/A	9.0	—	—	ns
RAH[2:0]	Output	TClock rising	N/A	7.5	—	—	ns
RAL[1:0]	Output	TClock rising	N/A	7.0	—	—	ns
MCS*[3:0]	Output	TClock rising	N/A	8.5	—	—	ns

Capacitive Load Deration

Parameter	Symbol	R4761 50MHz		Units
		Min	Max	
Load Derate	C_{LD}	—	2	ns/25pF

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DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE R4761

(V_{cc} = 5.0±5%, T_{CASE} = 0°C to +85°C)

Parameter	R4761 50MHz		Conditions
	Minimum	Maximum	
V_{OL}	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	—
V_{IH}	2.0V	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	10pF	—
C_{OUT}	—	10pF	—
I/O_{LEAK}	—	20uA	Input/Output Leakage
I_{cc}	—	300 mA	Vcc = Vcc max; Tc = 25°C

Notes:
1. V_{IH} should not be held above Vcc + 0.5 volts.
2., Guaranteed by design.

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PACKAGE PIN-OUT

The following is a list of pins available on the R4761. Pin names ending with an asterisk are active when low.

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	VDD	43	VDD	85	VSS	127	CAS*[1]	169	P3[2]
2	RELEASE*	44	SYSCMD[7]	86	SWPART*	128	CAS*[0]	170	P3[1]
3	SYSAD[55]	45	SYSAD[41]	87	PDMA	129	MA[11]	171	P3[0]
4	SYSAD[23]	46	SYSAD[9]	88	MDSEL	130	VSS	172	P2[2]
5	MODECLK	47	SYSCMD[6]	89	SDOE*[7]	131	VDD	173	P2[1]
6	SYSAD[54]	48	SYSAD[40]	90	SDOE*[6]	132	MA[10]	174	P2[0]
7	SYSAD[22]	49	SYSAD[8]	91	SDOE*[5]	133	MA[9]	175	P1[3]
8	MODEIN	50	SYSCMD[5]	92	SDOE*[4]	134	MA[8]	176	VSS
9	SYSAD[53]	51	SYSCMD[4]	93	SDOE*[3]	135	MA[7]	177	VDD
10	VSS	52	SYSAD[39]	94	VSS	136	MA[6]	178	P1[2]
11	VDD	53	VSS	95	VDD	137	MA[5]	179	P1[1]
12	SYSAD[21]	54	VDD	96	SDOE*[2]	138	MA[4]	180	P1[0]
13	SYSAD[52]	55	SYSAD[7]	97	SDOE*[1]	139	VSS	181	ORESET*
14	SYSAD[20]	56	SYSCMD[3]	98	SDOE*[0]	140	VDD	182	P0[4]
15	VALIDOUT*	57	SYSAD[38]	99	MBEN*	141	MA[3]	183	P0[3]
16	SYSAD[51]	58	SYSAD[6]	100	MDOE*	142	MA[2]	184	P0[2]
17	SYSAD[19]	59	RWRDY*	101	LMD[1]	143	MA[1]	185	P0[1]
18	SYSAD[50]	60	SYSAD[37]	102	LMD[0]	144	MA[0]	186	P0[0]
19	SYSAD[18]	61	SYSAD[5]	103	VSS	145	DA[2]	187	VSS
20	VALIDIN*	62	SYSCMD[2]	104	VDD	146	DA[1]	188	VDD
21	VSS	63	SYSAD[36]	105	RAS*[3]	147	DA[0]	189	SYSAD[63]
22	VDD	64	VSS	106	RAS*[2]	148	VSS	190	SYSAD[31]
23	SYSAD[49]	65	VDD	107	RAS*[1]	149	RAH[2]	191	SYSAD[62]
24	SYSAD[17]	66	SYSAD[4]	108	RAS*[0]	150	RAH[1]	192	SYSAD[30]
25	SYSAD[48]	67	SYSCMD[1]	109	CAS*[15]	151	RAH[0]	193	SYSAD[61]
26	SYSAD[16]	68	SYSAD[35]	110	CAS*[14]	152	RAL[1]	194	SYSAD[29]
27	SYSAD[47]	69	SYSAD[3]	111	CAS*[13]	153	RAL[0]	195	SYSAD[60]
28	SYSAD[15]	70	SYSCMD[0]	112	VSS	154	MCS*[3]	196	SYSAD[28]
29	SYSAD[46]	71	SYSAD[34]	113	VDD	155	MCS*[2]	197	VSS
30	SYSAD[14]	72	SYSAD[2]	114	CAS*[12]	156	VSS	198	VDD
31	VSS	73	SYSAD[33]	115	CAS*[11]	157	VDD	199	SYSAD[59]
32	VDD	74	SYSAD[1]	116	CAS*[10]	158	MCS*[1]	200	SYSAD[27]
33	SYSAD [45]	75	VSS	117	CAS*[9]	159	MCS*[0]	201	SYSAD[58]
34	SYSAD [13]	76	VDD	118	CAS*[8]	160	BCLK	202	SYSAD[26]
35	SYSAD [44]	77	SYSAD[32]	119	CAS*[7]	161	RXD	203	SYSAD[57]
36	SYSAD [12]	78	SYSAD[0]	120	CAS*[6]	162	TXD	204	SYSAD[25]
37	SYSAD [43]	79	INT*	121	VSS	163	DSR	205	EXTRQST*
38	SYSAD [11]	80	TCLK	122	VDD	164	DTR	206	SYSAD[56]
39	SYSCMD [8]	81	EPSCL	123	CAS*[5]	165	VSS	207	SYSAD[24]
40	SYSAD [42]	82	EPSDA	124	CAS*[4]	166	VDD	208	VSS
41	SYSAD [10]	83	SCLK	125	CAS*[3]	167	PEOT*		
42	VSS	84	SAEN	126	CAS*[2]	168	PRW		

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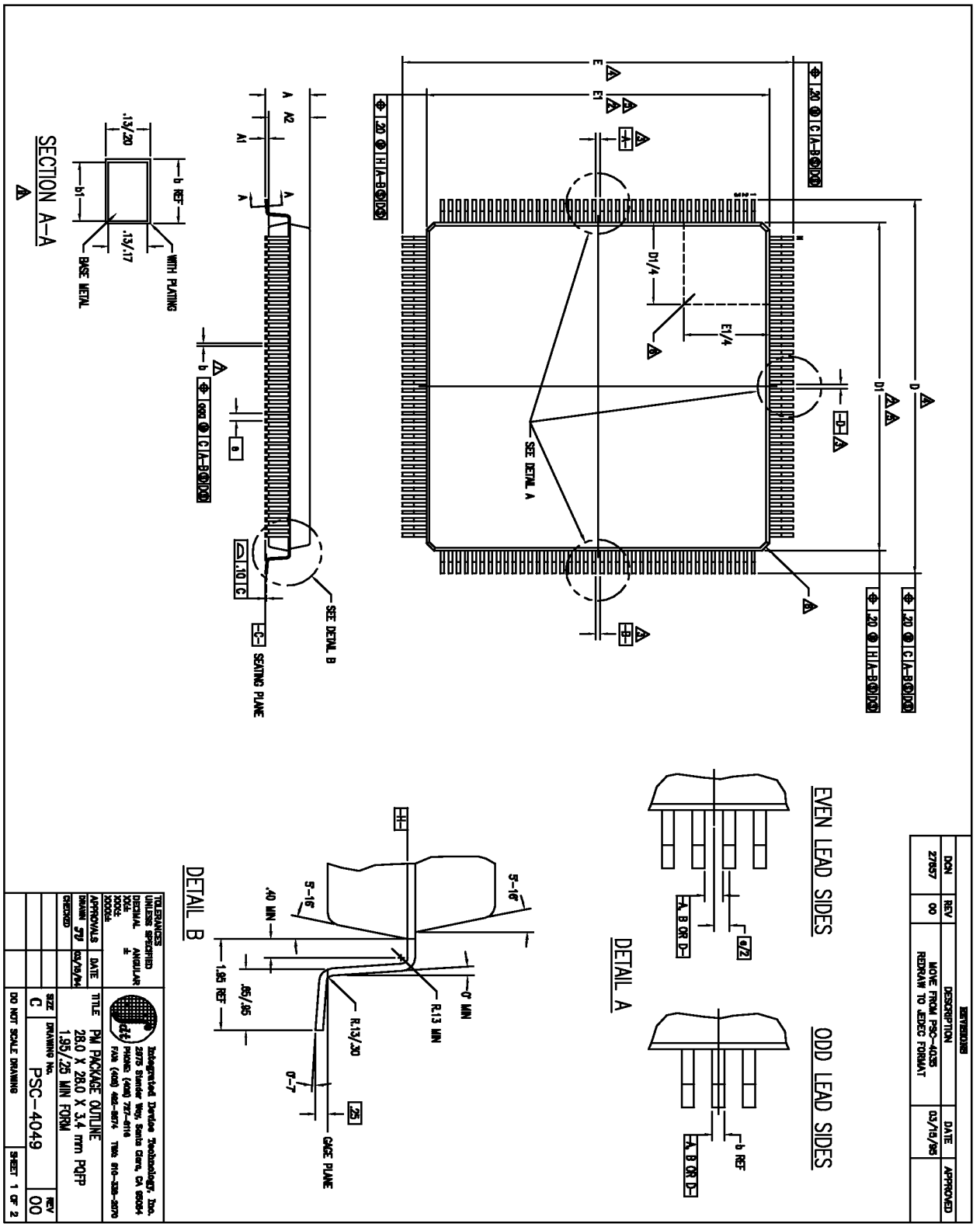
PHYSICAL SPECIFICATIONS - 208-PIN PQFP



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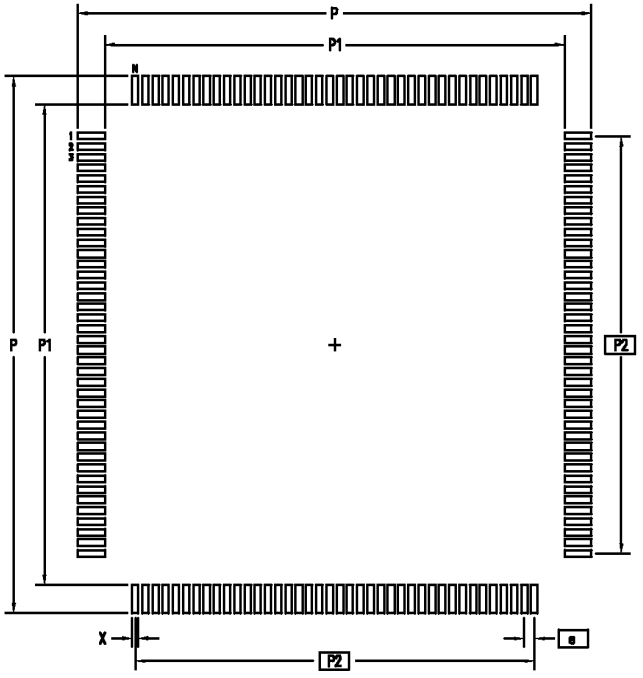
PQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27857	00	MOVE FROM PSC-4035 REDRAW TO JEDEC FORMAT	03/15/95	

	DWG #		PQ144-2		DWG #		PQ160-2		DWG #		PQ208-2	
SYMBOL	JEDEC VARIATION DC-1			NOTE	JEDEC VARIATION DD-1			NOTE	JEDEC VARIATION -			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	3.45	–	4.07		3.45	–	4.07		3.45	–	4.07	
A1	.25	–	–		.25	–	–		.25	–	–	
A2	3.18	3.42	3.65		3.18	3.42	3.65		3.18	3.42	3.65	
D	31.80	31.90	32.00	4	31.80	31.90	32.00	4	31.80	31.90	32.00	4
D1	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2
E	31.80	31.90	32.00	4	31.80	31.90	32.00	4	31.80	31.90	32.00	4
E1	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2
N	144				160				208			
e	.65 BSC				.65 BSC				.50 BSC			
b	.22	–	.35	7	.22	–	.35	7	.17	–	.27	7
b1	.22	.30	.32		.22	.30	.32		.17	.20	.23	
aaa	–	–	.12		–	–	.12		–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	32.50	32.70	32.50	32.70	32.50	32.70
P1	28.40	28.60	28.40	28.60	28.40	28.60
P2	22.75 BSC		25.35 BSC		25.50 BSC	
X	.30	.50	.30	.50	.30	.40
e	.65 BSC		.65 BSC		.50 BSC	
N	144		160		208	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THE 144 & 160 LD OUTLINES CONFORM TO JEDEC PUBLICATION 95 REGISTRATION MO-112, VARIATION DC-1 & DD-1 RESPECTIVELY

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PM PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.95/.25 MIN FORM	
DRAWN STP	03/15/94		
CHECKED		SIZE C	DRAWING No. PSC-4049 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

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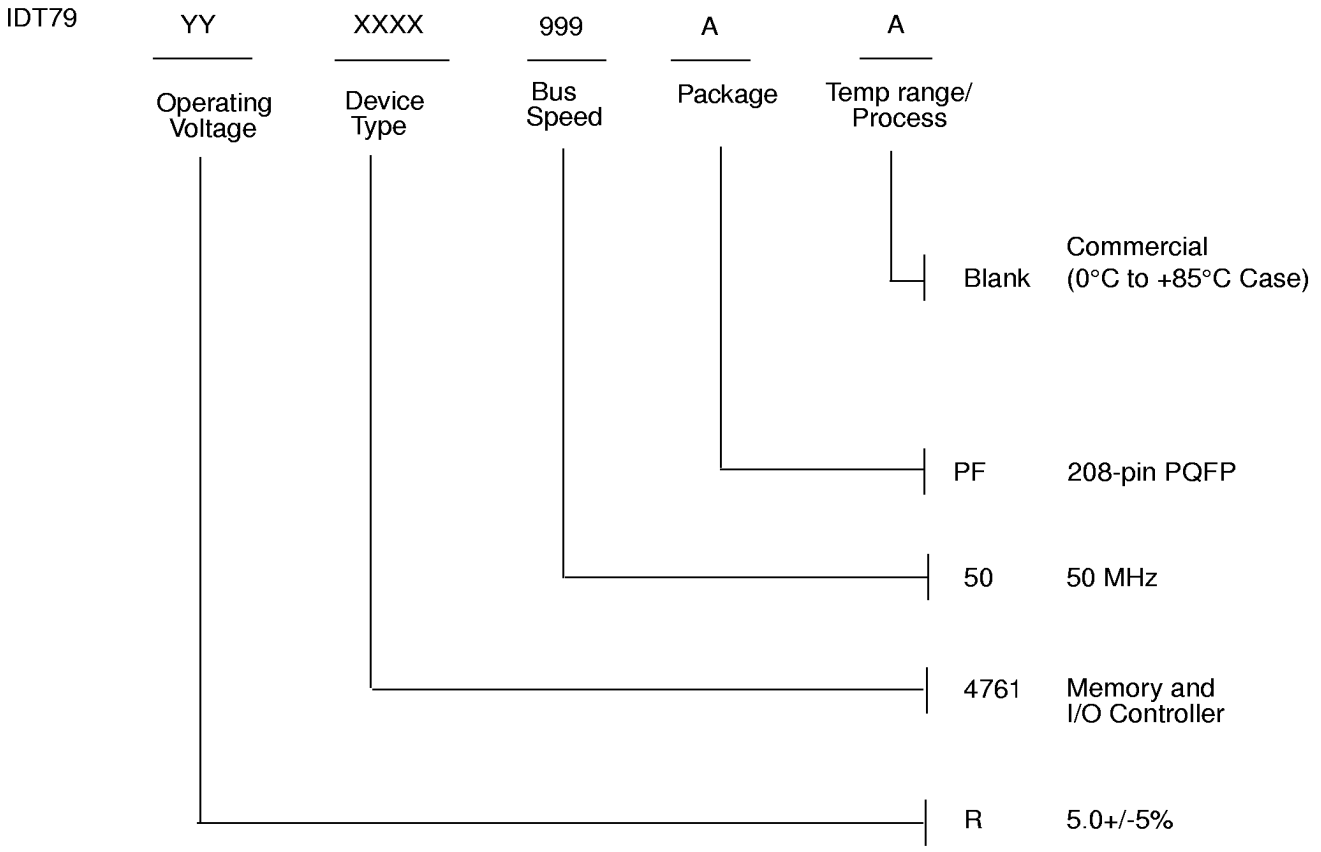
ORDERING INFORMATION



VALID COMBINATION

IDT79R4761 50 MHz PQFP package

Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

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