Lattice Semiconductor Corporation

ispGAL16Z8

In-System Programmable High Performance E²CMOS PLD

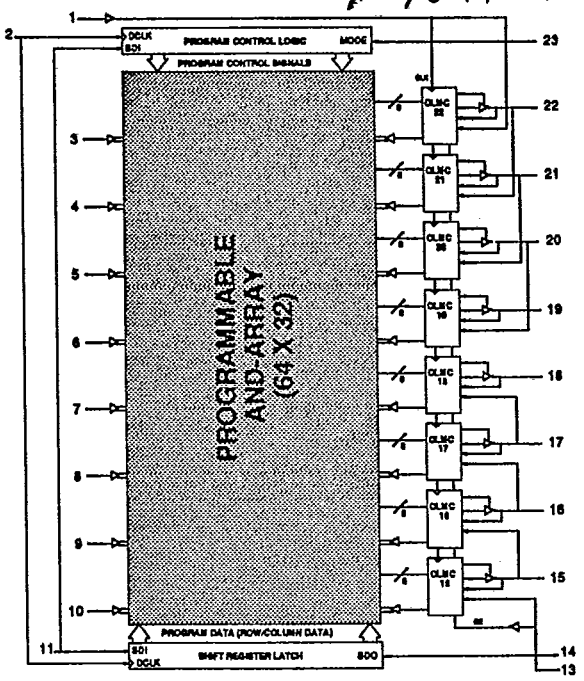
2

T-46-19-07

FEATURES

- IN-SYSTEM-PROGRAMMABLE — 5-VOLT ONLY
  - Change Logic "On The Fly" In Seconds
  - Non-volatile E² Technology
- MINIMUM 10,000 ERASE/WRITE CYCLES
- DIAGNOSTIC MODE FOR CONTROLLING AND OBSERVING SYSTEM LOGIC
- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 20 ns Maximum Propagation Delay
  - Fmax = 41.6 MHz
  - 90 mA MAX Icc
- E² CELL TECHNOLOGY
  - 100% Tested/Guaranteed 100% Yields
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - Reconfigurable Interfaces and Decoders
  - "Soft" Hardware (Generic Systems)
  - Copy Protection and Security Schemes
  - Reconfiguring Systems for Testing
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

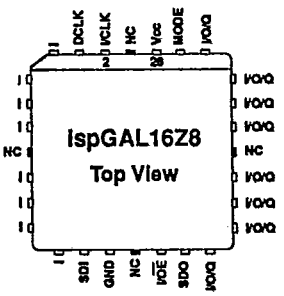
The Lattice ispGAL® 16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmability and in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage programming signals. Using Lattice's proprietary UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL16V8, but includes 4 extra pins to control in-system programming. These pins are not associated with normal logic functions and are used only during programming and diagnostic operations. This 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

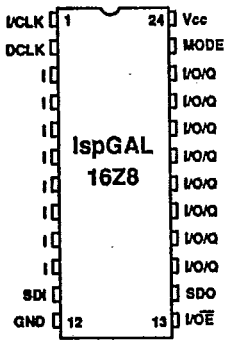
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

PIN CONFIGURATION

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.A

Lattice Semiconductor Corporation

Specifications *ispGAL16Z8*

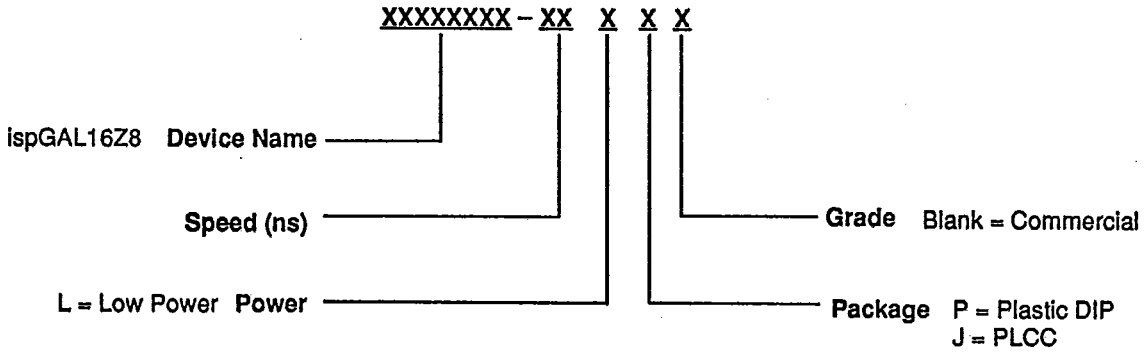
T-46-19-07

ispGAL16Z8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	15	15	90	ispGAL16Z8-20LP	24-Pin Plastic DIP
			90	ispGAL16Z8-20LJ	28-Lead PLCC
25	20	15	90	ispGAL16Z8-25LP	24-Pin Plastic DIP
			90	ispGAL16Z8-25LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



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Specifications *ispGAL16Z8*

T-46-19-07

2

OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple, complex,** and **registered.** Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells, the XOR bit of each macrocell controls the polarity of the output in any of the three modes, and the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in an ispGAL16Z8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8, and therefore the ispGAL16Z8, can emulate. It also shows the OLMC mode under which the ispGAL16Z8 emulates the PAL architecture.

PAL Architectures Emulated by ispGAL16Z8	ispGAL16Z8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

The ispGAL16Z8 can be treated as a GAL16V8, and tools are provided by Lattice to use GAL16V8 JEDEC files to program ispGAL16Z8 devices.

When using compiler software to configure the device, the user must pay special attention to the following restrictions:

In **registered mode** pin 1 and pin 13 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 18 and pin 19 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner-most pins (pins 18 and 19) will not have feedback, as these pins are always configured as dedicated combinatorial output. All macrocells are always either dedicated inputs or dedicated outputs in this mode.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8S	P16V8
CUPL	G16V8MS	G16V8MA	G16V8S	G16V8
LOG/IC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with Configuration keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Lattice Semiconductor Corporation

Specifications *ispGAL16Z8*

T-46-19-07

REGISTERED MODE

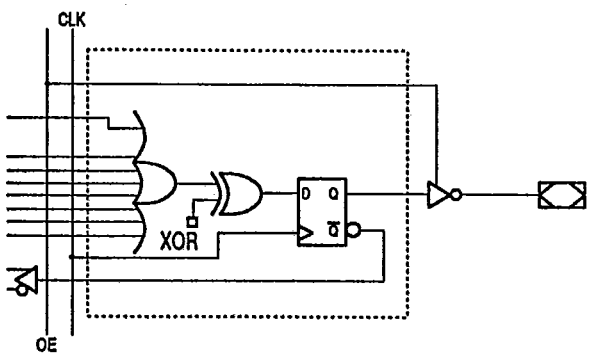
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

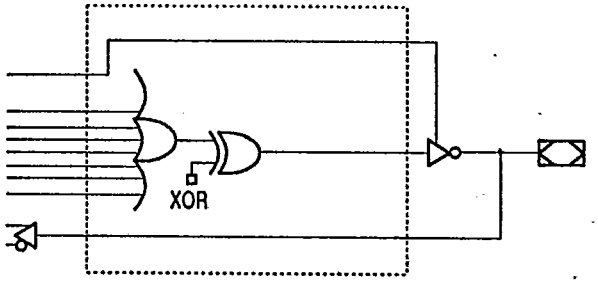
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK and $\overline{OE}$.



Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK and $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

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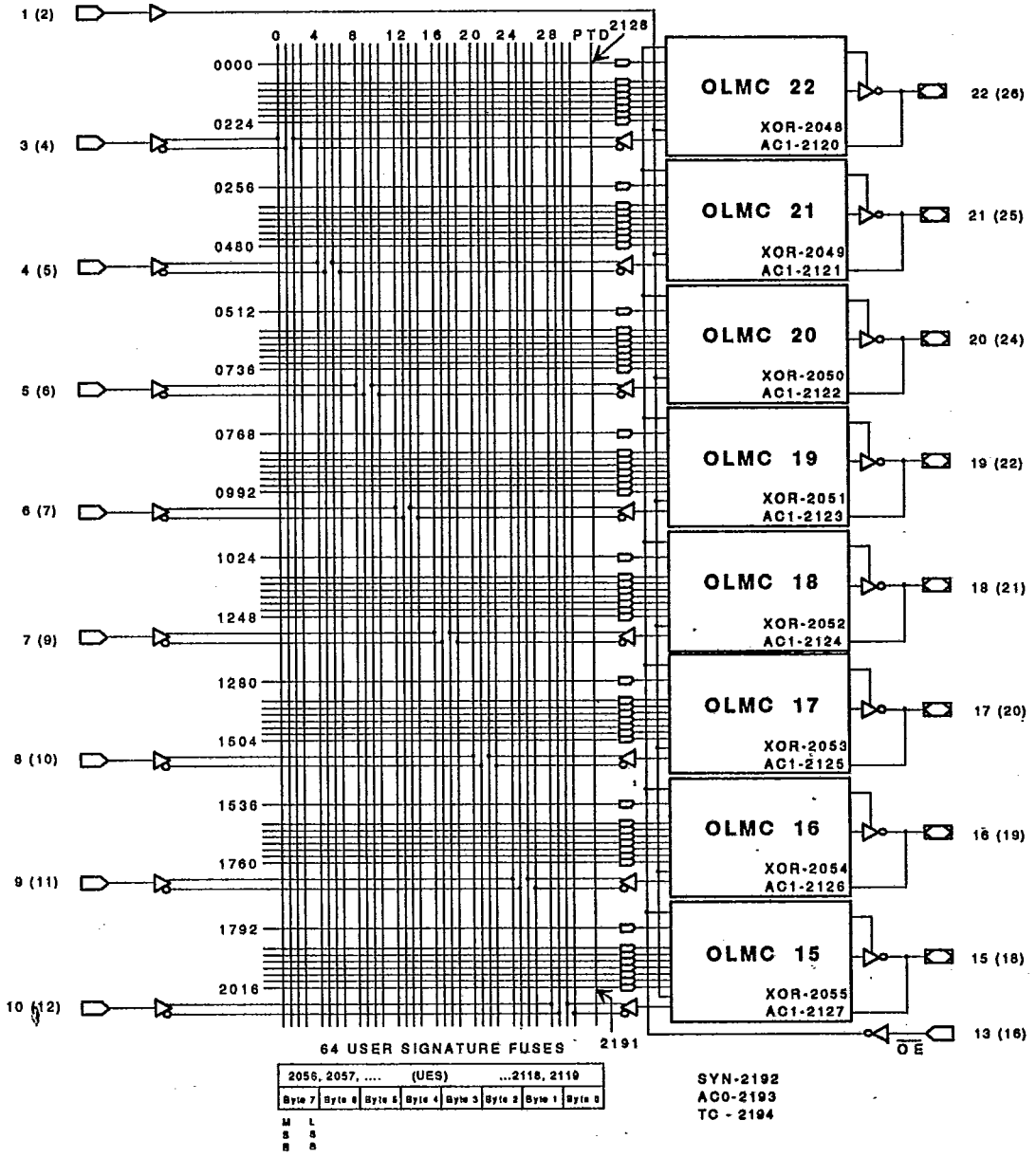
Specifications *ispGAL16Z8*

T-46-19-07

REGISTERED MODE LOGIC DIAGRAM

2

DIP (PLCC) Package Pinouts



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Specifications *ispGAL16Z8*

T-46-19-07

COMPLEX MODE

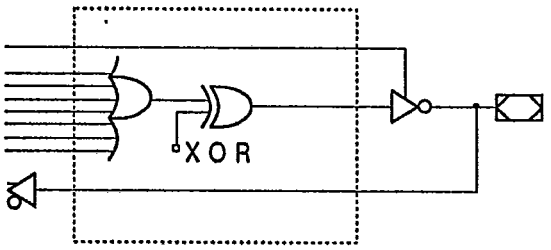
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

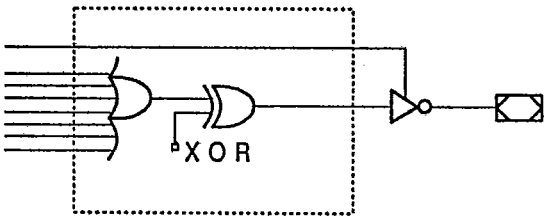
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pins 16 through Pin 21 are configured to this function.



Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pins 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

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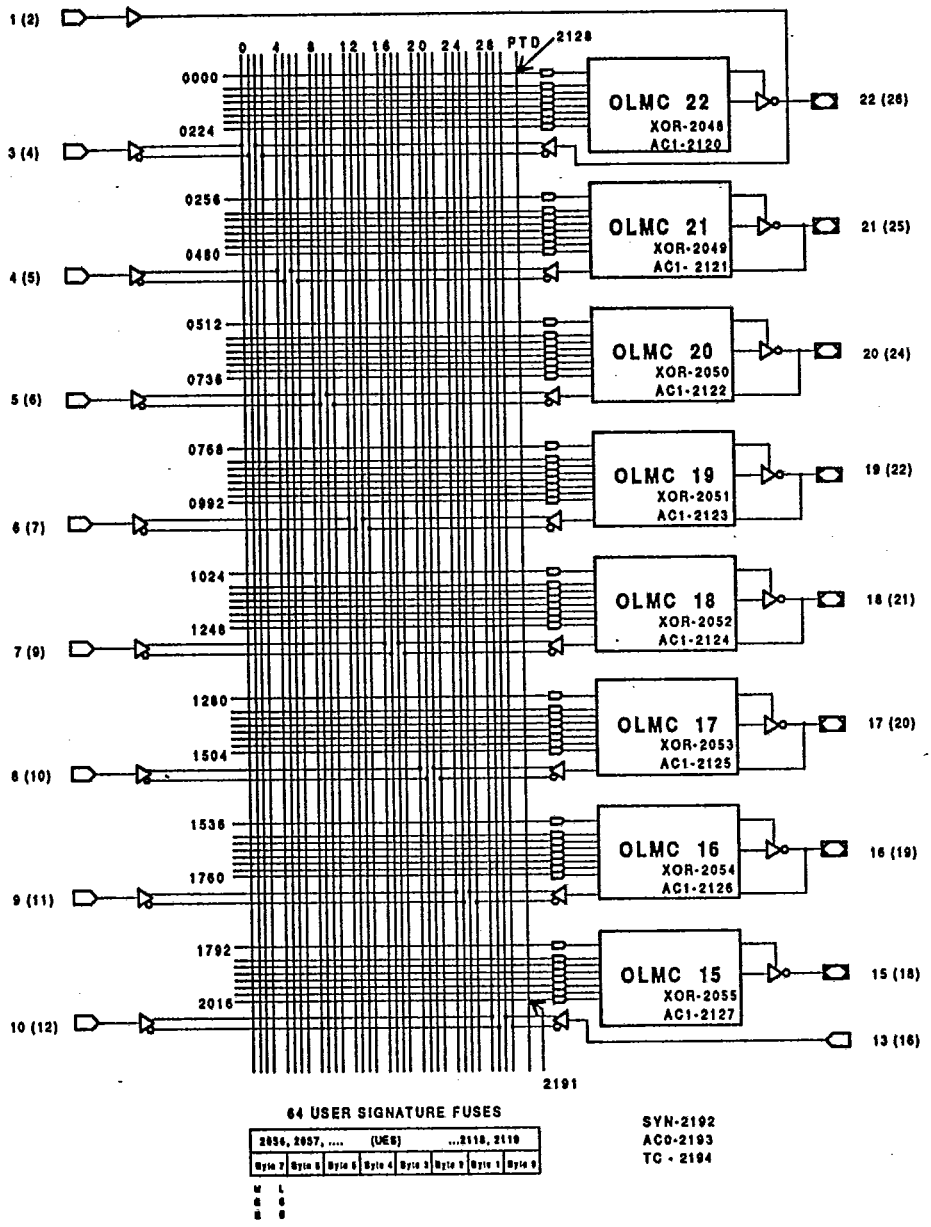
Specifications *ispGAL16Z8*

COMPLEX MODE LOGIC DIAGRAM

T-46-19-07

2

DIP (PLCC) Package Pinouts



SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

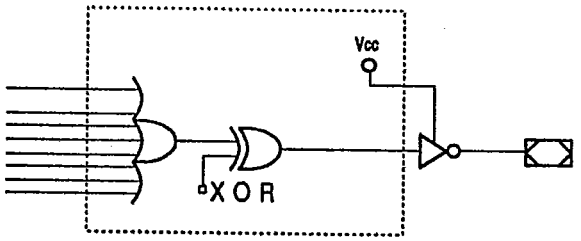
Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 13 are always available as data inputs into the AND array. The center two macrocells (pins 18 & 19) cannot be used in the input configuration.

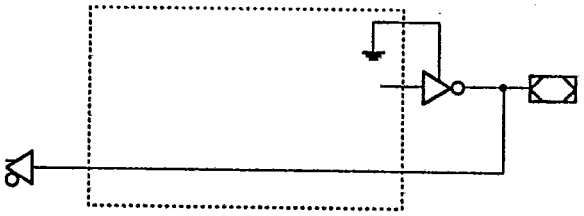
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

T-46-19-07



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMCs can be configured to this configuration.
- Pins 18 & 19 are permanently configured to this function.



Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMCs except pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

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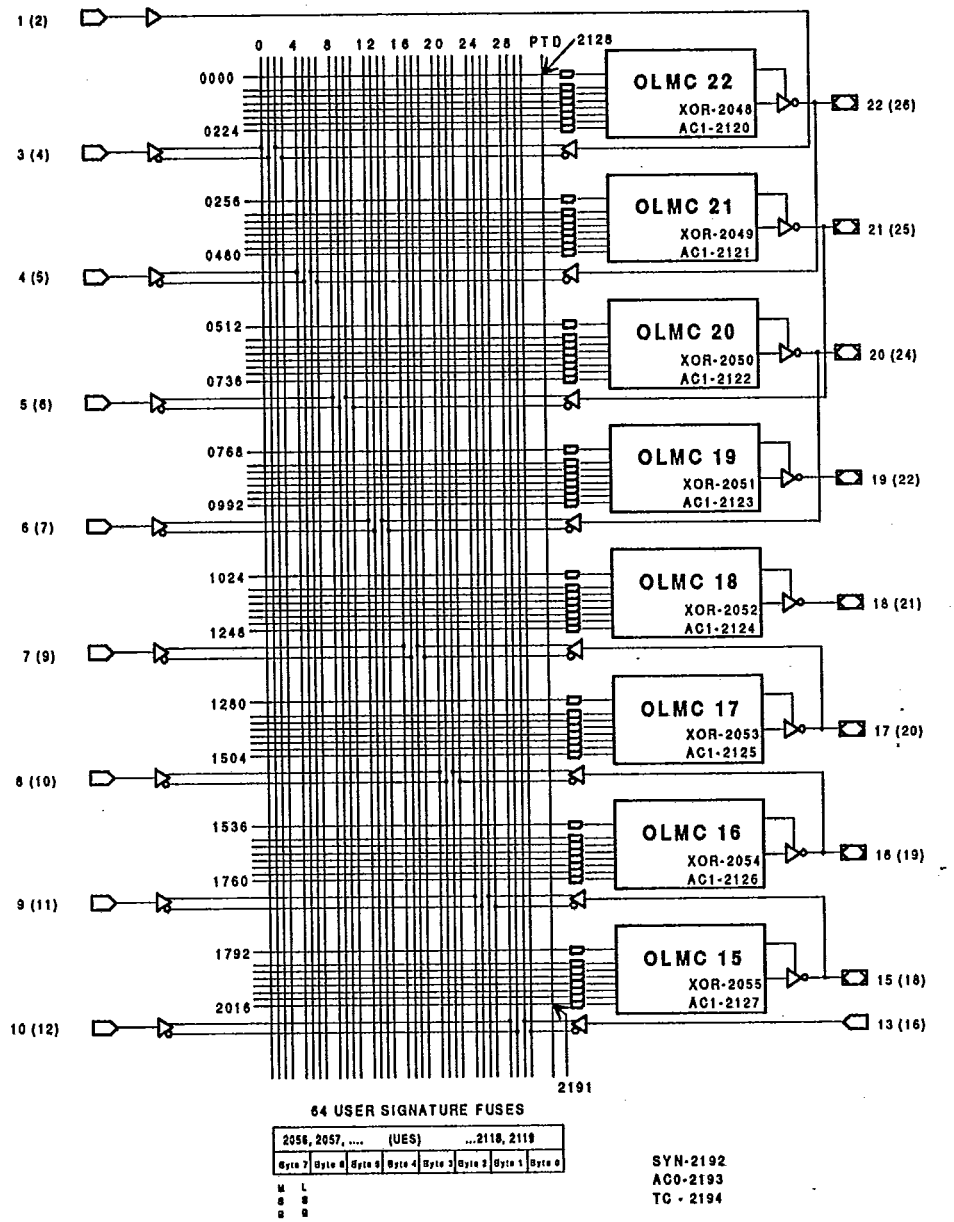
Specifications *ispGAL16Z8*

T-46-19-07

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} .....-0.5 to +7V
Input voltage applied .....-2.5 to V_{CC} +1.0V
Off-state output voltage applied .....-2.5 to V_{CC} +1.0V
Storage Temperature .....-65 to 150°C
Ambient Temperature with
Power Applied .....-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND

Ambient Temperature (T_A) .....0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	Vcc = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	75	90	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

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Specifications *ispGAL16Z8* Commercial

AC SWITCHING CHARACTERISTICS

T-46-19-07

2

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	20	3	25	ns
tco	1	Clock to Output Delay	2	15	2	15	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	15	—	20	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[2]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	33.3	—	28.5	—	MHz
	1	Maximum Clock Frequency with No Feedback	41.6	—	33.3	—	MHz
twh[3]	—	Clock Pulse Duration, High	12	—	15	—	ns
twl[3]	—	Clock Pulse Duration, Low	12	—	15	—	ns
ten	2	Input or I/O to Output Enabled	—	20	—	25	ns
	2	OE↓ to Output Enabled	—	18	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	20	—	25	ns
	3	OE↑ to Output Disabled	—	18	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Description** section.
3) Clock pulses of widths less than the specification may be detected as valid clock signals.

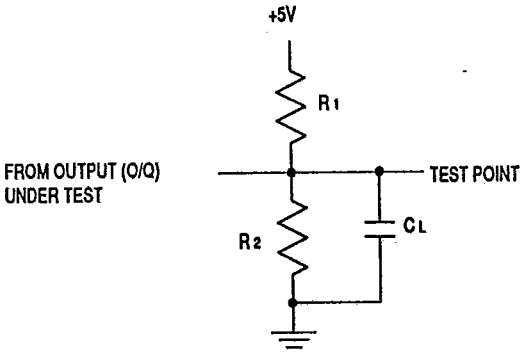
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

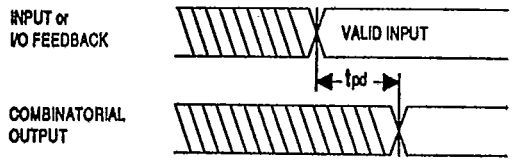
Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

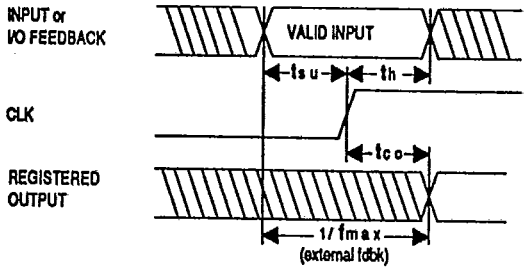


CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

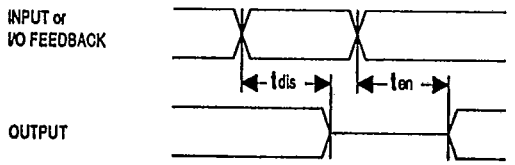
SWITCHING WAVEFORMS



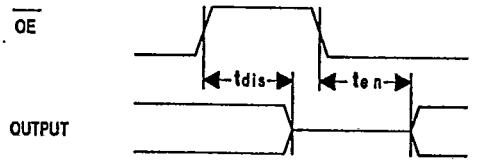
Combinatorial Output



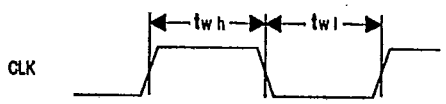
Registered Output



Input or I/O to Output Enable/Disable

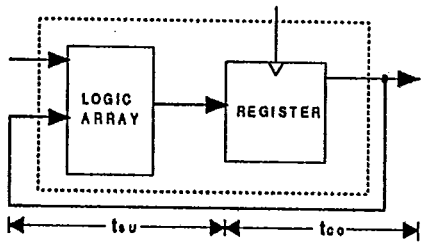


$\overline{OE}$ to Output Enable/Disable



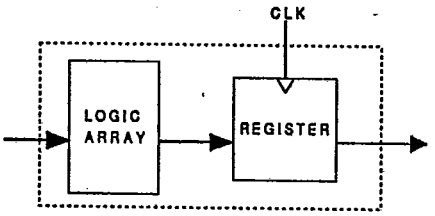
Clock Width

fmax DESCRIPTIONS



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax With No Feedback

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Specifications *ispGAL16Z8*

T-46-19-07

2

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided as part of the ispGAL16Z8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

The security cell is provided on the ispGAL16Z8 device to prevent unauthorized copying of the logic pattern. Once programmed, this cell prevents further read access to the functional bits in the device. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

The ispGAL16Z8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

TC CELL

The ispGAL16Z8 devices are equipped with a TC (Tri-State Control) cell which controls the state of the outputs when the device is being programmed. Since the device is programmed while on the circuit board, and connected to other devices, the state of the outputs is very important. Depending on how the TC cell is programmed, the outputs will either be tri-stated or latched upon entering the programming/diagnostic mode.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

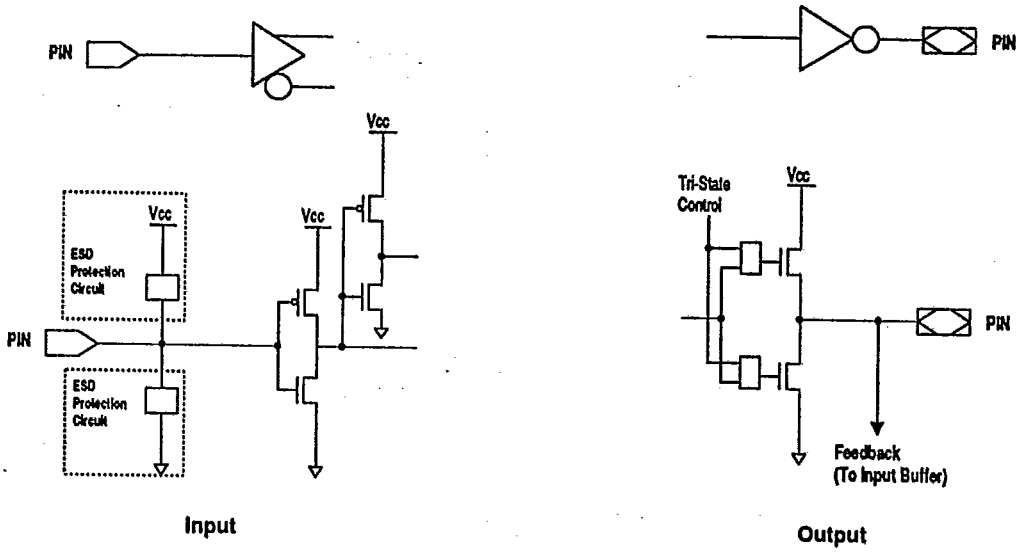
The ispGAL16Z8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any state condition can be forced for test sequencing.

INPUT BUFFERS

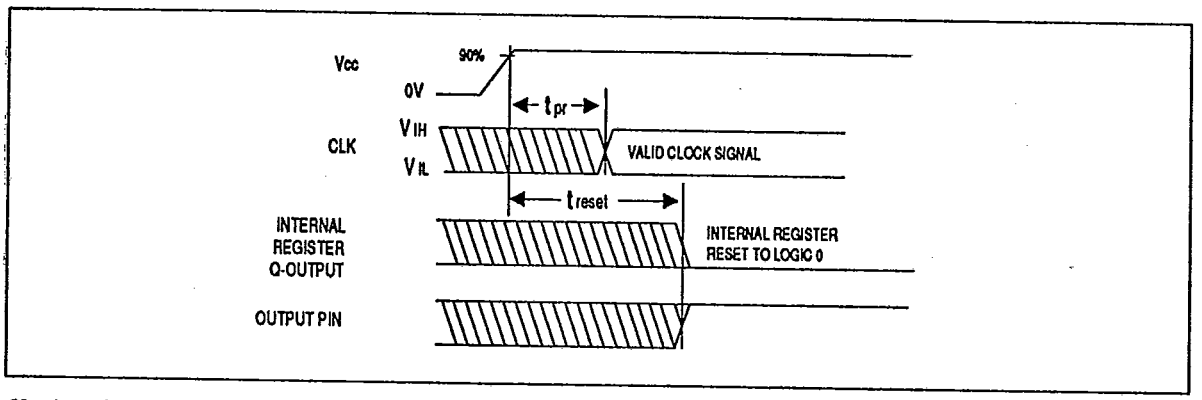
The ispGAL16Z8 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load the driving logic much less than traditional bipolar devices. Because the inputs are connected to a CMOS gate, there is no inherent pull-up structure, as there is with bipolar devices. Therefore, they cannot be depended on to float high (or to any particular state), and must be tied to the desired logic state.

Unused inputs and tri-stated I/Os should not be left floating. Lattice recommends that they be connected to Vcc, Ground, or another driven input. Doing so will tend to increase noise immunity and reduce Icc for the device.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



POWER-UP RESET



Circuitry within the ispGAL16Z8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.