MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

DESCRIPTION

The M37710E4LXXXFP is a built-in PROM single-chip microcomputer designed with high-performance CMOS silicon gate technology. This is housed in a small 80-pin plastic molded QFP. The features of this chip are similar to those of the M37710M4BXXXFP except that this chip has a 32K-byte PROM built in.

This single-chip microcomputer has a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for communication, office, business and industrial equipment controller that require high-speed processing of large data. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

FEATURES

● Number of basic instructions ···························· 103
● Memory size   PROM(one time) ·············· 32K bytes
                 RAM ···························· 1024 bytes
● Instruction execution time
  The fastest instruction at 8MHz frequency ·········· 500ns
● Single low supply voltage ························· 2.7~5.5V

● Low power dissipation
  (At 3V supply voltage, 8MHz frequency) ··· 12mW (Typ.)
  (At 5V supply voltage, 8MHz frequency) ··· 30mW (Typ.)
● Wide operating temperature range ············· −40~85℃
● Interrupts ···································· 19 types 7 levels
● Multiple function 16-bit timer ······························· 5+3
  (Pulse motor drive waveform can be output)
● UART (may also be synchronous) ··························· 2
● 10-bit A-D converter························· 8-channel inputs
● 8-bit D-A converter ·························2-channel outputs
● 12-bit watchdog timer
● Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) ·············· 68

APPLICATION

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers
Control devices for industrial equipment such as ME, NC, communication, portable equipment, and measuring instruments

NOTE

Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

PIN CONFIGURATION (TOP VIEW)

Left side pins (top to bottom):
- P8₃/TxD₀ ↔ 65
- P8₂/RxD₀ ↔ 66
- P8₁/CLK₀ ↔ 67
- P8₀/CTS₀/RTS₀/DA₀ ↔ 68
- Vcc 69
- AVcc 70
- VREF → 71
- AVss 72
- Vss 73
- P7₇/AN₇/ADTRG ↔ 74
- P7₆/AN₆ ↔ 75
- P7₅/AN₅ ↔ 76
- P7₄/AN₄ ↔ 77
- P7₃/AN₃ ↔ 78
- P7₂/AN₂ ↔ 79
- P7₁/AN₁ ↔ 80

Right side pins (top to bottom):
- 40 ↔ P2₄/A₂₀/D₄
- 39 ↔ P2₅/A₂₁/D₅
- 38 ↔ P2₆/A₂₂/D₆
- 37 ↔ P2₇/A₂₃/D₇
- 36 ↔ P3₀/R/W
- 35 ↔ P3₁/BHE
- 34 ↔ P3₂/ALE
- 33 ↔ P3₃/HLDA
- 32 Vss
- 31 → E
- 30 → XOUT
- 29 → XIN
- 28 ← RESET
- 27 CNVss
- 26 ← BYTE
- 25 ↔ P4₀/HOLD

Chip label: M37710E4LXXXFP

Top pins (left to right): P8₄/CTS₁/RTS₁/DA₁, P8₅/CLK₁, P8₆/RxD₁, P8₇/TxD₁, P0₀/A₀, P0₁/A₁, P0₂/A₂, P0₃/A₃, P0₄/A₄, P0₅/A₅, P0₆/A₆, P0₇/A₇, P1₀/A₈/D₈, P1₁/A₉/D₉, P1₂/A₁₀/D₁₀, P1₃/A₁₁/D₁₁, P1₄/A₁₂/D₁₂, P1₅/A₁₃/D₁₃, P1₆/A₁₄/D₁₄, P1₇/A₁₅/D₁₅, P2₀/A₁₆/D₀, P2₁/A₁₇/D₁, P2₂/A₁₈/D₂, P2₃/A₁₉/D₃

Bottom pins (left to right): P7₀/AN₀, P6₇/TB2IN, P6₆/TB1IN, P6₅/TB0IN, P6₄/INT₂, P6₃/INT₁, P6₂/INT₀, P6₁/TA4IN, P6₀/TA4OUT/RTP1₃, P5₇/TA3IN, P5₆/TA3OUT/RTP1₂, P5₅/TA2IN, P5₄/TA2OUT/RTP1₁, P5₃/TA1IN, P5₂/TA1OUT/RTP1₀, P5₁/TA0IN, P5₀/TA0OUT/RTP0₃, P4₇/DBC*, P4₆/VPA*, P4₅/VDA*, P4₄/QCL*, P4₃/MX*, P4₂/φ₁, P4₁/RDY

Outline 80P6N-A

*: Used in the evaluation chip mode only

M37710E4LXXXFP BLOCK DIAGRAM

Bus width selection input BYTE

Reference voltage input V_{REF}

(5V) AV_{CC}

(0V) AV_{SS}

(0V) CNV_{SS}

(0V) V_{SS}

(5V) V_{CC}

Reset input RESET

Enable output E

Clock output X_{OUT}

Clock input X_{IN}

Clock Generating Circuit

Data Bus (Even)

Data Bus (Odd)

Data Buffer DB$_H$(8)

Data Buffer DB$_L$(8)

Instruction Register (8)

Instruction Queue Buffer Q$_0$(8)

Instruction Queue Buffer Q$_1$(8)

Instruction Queue Buffer Q$_2$(8)

Incrementer (24)

Program Address Register PA(24)

Data Address Register DA(24)

Address Bus

Incrementer/Decrementer (24)

Program Counter PC(16)

Program Bank Register PG(8)

Data Bank Register DT(8)

Input Buffer Register IB(16)

Processor Status Register PS(11)

Direct Page Register DPR(16)

Stack Pointer S(16)

Index Register Y(16)

Index Register X(16)

Accumulator B(16)

Accumulator A(16)

Arithmetic Logic Unit(16)

D-A$_1$ Converter(8)

D-A$_0$ Converter(8)

A-D Converter(10)

UART1(9)

UART0(9)

Watchdog Timer

Timer TB2(16)

Timer TB1(16)

Timer TB0(16)

Timer TA4(16)

Timer TA3(16)

Timer TA2(16)

Timer TA1(16)

Timer TA0(16)

RAM 1024 Bytes

PROM 32K Bytes

P0(8) — Input/Output port P0

P1(8) — Input/Output port P1

P2(8) — Input/Output port P2

P3(4) — Input/Output port P3

P4(8) — Input/Output port P4

P5(8) — Input/Output port P5

P6(8) — Input/Output port P6

P7(8) — Input/Output port P7

P8(8) — Input/Output port P8

MITSUBISHI MICROCOMPUTERS
M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

FUNCTIONS OF M37710E4LXXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		500ns (the fastest instruction at external clock 8MHz frequency)
Memory size	PROM	32K bytes
	RAM	1024 bytes
Input/Output ports	P0~P2, P4~P8	8 -bit×8
	P3	4 -bit×1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit×5
	TB0, TB1, TB2	16-bit×3
Serial I/O		(UART or clock synchronous serial I/O)×2
A-D converter		10-bit×1 (8 channels)
D-A converter		8 -bit×2
Watchdog timer		12-bit×1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0~7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		2.7~5.5V
Power dissipation		12mW (At 3V supply voltage, external clock 8MHz frequency)
		30mW (At 5V supply voltage, external clock 8MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16M bytes
Operating temperature range		−40~85℃
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded QFP

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 2.7 to 5.5V to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS} input	Input	This pin controls the processor mode. Connect to V_{SS} for single-chip mode, and to V_{CC} for external ROM types.
$\overline{RESET}$	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV_{CC} AV_{SS}	Analog supply input		Power supply for the A-D converter. AV_{SS} is also used for D-A converter. Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS} externally.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter and the D-A converter.
$P0_0 \sim P0_7$	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address($A_7 \sim A_0$) is output in memory expansion mode or microprocessor mode.
$P1_0 \sim P1_7$	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data ($D_{15} \sim D_8$) is input or output when $\overline{E}$ output is "L" and an address ($A_{15} \sim A_8$) is output when $\overline{E}$ output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address($A_{15} \sim A_8$) is output.
$P2_0 \sim P2_7$	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data($D_7 \sim D_0$) is input or output when $\overline{E}$ output is "L" and an address($A_{23} \sim A_{16}$) is output when $\overline{E}$ output is "H".
$P3_0 \sim P3_3$	I/O port P3	I/O	In single-chip mode , these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/$\overline{W}$, $\overline{BHE}$, ALE, and $\overline{HLDA}$ signals are output.
$P4_0 \sim P4_7$	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$ and $P4_1$ become $\overline{HOLD}$ and $\overline{RDY}$ input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port $P4_2$ can be programmed for ϕ_1 output pin divided the clock to X_{IN} pin by 2. In microprocessor mode, $P4_2$ always has the function as ϕ_1 output pin.
$P5_0 \sim P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3. $P5_0 \sim P5_6$ also function as output pins for pulse motor drive waveform.
$P6_0 \sim P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input $\overline{INT_0}$, $\overline{INT_1}$ and $\overline{INT_2}$ pins, and input pins for timer B0, timer B1 and timer B2. $P6_0$ also functions as an output pin for pulse motor drive waveform.
$P7_0 \sim P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input $AN_0 \sim AN_7$ input pins. $P7_7$ also has an A-D conversion trigger input function.
$P8_0 \sim P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as R_XD, T_XD, CLK, $\overline{CTS}/\overline{RTS}$ pins for UART 0 and UART 1, and output pins for D-A converter.

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5 V$\pm$10% to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
BYTE	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV_{CC}, AV_{SS}	Analog supply input		Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
$P0_0 \sim P0_7$	Address input ($A_0 \sim A_7$)	Input	Port P0 functions as the lower 8 bits address input ($A_0 \sim A_7$).
$P1_0 \sim P1_7$	Address input ($A_8 \sim A_{15}$)	Input	Port $P1_0 \sim P1_7$ functions as the higher 8 bits address input ($A_8 \sim A_{15}$). In 256K mode, connect $P1_7$ to V_{CC}.
$P2_0 \sim P2_7$	Data I/O ($D_0 \sim D_7$)	I/O	Port P2 functions as the 8 bits data bus ($D_0 \sim D_7$).
$P3_0 \sim P3_3$	Input port P3	Input	Connect to V_{SS}.
$P4_0 \sim P4_7$	Input port P4	Input	Connect to V_{SS}.
$P5_0 \sim P5_7$	Control signal input	Input	$P5_0*$, $P5_1$ and $P5_2$ functions as $\overline{PGM}*$, $\overline{OE}$ and $\overline{CE}$ input pin respectively. Connect $P5_3$, $P5_4$ and $P5_5$ to V_{CC}. Connect $P5_6$ to V_{SS} in 256K mode and to V_{CC} in 1M mode. Connect $P5_7$ to V_{SS}.
$P6_0 \sim P6_7$	Input port P6	Input	Connect to V_{SS}.
$P7_0 \sim P7_7$	Input port P7	Input	Connect to V_{SS}.
$P8_0 \sim P8_7$	Input port P8	Input	Connect to V_{SS}.

∗ : It is available in 1M mode.

PROM VERSION of M37710M4LXXXFP

BASIC FUNCTION BLOCKS

The M37710E4LXXXFP has the same functions as the M37710M4BXXXFP except for the following:

(1) The external ROM is PROM.

(2) The reset circuit is different.

Therefore, refer to the section on the M37710M4BXXXFP.

MEMORY

The memory map is shown in Figure 1.

Fig. 1 Memory map

MITSUBISHI MICROCOMPUTERS
M37710E4LXXXFP
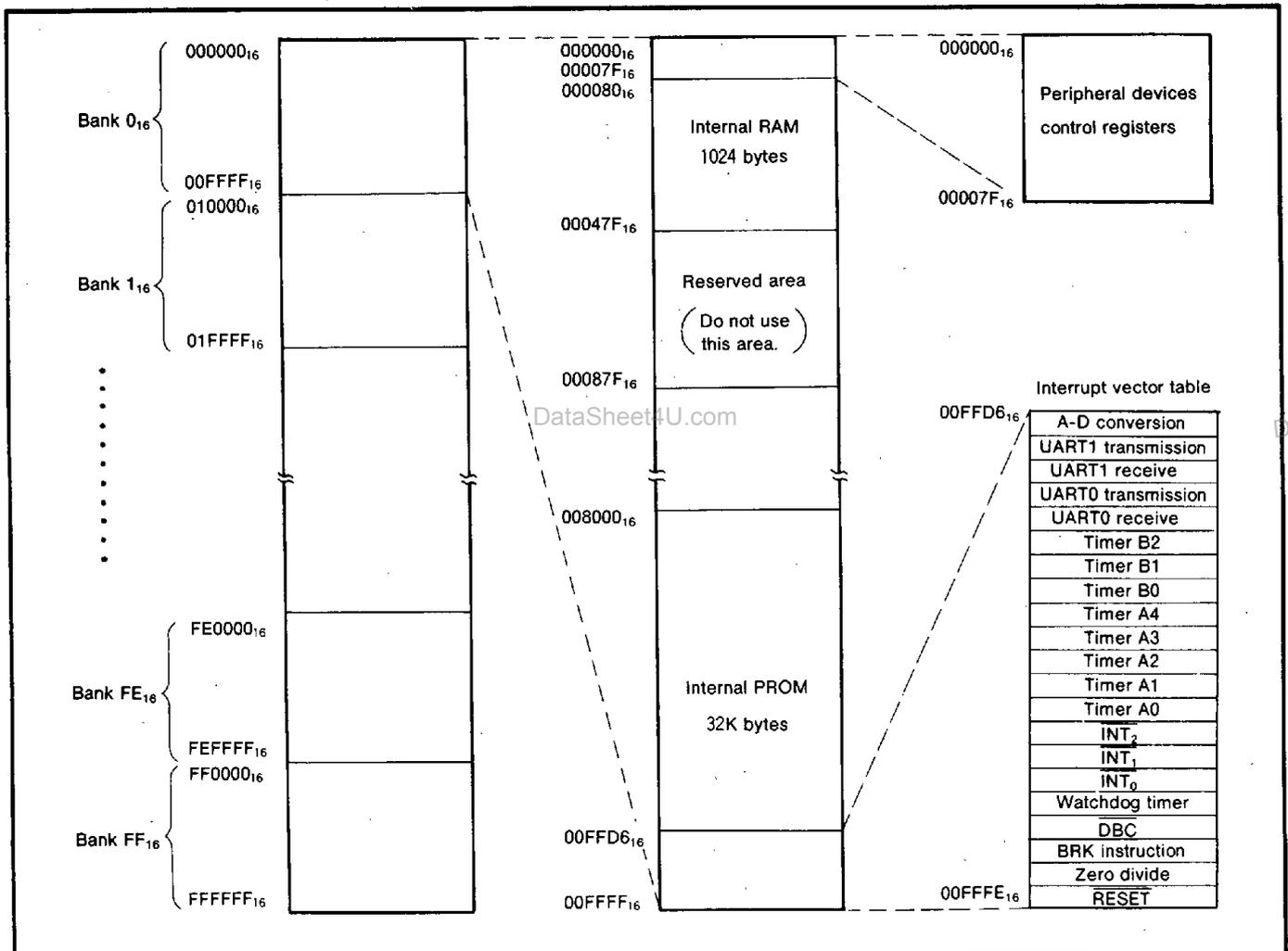
PROM VERSION of M37710M4LXXXFP

RESET CIRCUIT

Reset occurs when the RESET pin is returned to "H" level after holding it at "L" level when the power voltage is at 2.7 to 5.5V. Program execution starts at the address formed by setting the address pins $A_{23} \sim A_{16}$ to 00_{16}, $A_{15} \sim A_8$ to the contents of address $FFFF_{16}$, and $A_7 \sim A_0$ to the contents of address $FFFE_{16}$.

Figure 2 shows the status of the internal registers when a reset occurs.

Figure 3 shows an example of a reset circuit. The reset input voltage must be held 0.55V or lower when the power voltage reaches 2.7V.
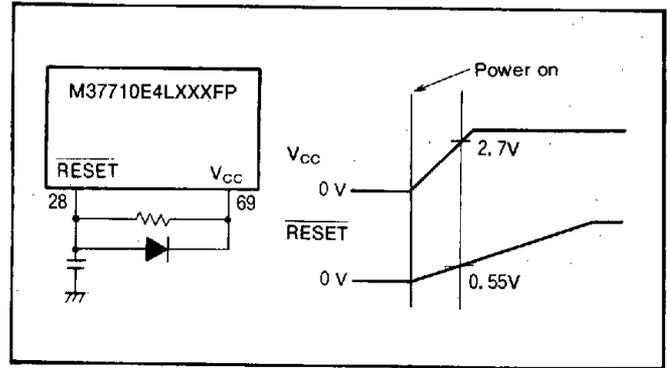
Fig. 3 Example of a reset circuit (perform careful evaluation at the system design level before using)

		Address												Address							
(1)	Port P0 data direction register	$(04_{16})\cdots$	00_{16}						(29)	Processor mode register 0	$(5E_{16})\cdots$	00_{16}								
(2)	Port P1 data direction register	$(05_{16})\cdots$	00_{16}						(30)	Processor mode register 1	$(5F_{16})\cdots$							0		
(3)	Port P2 data direction register	$(08_{16})\cdots$	00_{16}						(31)	Watchdog timer	$(60_{16})\cdots$	FFF_{16}								
(4)	Port P3 data direction register	$(09_{16})\cdots$					0	0	0	0	(32)	Watchdog timer frequency selection flag	$(61_{16})\cdots$							0
(5)	Port P4 data direction register	$(0C_{16})\cdots$	00_{16}						(33)	Waveform output mode register	$(62_{16})\cdots$	00_{16}								
(6)	Port P5 data direction register	$(0D_{16})\cdots$	00_{16}						(34)	Reserved area (Do not write to this address)	$(66_{16})\cdots$	00_{16}								
(7)	Port P6 data direction register	$(10_{16})\cdots$	00_{16}						(35)	A-D conversion interrupt control register	$(70_{16})\cdots$					0	0	0	0
(8)	Port P7 data direction register	$(11_{16})\cdots$	00_{16}						(36)	UART 0 transmission interrupt control register	$(71_{16})\cdots$					0	0	0	0
(9)	Port P8 data direction register	$(14_{16})\cdots$	00_{16}						(37)	UART 0 receive interrupt control register	$(72_{16})\cdots$					0	0	0	0
(10)	A-D control register 0	$(1E_{16})\cdots$	0	0	0	0	0	?	?	?	(38)	UART 1 transmission interrupt control register	$(73_{16})\cdots$					0	0	0	0
(11)	A-D control register 1	$(1F_{16})\cdots$	0	0		0	0	0	1	1	(39)	UART 1 receive interrupt control register	$(74_{16})\cdots$					0	0	0	0
(12)	UART 0 Transmit/Receive mode register	$(30_{16})\cdots$	00_{16}						(40)	Timer A0 interrupt control register	$(75_{16})\cdots$					0	0	0	0
(13)	UART 1 Transmit/Receive mode register	$(38_{16})\cdots$	00_{16}						(41)	Timer A1 interrupt control register	$(76_{16})\cdots$					0	0	0	0
(14)	UART 0 Transmit/Receive control register 0	$(34_{16})\cdots$				0	1	0	0	0	(42)	Timer A2 interrupt control register	$(77_{16})\cdots$					0	0	0	0
(15)	UART 1 Transmit/Receive control register 0	$(3C_{16})\cdots$				0	1	0	0	0	(43)	Timer A3 interrupt control register	$(78_{16})\cdots$					0	0	0	0
(16)	UART 0 Transmit/Receive control register 1	$(35_{16})\cdots$	0	0	0	0	0	0	1	0	(44)	Timer A4 interrupt control register	$(79_{16})\cdots$					0	0	0	0
(17)	UART 1 Transmit/Receive control register 1	$(3D_{16})\cdots$	0	0	0	0	0	0	1	0	(45)	Timer B0 interrupt control register	$(7A_{16})\cdots$					0	0	0	0
(18)	Count start flag	$(40_{16})\cdots$	00_{16}						(46)	Timer B1 interrupt control register	$(7B_{16})\cdots$					0	0	0	0
(19)	One-shot start flag	$(42_{16})\cdots$			0	0	0	0	0	(47)	Timer B2 interrupt control register	$(7C_{16})\cdots$					0	0	0	0
(20)	Up-down flag	$(44_{16})\cdots$	00_{16}						(48)	$\overline{INT}_0$ interrupt control register	$(7D_{16})\cdots$			0	0	0	0	0	0
(21)	Timer A0 mode register	$(56_{16})\cdots$	00_{16}						(49)	$\overline{INT}_1$ interrupt control register	$(7E_{16})\cdots$			0	0	0	0	0	0
(22)	Timer A1 mode register	$(57_{16})\cdots$	00_{16}						(50)	$\overline{INT}_2$ interrupt control register	$(7F_{16})\cdots$		0	0	0	0	0	0
(23)	Timer A2 mode register	$(58_{16})\cdots$	00_{16}						(51)	Processor status register PS		0	0	0	?	?	0	0	0	1	?	?
(24)	Timer A3 mode register	$(59_{16})\cdots$	00_{16}						(52)	Program bank register PG		00_{16}								
(25)	Timer A4 mode register	$(5A_{16})\cdots$	00_{16}						(53)	Program counter PC_H		Content of $FFFF_{16}$								
(26)	Timer B0 mode register	$(5B_{16})\cdots$	0	0	1	0	0	0	0	0	(54)	Program counter PC_L		Content of $FFFE_{16}$								
(27)	Timer B1 mode register	$(5C_{16})\cdots$	0	0	1		0	0	0	0	(55)	Direct page register DPR		0000_{16}								
(28)	Timer B2 mode register	$(5D_{16})\cdots$	0	0	1		0	0	0	0	(56)	Data bank register DT		00_{16}								

Contents of other registers and RAM are not initialized and should be initialized by software.

Fig. 2 Microcomputer internal status during reset

EPROM MODE

The M37710E4LXXXFP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

There are two EPROM modes. One is the 256K mode for the EPROM that is equivalent to the M5M27C256K, and the other is the 1M mode for the EPROM that is equivalent to the M5M27C101K. 256K mode is selected when port $P5_6$ is set to "L" level, and 1M mode is selected when it is set to "H" level.

When in the EPROM mode, ports P0, P1, P2, $P5_0$, $P5_1$, $P5_2$, CNV_{SS} and BYTE are used for the EPROM (equivalent to the M5M27C256K or M5M27C101K). When in this mode,

the built-in PROM can be written to or read from using these pins in the same way as with the M5M27C256K or M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address $0000_{16} \sim 7FFF_{16}$ in 256K mode, and address $18000_{16} \sim 1FFFF_{16}$ in 1M mode.

Connect the clock which is either ceramic resonator or external clock to X_{IN} pin and X_{OUT} pin.

For one time PROM version, 256K mode should be recommended to write more deeply.

* : Connect to ceramic oscillation circuit.

◯ : It is used in the EPROM mode.

Outline 80P6N-A
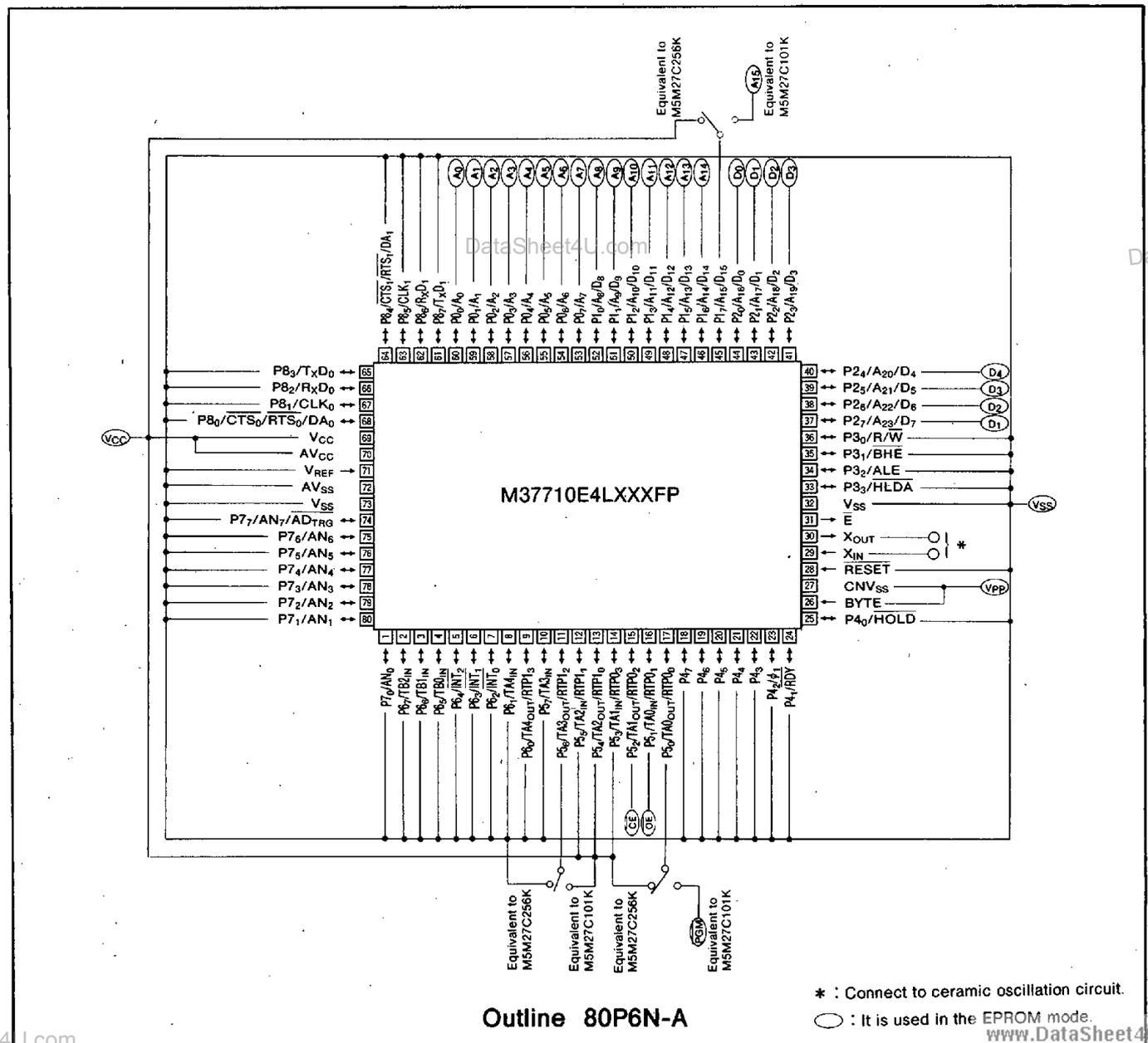
Fig. 4 Pin connection in EPROM mode

MITSUBISHI MICROCOMPUTERS
M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

Table 1. Pin function in EPROM mode

	M37710E4LXXXFP	M5M27C256K	M5M27C101K
V_{CC}	V_{CC}	V_{CC}	
V_{PP}	CNV_{SS}, BYTE	V_{PP}	
V_{SS}	V_{SS}	V_{SS}	
Address input	Ports P0, P1 *	$A_0 \sim A_{14}$	$A_0 \sim A_{15}$
Data I/O	Port P2	$D_0 \sim D_7$	
$\overline{CE}$	$P5_2$	$\overline{CE}$	
$\overline{OE}$	$P5_1$	$\overline{OE}$	
$\overline{PGM}$	$P5_0$ *	—	$\overline{PGM}$

* : In 256K mode, connect $P1_7$ and $P5_0$ to V_{CC}.

PROM VERSION of M37710M4LXXXFP

FUNCTION IN EPROM MODE
(1) 1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data $(A_0 \sim A_{15})$ to be read, and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

Writing must be performed in 8 bits by a byte program. To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when 12.5V is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{15}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{PGM}$ pin to a "L" level to being writing.

Writing operation

To program the M37710E4LXXXFP, first set V_{CC}=6V, V_{PP}= 12.5V, and set the address to 18000_{16}. Apply a 0.2ms write pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2ms write pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2X X ms).

When this series of write operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been written, read with $V_{CC}=V_{PP}$=5V(or $V_{CC}=V_{PP}$=5.5V).

Table 2. I/O signal in each mode

Pin / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	X	5 V	5 V	Output
Output Disable	V_{IL}	V_{IH}	X	5 V	5 V	Floating
	V_{IH}	X	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	V_{IL}	12.5V	6 V	Input
Programming Verify	V_{IL}	V_{IL}	V_{IH}	12.5V	6 V	Output
Program Disable	V_{IH}	V_{IH}	V_{IH}	12.5V	6 V	Floating

Note. An X indicates either V_{IL} or V_{IH}.

Program operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS (T_a=25±5℃, V_{CC}=6V±0.25V, V_{PP}=12.5±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

MITSUBISHI MICROCOMPUTERS
M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

AC waveforms
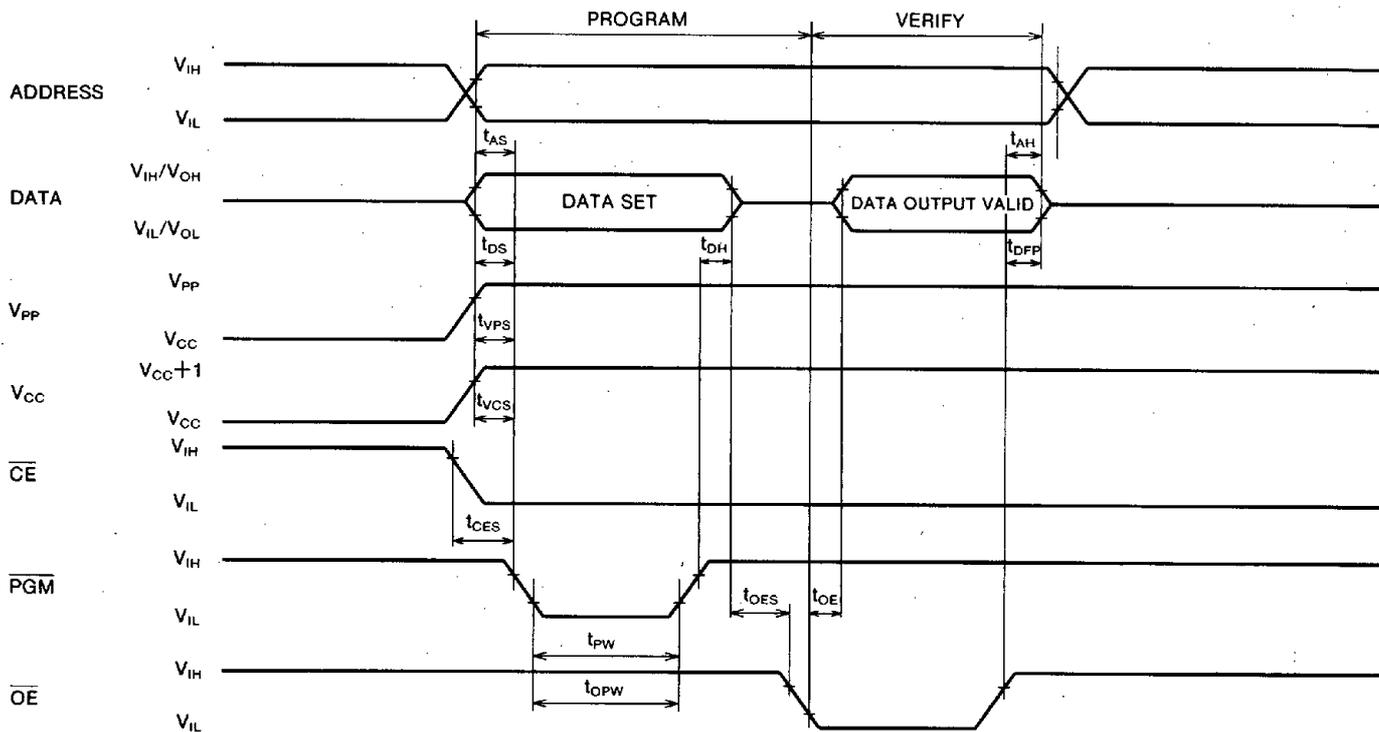
Test conditions for A.C. characteristics
Input voltage : $V_{IL}=0.45V$, $V_{IH}=2.4V$
Input rise and fall times (10%~90%) : $\leq 20ns$
Reference voltage at timing measurement : Input, Output
"L"=0.8V, "H"=2V

Programming algorithm flow chart
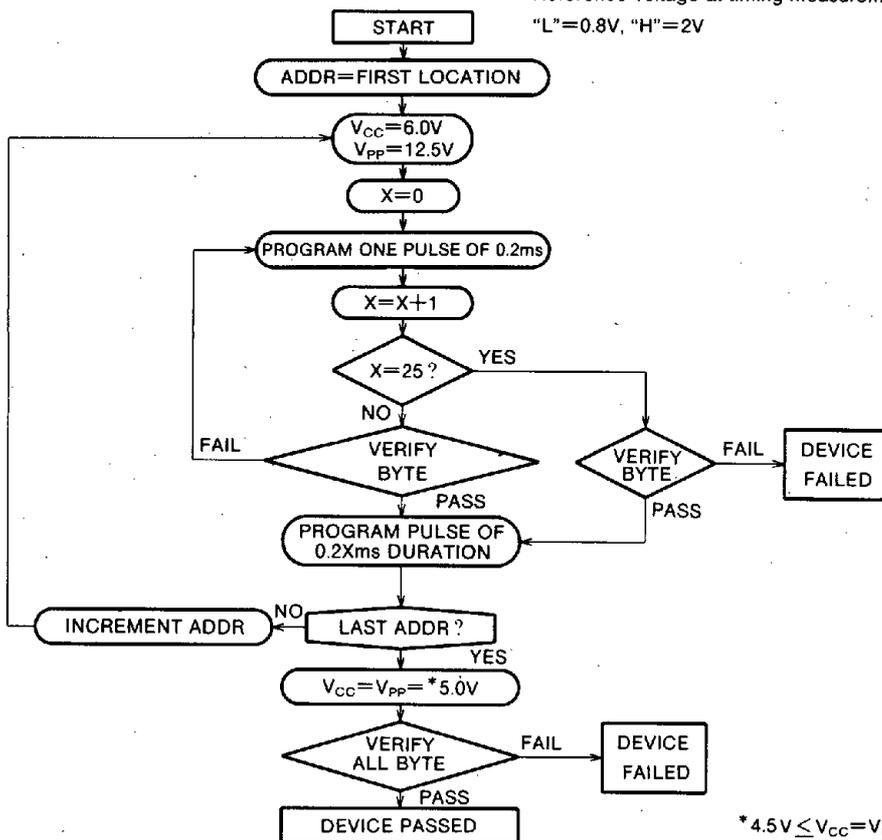
$*4.5V \leq V_{CC}=V_{PP}\leq 5.5V$

(2) 256K mode (equivalent to the M5M27C256K)

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data ($A_0 \sim A_{14}$) to be read, and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{14}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{CE}$ pin to a "L" level to being writing.

Writing operation

To program the M37710E4LXXXFP, first set $V_{CC}=6V$, $V_{PP}=12.5V$, and set the address to "0". Apply a 1ms write pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 1ms write pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further three times this number of pulses (3X X ms).

When this series of write operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been written, read with $V_{CC}=V_{PP}=5V$ (or $V_{CC}=V_{PP}=5.5V$).

Table 3. I/O signal in each mode

Pin / Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	5 V	5 V	Output
Output Disable	V_{IL}	V_{IH}	5 V	5 V	Floating
	V_{IH}	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	12.5V	6 V	Input
Programming Verify	V_{IH}	V_{IL}	12.5V	6 V	Output
Program Disable	V_{IH}	V_{IH}	12.5V	6 V	Floating

Note. An X indicates either V_{IL} or V_{IH}.

## Program operation (equivalent to the M5M27C256K)

AC ELECTRICAL CHARACTERISTICS ($T_a=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5\pm0.3V$, unless otherwise noted)

| Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC waveforms
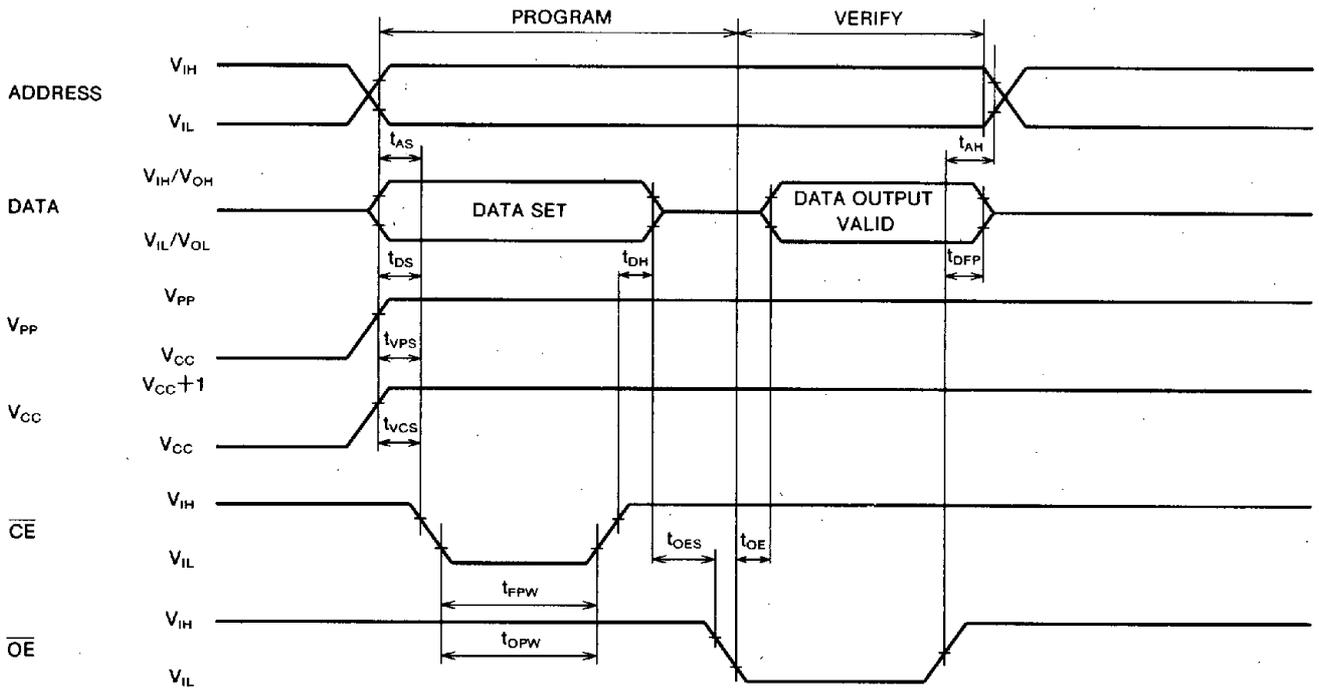
Programming algorithm flow chart
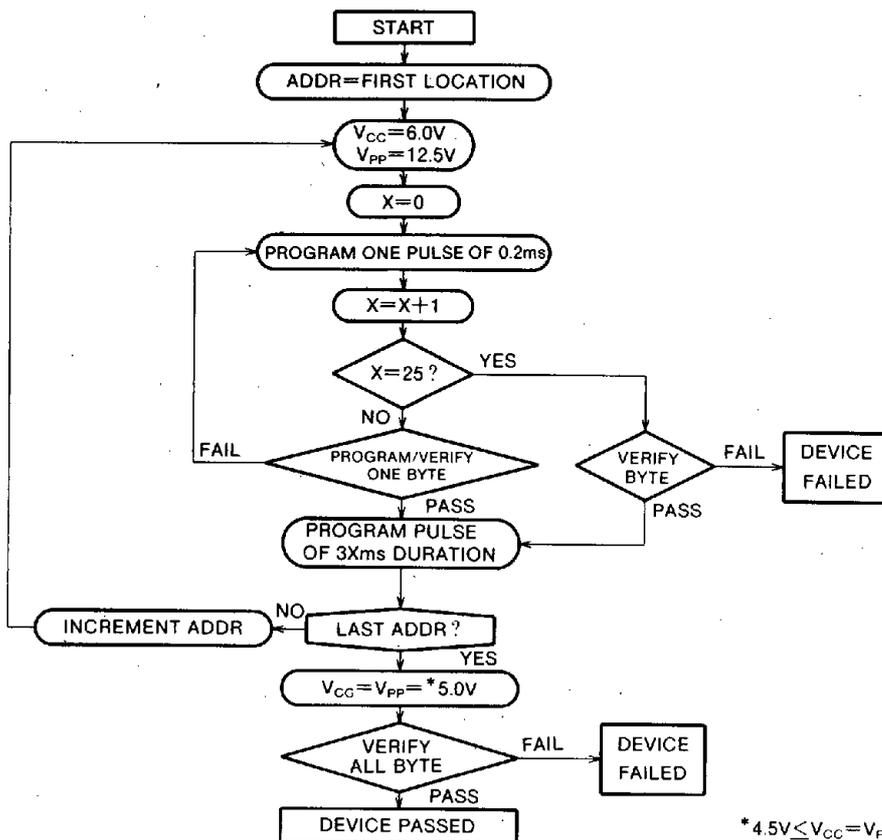

*$4.5V \leq V_{CC} = V_{PP} \leq 5.5V$

PROM VERSION of M37710M4LXXXFP

SAFETY INSTRUCTIONS

(1) A high voltage is used for writing. Take care that over-voltage is not applied. Take care especially at power on.

(2) The programmable M37710E4LFP that are shipped in blank is also provided.

For the M37710E4LFP, Mitsubishi Electric corp. does not perform PROM write test and screening following the assembly processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.

```
┌─────────────────────────────────┐
│    Writing with PROM writer     │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│   Screening      (Caution)      │
│ (Leave at 150℃ for 40 hours)    │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│   Verify test with PROM writer  │
└─────────────────────────────────┘
                │
                ▼
┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
   Function check in target device
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
```
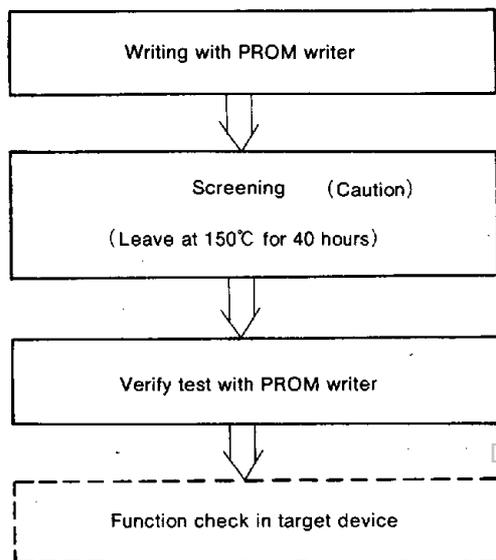
Caution : Never expose to 150 ℃ exceeding 100 hours because the screening temperature is higher than the storage temperature.

ADDRESSING MODES

The M37710E4LXXXFP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37710E4LXXXFP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.

(1) M37710E4LXXXFP writing to PROM order confirmation form

(2) 80P6N mark specification form

(3) ROM data (EPROM 3 sets)

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.3 \sim 7$	V
AV_{CC}	Analog supply voltage		$-0.3 \sim 7$	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}, BYTE		$-0.3 \sim 12$ (Note 1)	V
V_I	Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, V_{REF}, X_{IN}		$-0.3 \sim V_{CC} + 0.3$	V
V_O	Output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{OUT}, $\overline{E}$		$-0.3 \sim V_{CC} + 0.3$	V
P_d	Power dissipation	$Ta = 25°C$	300	mW
T_{opr}	Operating temperature		$-40 \sim 85$	°C
T_{stg}	Storage temperature		$-65 \sim 150$	°C

Note 1. Input voltage for CNV_{SS} and BYTE pins is 13V in writing to PROM.

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = 2.7 \sim 5.5V$, $Ta = -40 \sim 85°C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2.7		5.5	V
AV_{CC}	Analog supply voltage		V_{CC}		V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	High-level input voltage $P0_0 \sim P0_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	$0.8V_{CC}$		V_{CC}	V
V_{IH}	High-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in single-chip mode)	$0.8V_{CC}$		V_{CC}	V
V_{IH}	High-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in memory expansion mode and microprocessor mode)	$0.5V_{CC}$		V_{CC}	V
V_{IL}	Low-level input voltage $P0_0 \sim P0_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		$0.2V_{CC}$	V
V_{IL}	Low-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in single-chip mode)	0		$0.2V_{CC}$	V
V_{IL}	Low-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in memory expansion mode and microprocessor mode)	0		$0.16V_{CC}$	V
$I_{OH(peak)}$	High-level peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			-10	mA
$I_{OH(avg)}$	High-level average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			-5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			10	mA
$I_{OL(avg)}$	Low-level average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			5	mA
$f(X_{IN})$	External clock frequency input			8	MHz

Notes 2. Average output current is the average value of a 100ms interval.
   3. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less,
      the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less,
      the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less, and
      the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less.

MITSUBISHI MICROCOMPUTERS
M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f(X_{IN})$=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions			Min.	Typ.	Max.	Unit
V_{OH}	High-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$	V_{CC}=5V, I_{OH}=−10mA			3			V
		V_{CC}=3V, I_{OH}=−1mA			2.5			
V_{OH}	High-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$	V_{CC}=5V, I_{OH}=−400μA			4.7			V
V_{OH}	High-level output voltage $P3_2$	V_{CC}=5V, I_{OH}=−10mA			3.1			V
		V_{CC}=5V, I_{OH}=−400μA			4.8			
		V_{CC}=3V, I_{OH}=−1mA			2.6			
V_{OH}	High-level output voltage $\overline{E}$	V_{CC}=5V, I_{OH}=−10mA			3.4			V
		V_{CC}=5V, I_{OH}=−400μA			4.8			
		V_{CC}=3V, I_{OH}=−1mA			2.6			
V_{OL}	Low-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$	V_{CC}=5V, I_{OL}=10mA					2	V
		V_{CC}=3V, I_{OL}=1mA					0.5	
V_{OL}	Low-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$	V_{CC}=5V, I_{OL}=2mA					0.45	V
V_{OL}	Low-level output voltage $P3_2$	V_{CC}=5V, I_{OL}=10mA					1.9	V
		V_{CC}=5V, I_{OL}=2mA					0.43	
		V_{CC}=3V, I_{OL}=1mA					0.4	
V_{OL}	Low-level output voltage $\overline{E}$	V_{CC}=5V, I_{OL}=10mA					1.6	V
		V_{CC}=5V, I_{OL}=2mA					0.4	
		V_{CC}=3V, I_{OL}=1mA					0.4	
$V_{T+} - V_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN} \sim TA4_{IN}$, $TB0_{IN} \sim TB2_{IN}$, $\overline{INT_0} \sim \overline{INT_2}$, AD_{TRG}, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1	V_{CC}=5V			0.4		1	V
		V_{CC}=3V			0.1		0.7	
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.2		0.5	V
		V_{CC}=3V			0.1		0.4	
$V_{T+} - V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V			0.1		0.3	V
		V_{CC}=3V			0.06		0.2	
I_{IH}	High-level input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_{CC}=5V, V_I=5V					5	μA
		V_{CC}=3V, V_I=3V					4	
I_{IL}	Low-level input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_{CC}=5V, V_I=0V					−5	μA
		V_{CC}=3V, V_I=0V					−4	
V_{RAM}	RAM hold voltage	When clock is stopped.			2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.	$f(X_{IN})$=8MHz, square waveform	V_{CC}=5V		6	12	mA
				V_{CC}=3V		4	8	
			T_a=25℃ when clock is stopped.				1	μA
			T_a=85℃ when clock is stopped.				20	

PROM VERSION of M37710M4LXXXFP

A-D CONVERTER CHARACTERISTICS (V$_{CC}$=AV$_{CC}$=5V, V$_{SS}$=AV$_{SS}$=0V, T$_a$=25℃, f(X$_{IN}$)=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V$_{REF}$=V$_{CC}$			10	Bits
—	Absolute accuracy	V$_{REF}$=V$_{CC}$			±3	LSB
R$_{LADDER}$	Ladder resistance	V$_{REF}$=V$_{CC}$	5		20	kΩ
t$_{CONV}$	Conversion time		29.5			μs
V$_{REF}$	Reference voltage		2.7		V$_{CC}$	V
V$_{IA}$	Analog input voltage		0		V$_{REF}$	V

D-A CONVERTER CHARACTERISTICS (V$_{CC}$=5V, V$_{SS}$=AV$_{SS}$=0V, V$_{REF}$=5V, T$_a$=25℃, f(X$_{IN}$)=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
t$_{SU}$	Set time				3	μs
R$_O$	Output resistance		1	2.5	4	kΩ
I$_{VREF}$	Reference power input current	(Note)			3.2	mA

Note. One D-A converter is used, and the value of D-A register for unused D-A converter is "00$_{16}$".
Current that flows to the ladder resistance of A-D converter is excluded.

MITSUBISHI MICROCOMPUTERS
M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

TIMING REQUIREMENTS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

External clock input

Symbol	Parameter	Limits Min.	Limits Max.	Unit
t_C	External clock input cycle time	125		ns
$t_{W(H)}$	External clock input high-level pulse width	50		ns
$t_{W(L)}$	External clock input low-level pulse width	50		ns
t_r	External clock rise time		20	ns
t_f	External clock fall time		20	ns

Single-chip mode

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{SU(P0D-E)}$	Port P0 input setup time	300		ns
$t_{SU(P1D-E)}$	Port P1 input setup time	300		ns
$t_{SU(P2D-E)}$	Port P2 input setup time	300		ns
$t_{SU(P3D-E)}$	Port P3 input setup time	300		ns
$t_{SU(P4D-E)}$	Port P4 input setup time	300		ns
$t_{SU(P5D-E)}$	Port P5 input setup time	300		ns
$t_{SU(P6D-E)}$	Port P6 input setup time	300		ns
$t_{SU(P7D-E)}$	Port P7 input setup time	300		ns
$t_{SU(P8D-E)}$	Port P8 input setup time	300		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{SU(P1D-E)}$	Port P1 input setup time	80		ns
$t_{SU(P2D-E)}$	Port P2 input setup time	80		ns
$t_{SU(RDY-\phi_1)}$	RDY input setup time	90		ns
$t_{SU(HOLD-\phi_1)}$	HOLD input setup time	90		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(\phi_1-RDY)}$	RDY input hold time	0		ns
$t_{h(\phi_1-HOLD)}$	HOLD input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAi$_{IN}$ input cycle time	250		ns
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	125		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAi$_{IN}$ input cycle time	1000		ns
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	500		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	500		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAi$_{IN}$ input cycle time	500		ns
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	250		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	250		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAi$_{IN}$ Input high-level pulse width	250		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	250		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(UP)}$	TAi$_{OUT}$ input cycle time	5000		ns
$t_{W(UPH)}$	TAi$_{OUT}$ input high-level pulse width	2500		ns
$t_{W(UPL)}$	TAi$_{OUT}$ input low-level pulse width	2500		ns
$t_{SU(UP-T_{IN})}$	TAi$_{OUT}$ input setup time	1000		ns
$t_{h(T_{IN}-UP)}$	TAi$_{OUT}$ input hold time	1000		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time (one edge count)	250		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	125		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	125		ns
$t_{C(TB)}$	TBi_{IN} input cycle time (both edges count)	500		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	250		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time	1000		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width	500		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width	500		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time	1000		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width	500		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width	500		ns

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)	2000		ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	250		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(CK)}$	CLK_i input cycle time	500		ns
$t_{W(CKH)}$	CLK_i input high-level pulse width	250		ns
$t_{W(CKL)}$	CLK_i input low-level pulse width	250		ns
$t_{d(C-Q)}$	TxD_i output delay time		170	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	80		ns
$t_{h(C-D)}$	RxD_i input hold time	100		ns

External interrupt $\overline{INT_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{W(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

SWITCHING CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=25°C, $f(X_{IN})$=8MHz, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(E-P0Q)}$	Port P0 data output delay time			300	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time	Fig. 5		300	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			300	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(P0A-E)}$	Port P0 address output delay time		62		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			130	ns
$t_{pxz(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			10	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		62		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		52		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns
$t_{pxz(E-P2Z)}$	Port P2 floating start delay time			10	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		62		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		52		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time			120	ns
$t_{d(ALE-E)}$	ALE output delay time		4		ns
$t_{W(ALE)}$	ALE pulse width		82		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time	Fig. 5	62		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		62		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time		95		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		95		ns
$t_{pzx(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		95		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		95		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		95		ns
$t_{pzx(E-P2Z)}$	Port P2 floating release delay time		95		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		18		ns
$t_{W(EL)}$	$\overline{E}$ pulse width		220		ns

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

Memory expansion mode and microprocessor mode

(when wait bit = "0", wait selection bit = "1", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(P0A-E)}$	Port P0 address output delay time		62		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			130	ns
$t_{pxz(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			10	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		62		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		52		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns
$t_{pxz(E-P2Z)}$	Port P2 floating start delay time			10	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		62		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		52		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time	Fig. 5		120	ns
$t_{d(ALE-E)}$	ALE output delay time		4		ns
$t_{W(ALE)}$	ALE pulse width		82		ns
$t_{d(BHE-E)}$	BHE output delay time		62		ns
$t_{d(R/W-E)}$	R/W output delay time		62		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time		95		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		95		ns
$t_{pzx(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		95		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		95		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		95		ns
$t_{pzx(E-P2Z)}$	Port P2 floating release delay time		95		ns
$t_{h(E-BHE)}$	BHE hold time		18		ns
$t_{h(E-R/W)}$	R/W hold time		18		ns
$t_{W(EL)}$	E pulse width		470		ns

PROM VERSION of M37710M4LXXXFP

Memory expansion mode and microprocessor mode

(when wait bit = "0", wait selection bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(P0A-E)}$	Port P0 address output delay time		312		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			130	ns
$t_{pxz(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			10	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		312		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		177		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns
$t_{pxz(E-P2Z)}$	Port P2 floating start delay time			10	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		312		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		177		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time			120	ns
$t_{d(ALE-E)}$	ALE output delay time		100		ns
$t_{W(ALE)}$	ALE pulse width		207		ns
$t_{d(BHE-E)}$	BHE output delay time	Fig. 5	312		ns
$t_{d(R/W-E)}$	R/W output delay time		312		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time		95		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		105		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		95		ns
$t_{pzx(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		95		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		95		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		105		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		95		ns
$t_{pzx(E-P2Z)}$	Port P2 floating release delay time		95		ns
$t_{h(E-BHE)}$	BHE hold time		18		ns
$t_{h(E-R/W)}$	R/W hold time		18		ns
$t_{W(EL)}$	E pulse width		470		ns
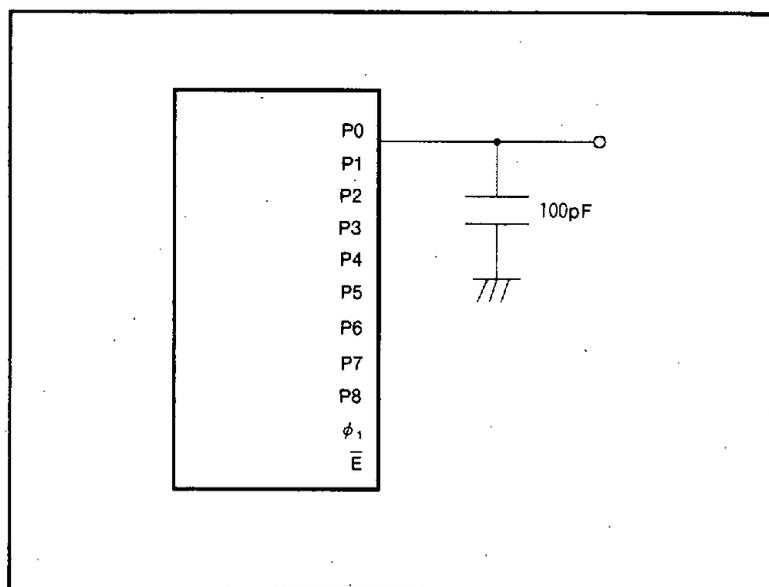
Fig. 5 Testing circuit for ports P0~P8, ϕ_1

TIMING DIAGRAM
### Single-chip mode
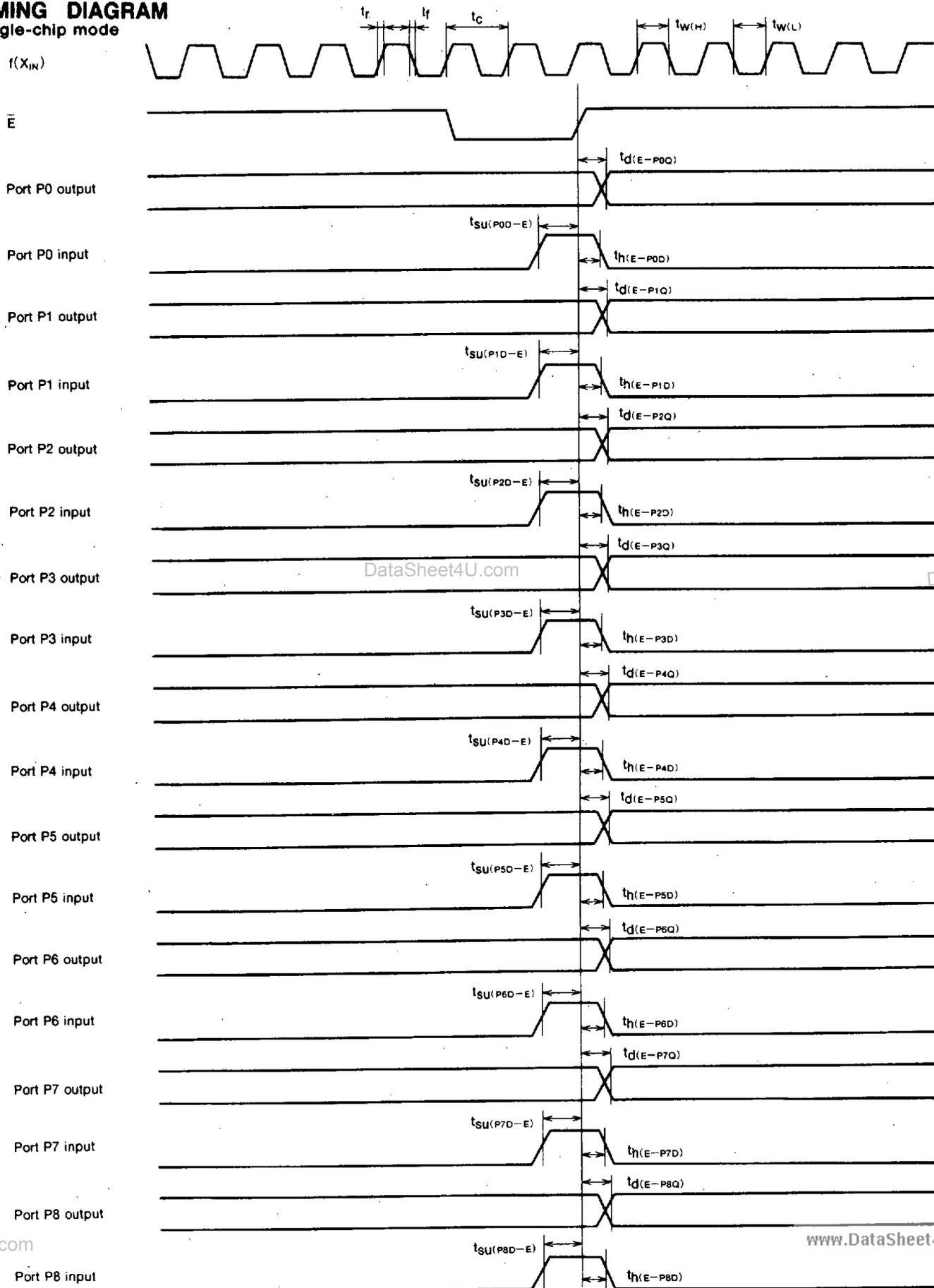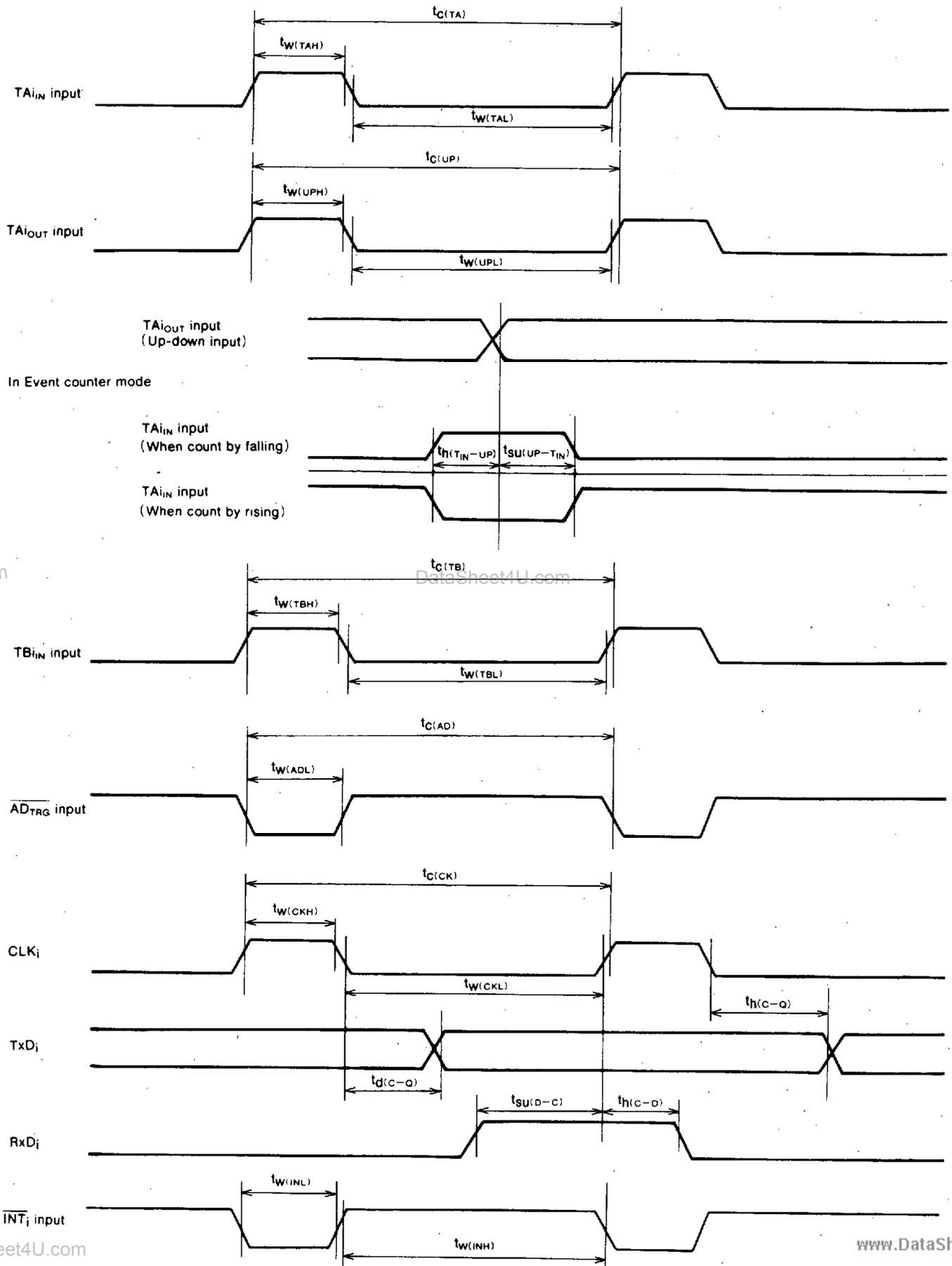
Memory expansion mode and microprocessor mode
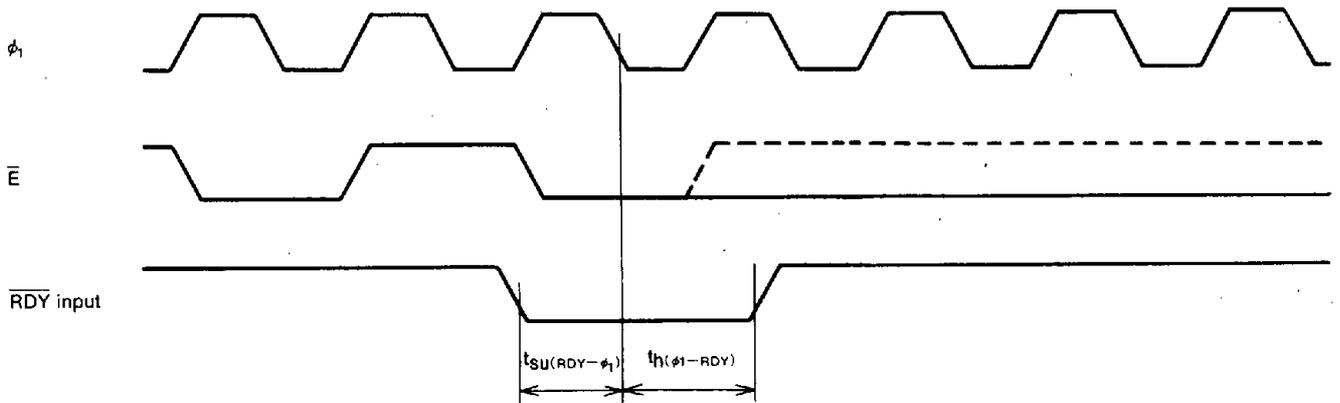
(When wait bit = "1")


(When wait bit = "0")
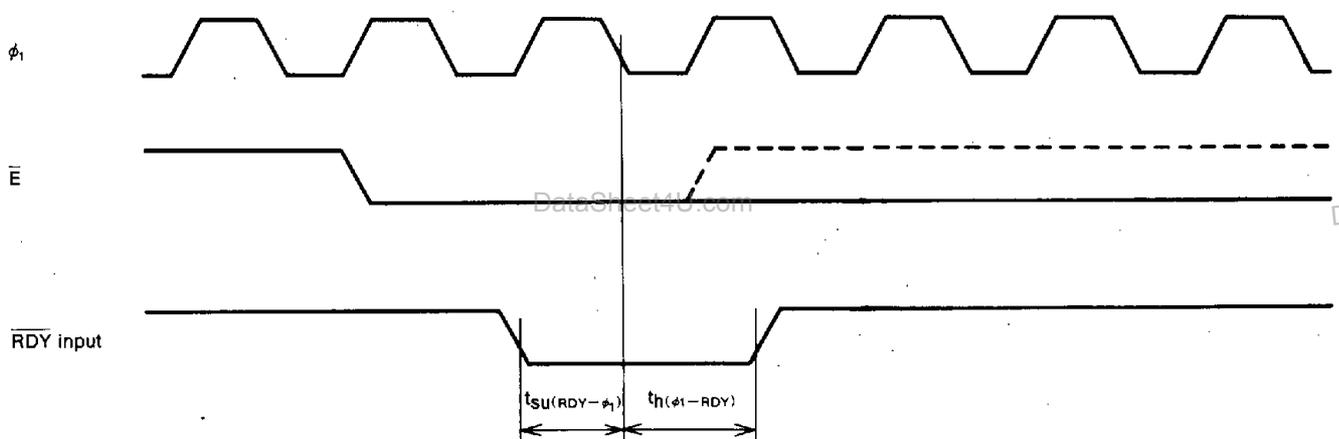


(When wait bit = "1" or "0" in common)
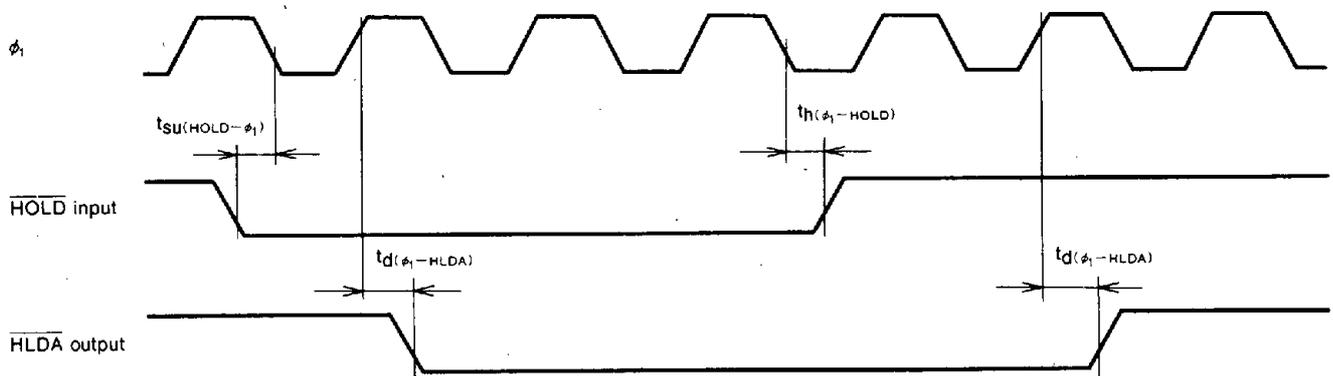
Test conditions

- $V_{CC} = 2.7 \sim 5.5V$
- Input timing voltage : $V_{IL} = 0.2V_{CC}$, $V_{IH} = 0.8V_{CC}$
- Output timing voltage : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

Memory expansion mode and microprocessor mode (When wait bit="1")

Test conditions

- $V_{CC}=2.7\sim5.5V$
- Output timing voltage : $V_{OL}=0.8V$, $V_{OH}=2.0V$
- Ports P1, P2 input : $V_{IL}=0.16V_{CC}$, $V_{IH}=0.5V_{CC}$

MITSUBISHI MICROCOMPUTERS

M37710E4LXXXFP

PROM VERSION of M37710M4LXXXFP

Memory expansion mode and microprocessor mode

(When wait bit = "0", wait selection bit = "1", and external memory area is accessed)

t_C

$f(X_{IN})$

ϕ_1

$t_{d(E-\phi_1)}$

$\overline{E}$

$t_{W(EL)}$ $t_{d(E-\phi_1)}$

$t_{h(E-P0A)}$ $t_{d(P0A-E)}$

Port P0 output ($A_0 \sim A_7$)

Address Address

$t_{h(ALE-P1A)}$ $t_{h(E-P1Q)}$ $t_{pxz(E-P1Z)}$ $t_{pzx(E-P1Z)}$

Port P1 output ($A_8 \sim A_{15}/D_8 \sim D_{15}$) (BYTE="L")

Address Data Address Address

$t_{d(P1A-ALE)}$ $t_{d(E-P1Q)}$

$t_{h(E-P1A)}$ $t_{d(P1A-E)}$

Port P1 output ($A_8 \sim A_{15}$) (BYTE="H")

Address Address

$t_{su(P1D-E)}$ $t_{h(E-P1D)}$

Port P1 input

$t_{h(ALE-P2A)}$ $t_{h(E-P2Q)}$ $t_{pxz(E-P2Z)}$ $t_{pzx(E-P2Z)}$

Port P2 output ($A_{16} \sim A_{23}/D_0 \sim D_7$)

Address Data Address Address

$t_{su(P2D-E)}$

$t_{d(P2A-ALE)}$ $t_{d(E-P2Q)}$ $t_{d(P2A-E)}$ $t_{h(E-P2D)}$

Port P2 input

$t_{W(ALE)}$

$t_{d(ALE-E)}$

Port P3$_2$ output (ALE)

$t_{d(BHE-E)}$ $t_{h(E-BHE)}$

Port P3$_1$ output ($\overline{BHE}$)

$t_{d(R/W-E)}$ $t_{h(E-R/W)}$

Port P3$_0$ output (R/$\overline{W}$)
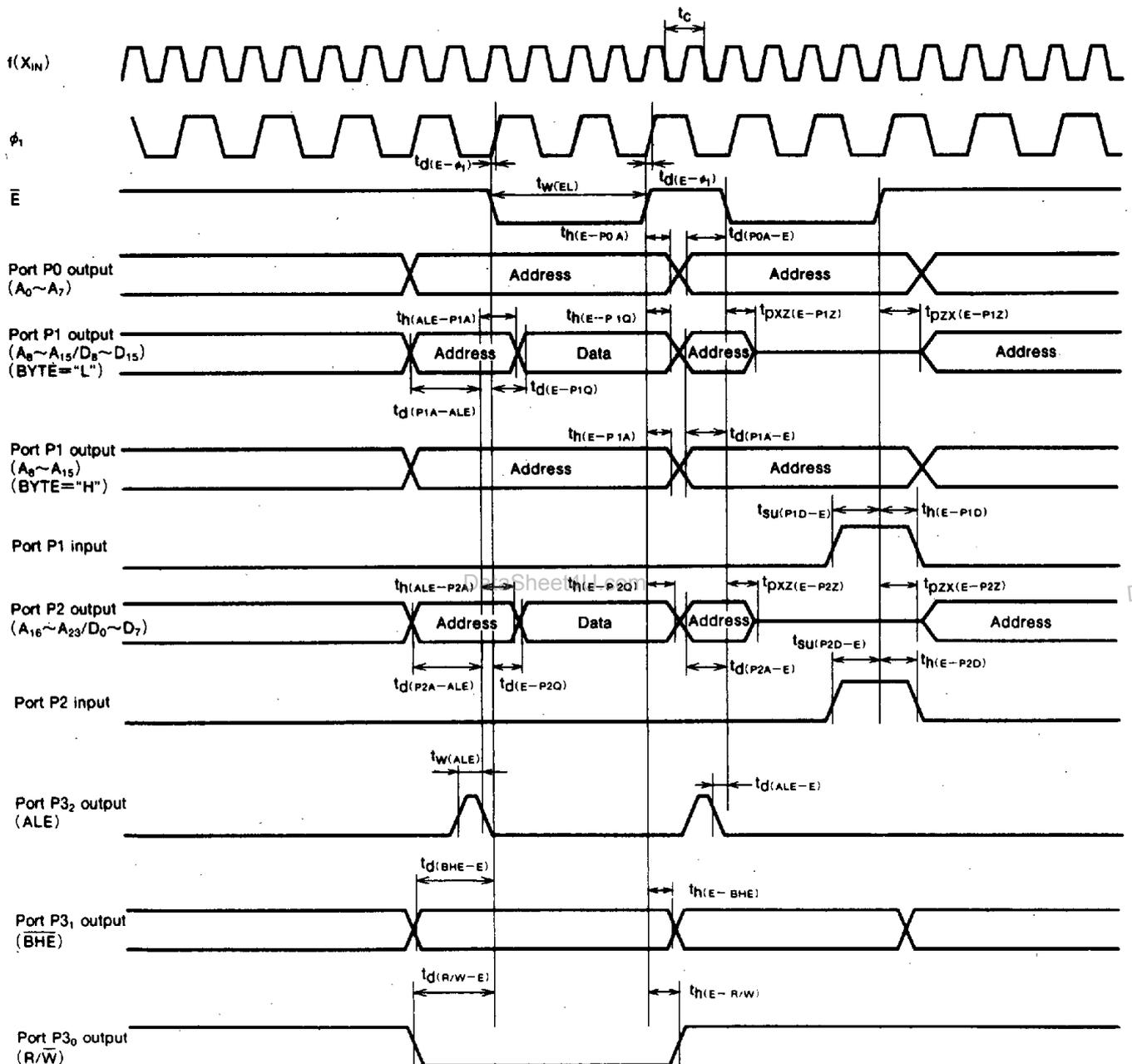
Test conditions

· $V_{CC}=2.7 \sim 5.5V$

· Output timing voltage : $V_{OL}=0.8V$, $V_{OH}=2.0V$

· Ports P1, P2 input : $V_{IL}=0.16V_{CC}$, $V_{IH}=0.5V_{CC}$

Memory expansion mode and microprocessor mode

(When wait bit = "0", wait selection bit = "0", and external memory area is accessed)

Test conditions

- $V_{CC} = 2.7 \sim 5.5V$

- Output timing voltage : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$

- Ports P1, P2 input : $V_{IL} = 0.16V_{CC}$, $V_{IH} = 0.5V_{CC}$

MITSUBISHI MEMORY CARD
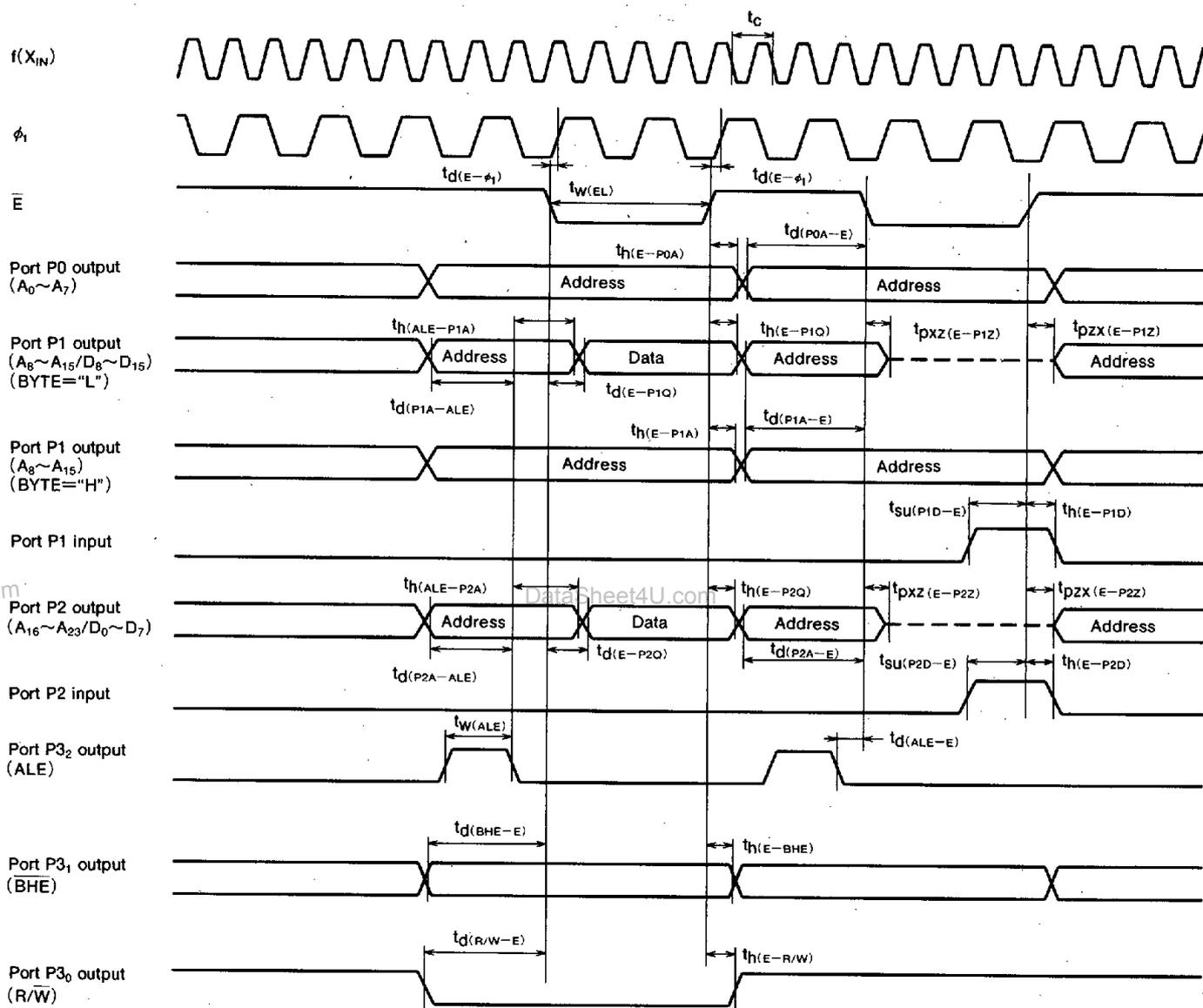
FLASH MEMORY CARDS

8/16-bit Data Bus Flash Memory Card

MF84M1-G1EATXX

Connector Type

Two-piece 68-pin

DESCRIPTION

The MF84M1-G1EATXX is a flash memory card which uses sixteen two-megabit flash electrically erasable and programmable read only memory IC's.

FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level
- Program/erase operation by software command control
- Program/erase voltage 12V
- 10,000 program/erase cycles
- Write protect switch

APPLICATIONS

- Note book computers
- Industrial machines
- Printers

PRODUCT LIST

Type name \ Item	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF84M1-G1EATXX	4 MB	8/16	250	Two-piece	68	68P-002

MITSUBISHI MEMORY CARD

FLASH MEMORY CARDS

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D 3	} Data I/O	36	$\overline{CD1}$	Card detect 1
3	D 4		37	D11	} Data I/O
4	D 5	Data I/O	38	D12	
5	D 6		39	D13	Data I/O
6	D 7		40	D14	
7	$\overline{CE1}$	Card enable 1	41	D15	
8	A10	Address input	42	$\overline{CE2}$	Card enable 2
9	$\overline{OE}$	Output enable	43	NC	} No connection
10	A11	} Address input	44	NC	No connection
11	A 9		45	NC	
12	A 8	Address input	46	A17	} Address input
13	A13		47	A18	
14	A14		48	A19	Address input
15	$\overline{WE}$	Write enable	49	A20	
16	NC	No connection	50	A21	
17	Vcc	Power supply voltage	51	Vcc	Power supply voltage
18	VPP 1	Programming supply voltage 1	52	VPP 2	Programming supply voltage 2
19	A16		53	NC	
20	A15		54	NC	
21	A12		55	NC	
22	A 7		56	NC	} No connection
23	A 6		57	NC	No connection
24	A 5	Address input	58	NC	
25	A 4		59	NC	
26	A 3		60	NC	
27	A 2		61	$\overline{REG}$	Attribute memory select
28	A 1		62	BVD 2	Battery voltage detect 2
29	A 0		63	BVD 1	Battery voltage detect 1
30	D 0	} Data I/O	64	D 8	} Data I/O
31	D 1	Data I/O	65	D 9	Data I/O
32	D 2		66	D10	
33	WP	Write protect	67	$\overline{CD2}$	Card detect 2
34	GND	Ground	68	GND	Ground

BLOCK DIAGRAM (MF84M1-G1EATXX)
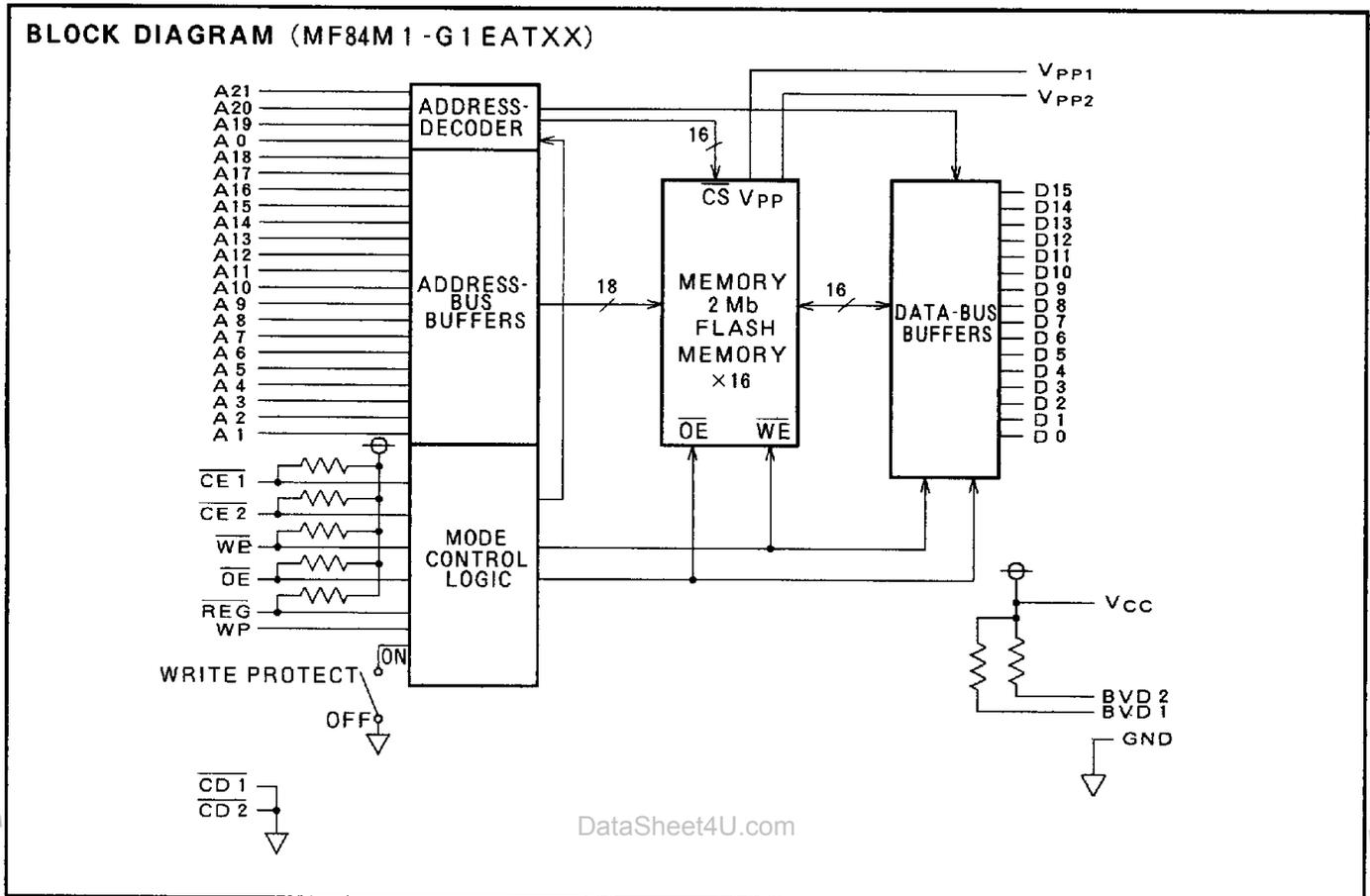
FUNCTIONAL DESCRIPTION

The operating mode of the card is determined by five active low control signals ($\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$), three supply voltages (V_{CC}, V_{PP1}, V_{PP2}) and control registers located in each memory IC.

Common memory function

When the $\overline{REG}$ signal is set to a high level common memory is selected.

Read only mode

When the voltages applied to both V_{PP1} and V_{PP2} are less than the voltage applied to V_{CC} (i. e. $V_{PP} =$ 0V to V_{CC}), the control registers of each memory IC are set to read only mode.

Operation of the card then depends on the four possible combinations of $\overline{CE1}$ and $\overline{CE2}$ (note/WE should be set to a high level when the device is in read only mode except during combination (4) where it's condition is unimportant) :

(1) If $\overline{CE1}$ is set to a low level and $\overline{CE2}$ is set to a high level, the card will work as an eight bit data bus width card. Data can be accessed via the lower

half of the data bus (D0 to D7).

(2) If both $\overline{CE1}$ and $\overline{CE2}$ are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.

(3) If $\overline{CE1}$ is set to a high level and $\overline{CE2}$ is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.

(4) If $\overline{CE1}$ and $\overline{CE2}$ are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When $\overline{OE}$ is set to a low level data can be read from the card, depending on the address applied and the setting of $\overline{CE1}$ and $\overline{CE2}$ as mentioned above, except under combination (4).

When $\overline{OE}$ is set to a high level and $\overline{WE}$ is set to a high level the card is in an output disable mode and the data bus will be in a high impedance state regardless of the condition of $\overline{CE1}$ and $\overline{CE2}$.

Read/write mode
When a programming voltage (VppH) is applied to either or both of Vpp1 and Vpp2, read/write mode is enabled for the corresponding banks of memory IC's inside the card. Vpp1 enables the Even Byte bank and Vpp2 enables the Odd Byte bank.

By using the 4 combinations of $\overline{CE1}$ and $\overline{CE2}$ as descibed under Read only mode above the appropriate Data Out and Command/Data In bus selection can be made.

If $\overline{OE}$ is set to a high level and $\overline{WE}$ set to a low level, the control register will latch command data applied at the rising edge of the $\overline{WE}$ signal. Note that more than one bus cycle may be required to latch the command and/or the related data — please refer to the Command Definition table.

If $\overline{OE}$ is set to a low level and $\overline{WE}$ is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details please refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

Attribute memory
When $\overline{REG}$ is set to a low level attribute memory is selected.

The card then outputs FFh on the lower half of the data bus (D0 to D7) when the following conditions are applied :

(1) $\overline{CE1}$: low level, $\overline{CE2}$: high level, $\overline{OE}$: low level, $\overline{WE}$: high level, A0 : low level
(2) $\overline{CE1}$: low level, $\overline{CE2}$: low level, $\overline{OE}$: low level, $\overline{WE}$: high level.

Write protect mode
The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and Vcc is applied. When the card is not in write protect mode the WP output pin is set to a low level when Vcc is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.