

PowerMOS transistor**PHT1N52R****GENERAL DESCRIPTION**

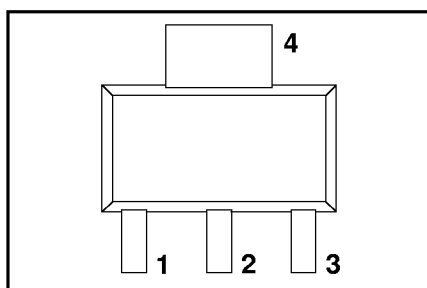
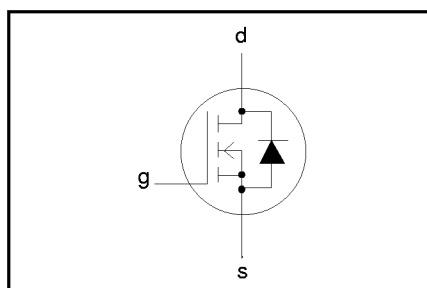
N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance. Intended for use in Compact Fluorescent Lights (CFL) and general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	520	V
I_D	Drain current (DC)	0.46	A
P_{tot}	Total power dissipation	8.3	W
$R_{DS(ON)}$	Drain-source on-state resistance	16	Ω

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION**SYMBOL****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	520	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	520	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	$T_{sp} = 25^\circ\text{C}$	-	0.46	A
		$T_{sp} = 100^\circ\text{C}$	-	0.3	A
I_{DM}	Drain current (pulse peak value)	$T_{sp} = 25^\circ\text{C}$	-	3.2	A
I_{DR}	Source-drain diode current (DC)	$T_{sp} = 25^\circ\text{C}$	-	0.5	A
I_{DRM}	Source-drain diode current (pulse peak value)	$T_{sp} = 25^\circ\text{C}$	-	3.2	A
P_{tot}	Total power dissipation	$T_{sp} = 25^\circ\text{C}$	-	8.3	W
T_{stg}	Storage temperature		-55	150	$^\circ\text{C}$
T_j	Junction temperature		-	150	$^\circ\text{C}$

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 2 \text{ A}$; $V_{DD} \leq 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \Omega$ $T_j = 25^\circ\text{C}$ prior to surge $T_j = 100^\circ\text{C}$ prior to surge	-	120	mJ
W_{DSR}^1	Drain-source repetitive unclamped inductive turn-off energy	$I_D = 2 \text{ A}$; $V_{DD} \leq 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \Omega$; $T_j \leq 150^\circ\text{C}$	-	20	mJ
			-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

PowerMOS transistor

PHT1N52R

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint pcb mounted; pad area as in fig:2	- -	156 70	- -	K/W K/W

STATIC CHARACTERISTICS

 $T_{mb} = 25\ ^\circ\text{C}$ unless otherwise specified

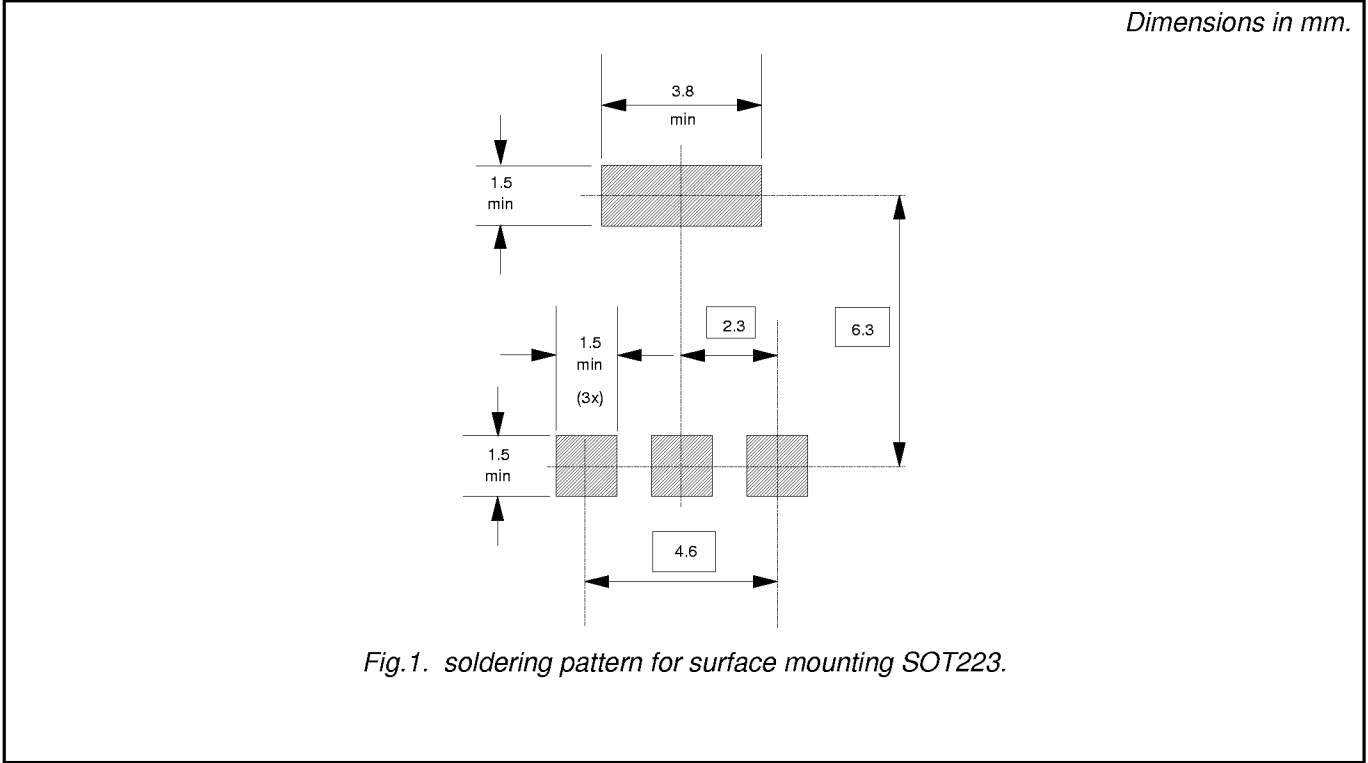
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	520	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	$V_{DS} = 500\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\ ^\circ\text{C}$	-	1	100	μA
		$V_{DS} = 400\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\ ^\circ\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 35\text{ V}; V_{DS} = 0\text{ V}$	-	4	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 1\text{ A}$	-	12	16	Ω
V_{SD}	Source-drain diode forward voltage	$I_F = 2\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V

DYNAMIC CHARACTERISTICS

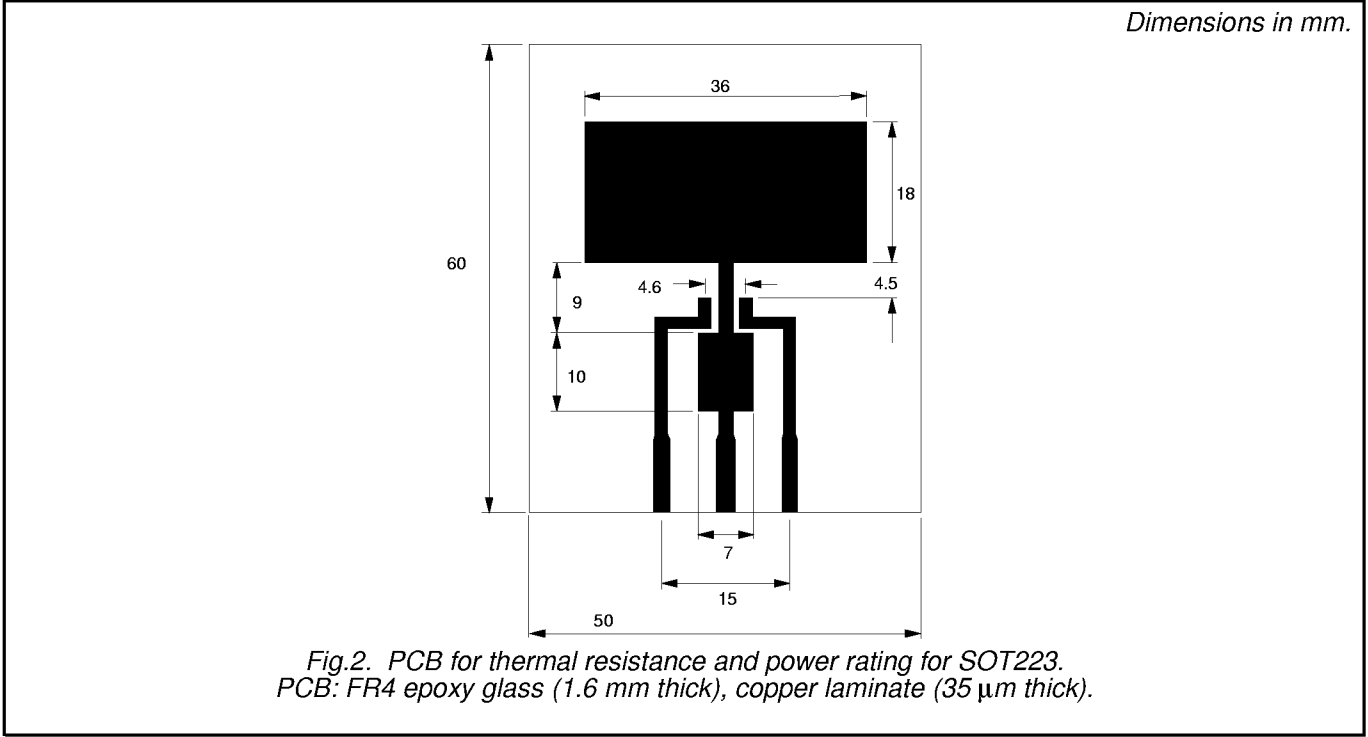
 $T_{mb} = 25\ ^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 15\text{ V}; I_D = 1\text{ A}$	0.5	0.8	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	75	100	pF
C_{oss}	Output capacitance		-	10	15	pF
C_{rss}	Feedback capacitance		-	5	10	pF
$Q_{g(tot)}$	Total gate charge	$V_{GS} = 10\text{ V}; I_D = 2\text{ A}; V_{DS} = 400\text{ V}$	-	5	-	nC
Q_{gs}	Gate to source charge		-	.5	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	3	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 2\text{ A};$	-	5	10	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}; R_{GS} = 50\ \Omega;$	-	15	20	ns
t_{doff}	Turn-off delay time	$R_{GEN} = 50\ \Omega$	-	15	20	ns
t_f	Turn-off fall time		-	7	15	ns
t_{rr}	Source-drain diode Reverse recovery time	$I_F = 2\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	150	-	ns
Q_{rr}	Source-drain diode Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 100\text{ V}$	-	1.5	-	μC

MOUNTING INSTRUCTIONS



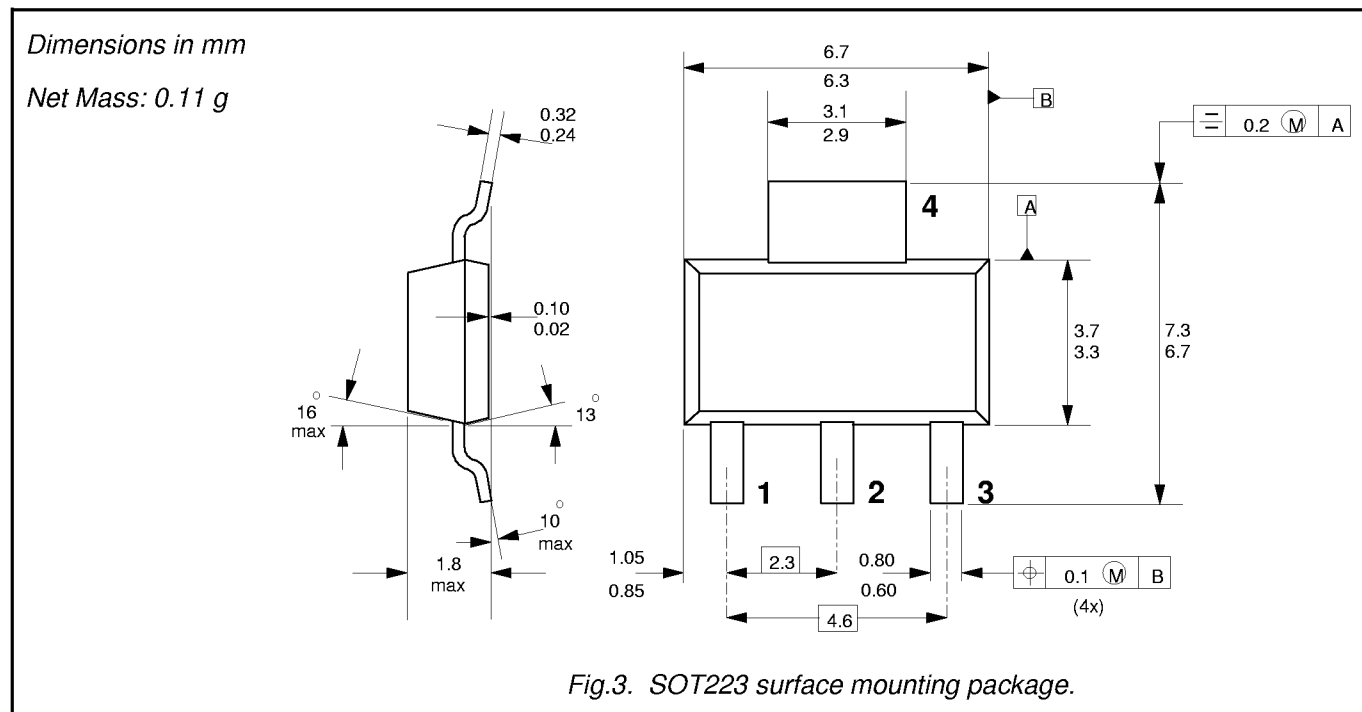
PRINTED CIRCUIT BOARD



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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".