REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R183-93	93-06-11	M. L. Poelking
B	Add device type 02. Incorporate previous NOR revision. Update boilerplate.	93-10-12	M. L. Poelking

REV																			
SHEET																			
REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Thomas M. Hess

CHECKED BY Thomas M. Hess

APPROVED BY Monica L. Poelking

DRAWING APPROVAL DATE
93-05-07

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 32-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92122
A	67268	

SHEET 1 OF 31

DESC FORM 193
JUL 91

5962-E432-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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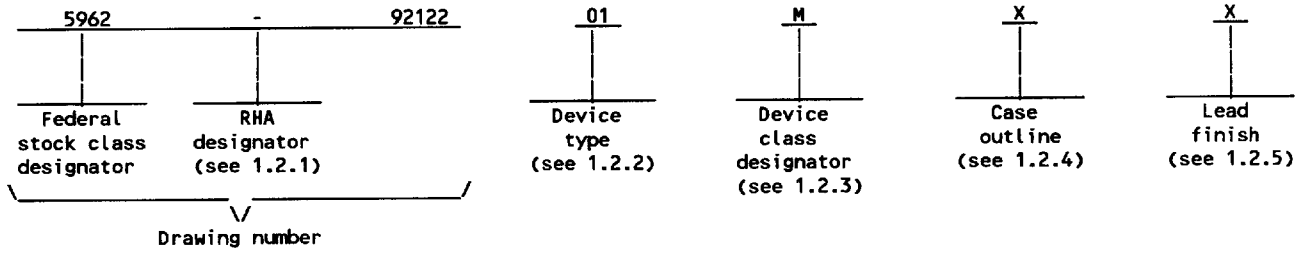
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	49C465A	Flow-thru error detection and correction unit
02	49C465	Flow-thru error detection and correction unit

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7-P144	144	Pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Storage temperature range	-65°C to +150°C
Supply voltage	-0.5 V dc to +7.0 V dc
Terminal voltage with respect to ground	-0.5 V dc to V_{CC} + 0.5 V dc
Maximum power dissipation (PD)	1.5 W
Lead temperature (soldering 10 seconds)	260°C
Thermal resistance, junction-to-case (θJC):	
Case X	See MIL-STD-1835
Maximum junction temperature	150°C

1.4 Recommended operating conditions.

Ambient operating temperature range	-55°C to +125°C
Supply voltage, (V_{CC})	4.5 V dc ≤ V_{CC} ≤ 5.5 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	Normal inputs / Hysteresis inputs	1, 2, 3	All	2.0 / 3.0		V
Input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input high current	I_{IH}	V_{CC} = Max, V_{IN} = V_{CC}	1, 2, 3	All		5.0	µA
Input low current	I_{IL}	V_{CC} = Max, V_{IN} = GND	1, 2, 3	All		-5.0	µA
Off state (HI-Z)	I_{OZ}	V_{CC} = Max; V_O = 0 V / V_O = 3 V	1, 2, 3	All		-10 / 10	µA
Short circuit current	I_{OS}	V_{CC} = Max 2/	1, 2, 3	All	-20	-150	mA
Output high voltage	V_{OH}	V_{CC} = Min , I_{OH}= -4 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = Min, I_{OL} = 4 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All		0.5	V
Quiescent power supply current CMOS input levels	I_{CCQ}	V_{CC} = Max V_{IN} = V_{CC} or GND All inputs, outputs disabled	1, 2, 3	All		5	mA
Quiescent power supply current TTL input levels	I_{CCQT}	V_{IH} = 3.4 V, V_{IL} = 0V V_{CC} = Max, All inputs, outputs disabled	1, 2, 3	All		1	mA/input
Dynamic power supply current f = 10 MHz	I_{CCD1}	f_{CP} = 10 MHz, 50% duty cycle V_{IH} = V_{CC}, V_{IL} = GND Read mode, outputs disabled	4, 5, 6	All		150	mA
Dynamic power supply current f = 20 MHz	I_{CCD2}	f_{CP} = 20 MHz, 50% duty cycle V_{IH} = V_{CC}, V_{IL} = GND Read mode, outputs disabled	4, 5, 6	All		300	mA
Input capacitance	C_{IN}	See 4.4.1.c	4	All		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output capacitance	C_{OUT}	See 4.4.1.c	4	All	-	15	pF
Functional test		See 4.4.1.b	7, 8	All			
BE_N to CBO	t_{BC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- 20 20	ns
BE_N to CBO	t_{BC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		25 --- 25 25	ns
BE_N to MD_{OUT}	t_{BM}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- 20 20	ns
BE_N to MD_{OUT}	t_{BM}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		25 --- 25 25	ns
MD_{IN} to CBO	t_{MC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		--- 18 --- ---	ns
MD_{IN} to CBO	t_{MC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		--- 20 --- ---	ns
PC_{BI} to CBO	t_{PCC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		--- --- --- 18	ns
PC_{BI} to CBO	t_{PCC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		--- --- --- 20	ns
P_{XIN} to $\overline{PERR}$	t_{PPE}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- 18 18	ns
P_{XIN} to $\overline{PERR}$	t_{PPE}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- 20 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SD_{IN} to CBO	t_{SC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01	-	18 18 18 18	ns
SD_{IN} to CBO	t_{SC}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 20 20 20	ns
SD_{IN} to MD_{OUT}	t_{SM}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- 18 18	ns
SD_{IN} to MD_{OUT}	t_{SM}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- 20 20	ns
SD_{IN} to $\overline{PERR}$	t_{SPE}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- 18 18	ns
SD_{IN} to $\overline{PERR}$	t_{SPE}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- 20 20	ns
CBI to $\overline{ERR}$(L)	t_{CE}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- --- 18	ns
CBI to $\overline{ERR}$(L)	t_{CE}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- --- 20	ns
CBI to $\overline{MERR}$(L)	t_{CME}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- --- 20	ns
CBI to $\overline{MERR}$(L)	t_{CME}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		24 --- --- 24	ns
CBI to SYO	t_{CSY}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- 18 18	ns
CBI to SYO	t_{CSY}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- 18 ---	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics = Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MD_{IN} to $\overline{ERR}$	t_{ME}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01	-	18 --- --- 18	ns
MD_{IN} to $\overline{ERR}$	t_{ME}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- --- ---	ns
MD_{IN} to $\overline{MERR}$	t_{MME}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- --- 20	ns
MD_{IN} to $\overline{MERR}$	t_{MME}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		24 --- --- 24	ns
MD_{IN} to SYO	t_{MSY}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- 18 18	ns
MD_{IN} to SYO	t_{MSY}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- 20 20	ns
CBI to SD_{OUT}	t_{CS}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- --- 20	ns
CBI to SD_{OUT}	t_{CS}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		24 --- --- 24	ns
MD_{IN} to P_X	t_{MP}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		22 --- 22 22	ns
MD_{IN} to P_X	t_{MP}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		26 --- 26 26	ns
MD_{IN} to SD_{OUT}	t_{MS}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		18 --- --- ---	ns
MD_{IN} to SD_{OUT}	t_{MS}	Code ID = 00 See figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		20 --- --- ---	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics = Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MD_{IN} to SYO	t_{MSY}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- 18 18	ns
MD_{IN} to SYO	t_{MSY}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		22 --- 20 20	ns
PCBI to SD_{OUT}	t_{PCS}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		--- --- 18 ---	ns
PCBI to SD_{OUT}	t_{PCS}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		--- --- 20 ---	ns
CLEAR(L) to SD_{OUT}	t_{CLR}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- 20 20	ns
CLEAR(L) to SD_{OUT}	t_{CLR}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		24 --- 24 24	ns
MODE ID to SD_{OUT}	t_{MIS}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	01		20 --- 20 20	ns
MODE ID to SD_{OUT}	t_{MIS}	Code ID = 00 see figure 3 Code ID = 01 V_{CC} = 4.5 V Code ID = 10 Code ID = 11	9,10,11	02		24 --- 24 24	ns
MLE(H) to CBO	t_{MLC}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		20 24	ns
MLE(H) to $\overline{ERR}$	t_{MLE}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		18 20	ns
MLE(H) to $\overline{MERR}$	t_{MLME}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		20 24	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics = Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MLE(H) to P_X	t_{MLP}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		22 25	ns
MLE(H) to SD_{OUT}	t_{MLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		22 25	ns
MLE(H) to SYO	t_{MLSY}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		20 22	ns
$\overline{PLE}$(L) to SD_{OUT}	t_{PLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		12 16	ns
$\overline{PLE}$(L) to P_X	t_{PLP}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		18 20	ns
SLE(H) to CBO	t_{SLC}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		20 24	ns
SLE(H) to MD_{OUT}	t_{SLM}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02		18 20	ns
BEN(H) to SD_{OUT}	t_{BESZx}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	16 18	ns
BEN(L) to SD_{OUT}(Hi-Z)	t_{BESxZ}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	14 16	ns
BEN(H) to P_{OUT}	t_{BEPZx}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	16 18	ns
BEN(L) to P_{OUT}(Hi-Z)	t_{BEPxZ}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	14 16	ns
$\overline{CBOE}$(L) to CBO	t_{CECZx}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	16 18	ns
$\overline{CBOE}$(H) to CBO(Hi-Z)	t_{CECxZ}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	14 16	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics = Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{MOE}$(L) to MD_{OUT}	t_{MEMZx}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	16 18	ns
$\overline{MOE}$(H) to MD_{OUT}(Hi-Z)	t_{MEMxZ}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	14 16	ns
$\overline{SOE}$(L) to SD_{OUT}	t_{SESZx}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	16 18	ns
$\overline{SOE}$(H) to SD_{OUT}(Hi-Z)	t_{SESxZ}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	2 2	14 16	ns
SDIN setup to before SLE(L)	t_{SSLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
SDIN hold to after SLE(L)	t_{SSLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
MDIN setup to before MLE(L)	t_{MMLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
MDIN hold to after MLE(L)	t_{MMLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
CBI setup to before MLE(L)	t_{CMLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
CBI hold to after MLE(L)	t_{CMLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
MDIN setup to before $\overline{PLE}$(H)	t_{MPLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	12 15		ns
MDIN hold to after $\overline{PLE}$(H)	t_{MPLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	All	0		ns
CBI setup to before $\overline{PLE}$(H)	t_{CPLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	12 15		ns

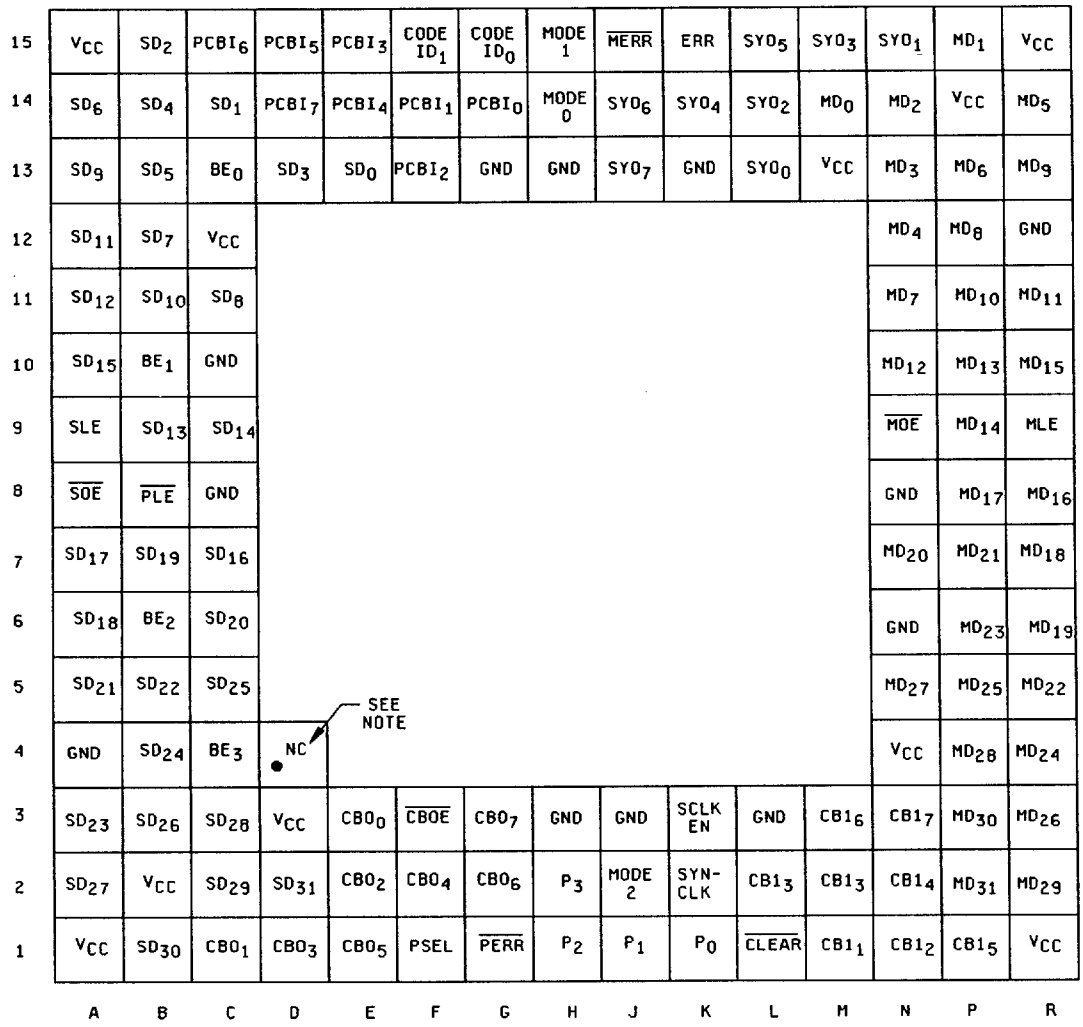
See footnotes at end of table.

TABLE I. Electrical performance characteristics = Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CBI hold to after $\overline{PLE}$(H)	t_{CPLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	All	0		ns
PCBI setup to before $\overline{PLE}$(H)	t_{PCPLS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	12 15		ns
PCBI hold to after $\overline{PLE}$(H)	t_{PCPLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	All	0		ns
CBI setup to before SYNCLK(H)	t_{CSCS}	V_{CC} = 4.5 V See figure 3	9,10,11	01 02	12 15		ns
MDIN setup before SYNCLK(H)	t_{MSCS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	12 15		ns
MLE setup(H) before SYNCLK(H)	t_{MLSCS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	12 15		ns
SCLKEN setup(L) to before SYNCLK(H)	t_{SESCS}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
SCLKEN hold(L) to after SYNCLK(H)	t_{SESCH}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02	4 5		ns
Min $\overline{CLEAR}$ low time to clear diag. registers	t_{CLEAR}	Data = valid See figure 3 V_{CC} = 4.5 V	9,10,11	All	10		ns
Min MLE high time to strobe new data	t_{MLE}	MD, CBI = valid see figure 3 V_{CC} = 4.5 V	9,10,11	All	6		ns
Min $\overline{PLE}$ low time to strobe new data	t_{PLE}	SD = Valid See figure 3 V_{CC} = 4.5 V	9,10,11	All	6		ns
Min SLE high time to strobe new data	t_{SLE}	SD = Valid See figure 3 V_{CC} = 4.5 V	9,10,11	All	6		ns
Min SYNCLK high time to clock in new data	t_{SYNCLK}	SCKEN = low See figure 3 V_{CC} = 4.5 V	9,10,11	All	6		ns

1/ All testing to be performed using worst-case test conditions. Dashed lines in limits column indicates that a test is not applicable.
2/ Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 1 s.

Case X



NOTE: TIED TO V_{CC} INTERNALLY.

FIGURE 1. Terminal connections.

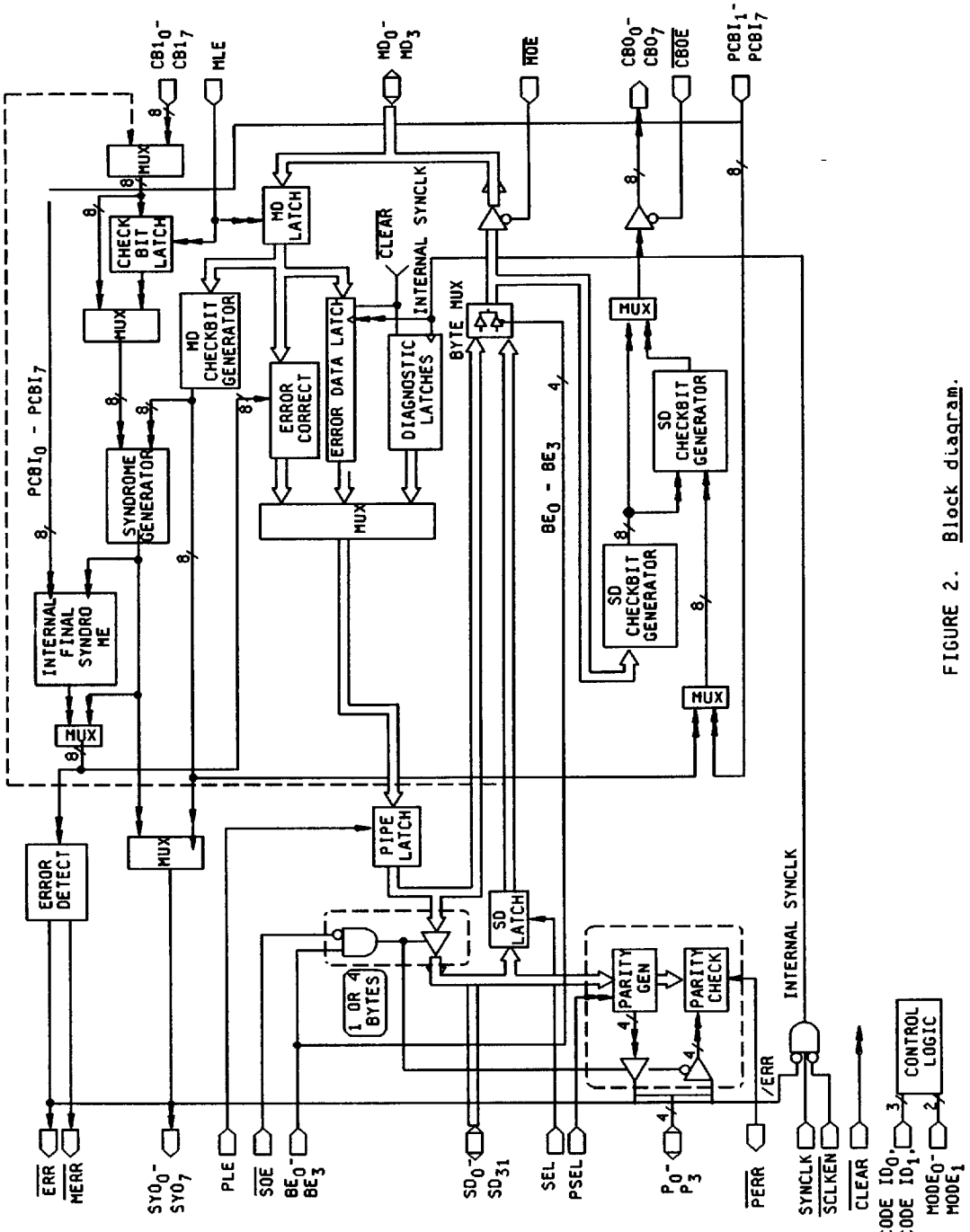
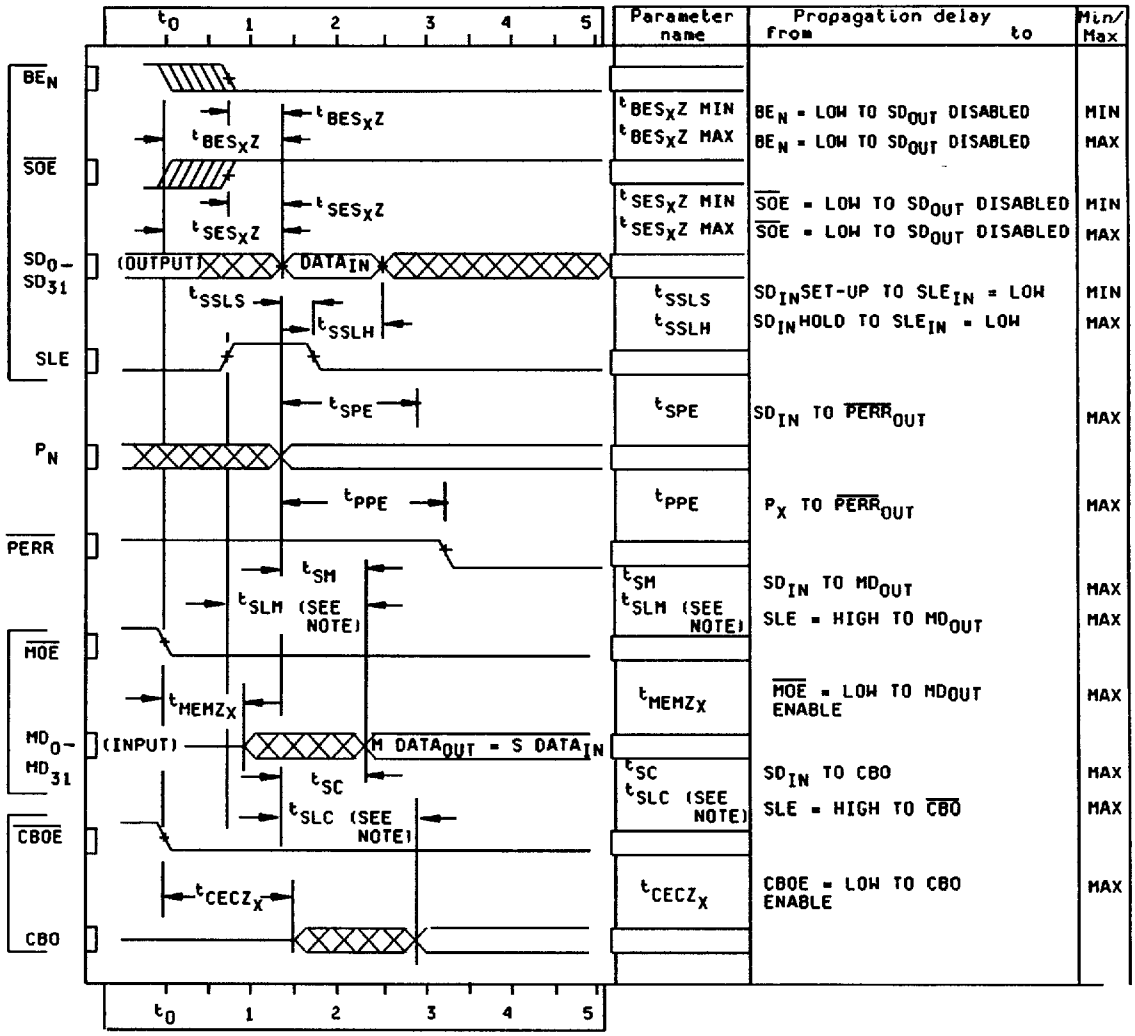


FIGURE 2. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92122
		REVISION LEVEL B	SHEET 14

DESC FORM 193A
JUL 91

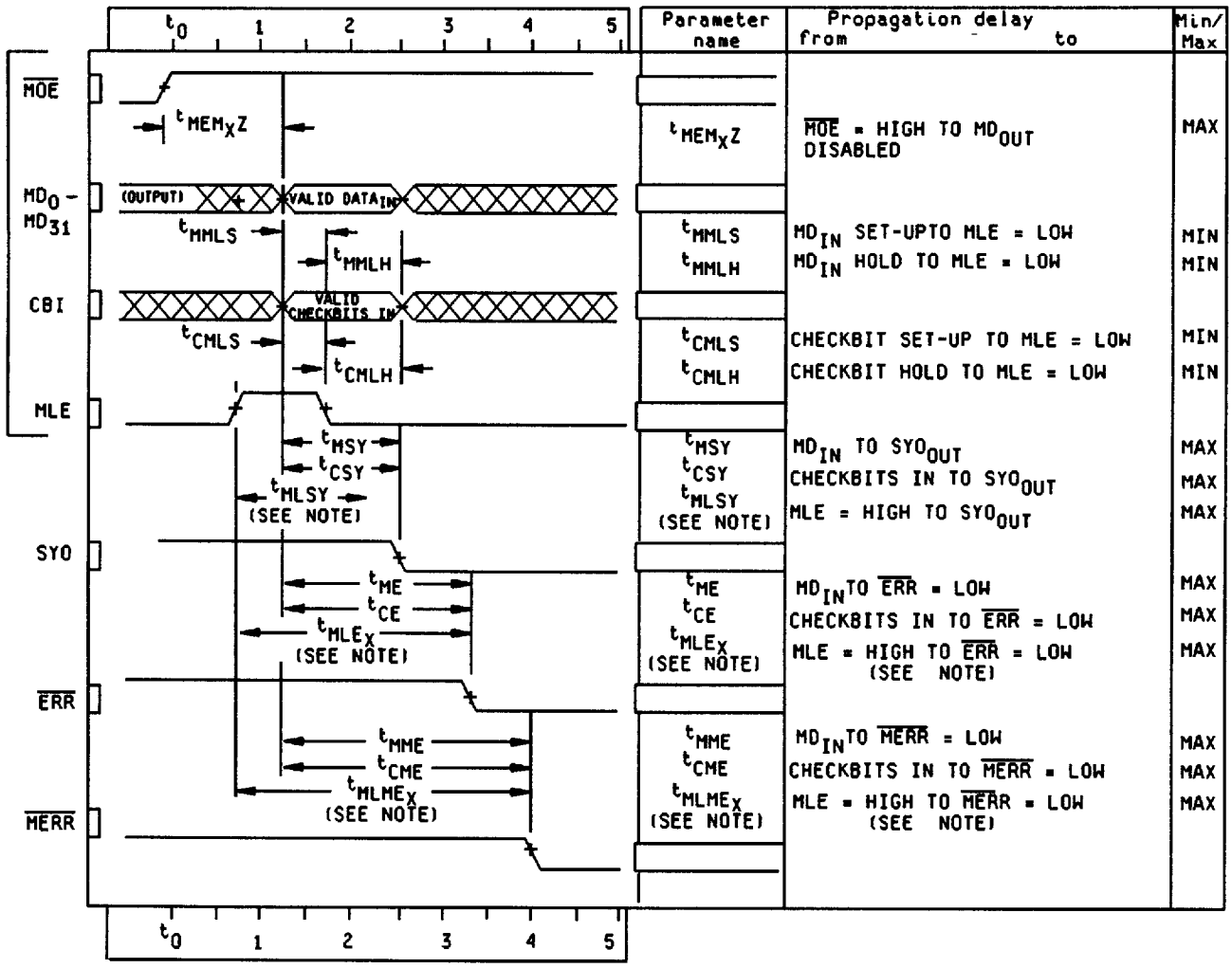
9004708 0005426 TT8



32-Bit Configuration

Note:
Assumes that system data is valid at least 4 ns before SLE goes high

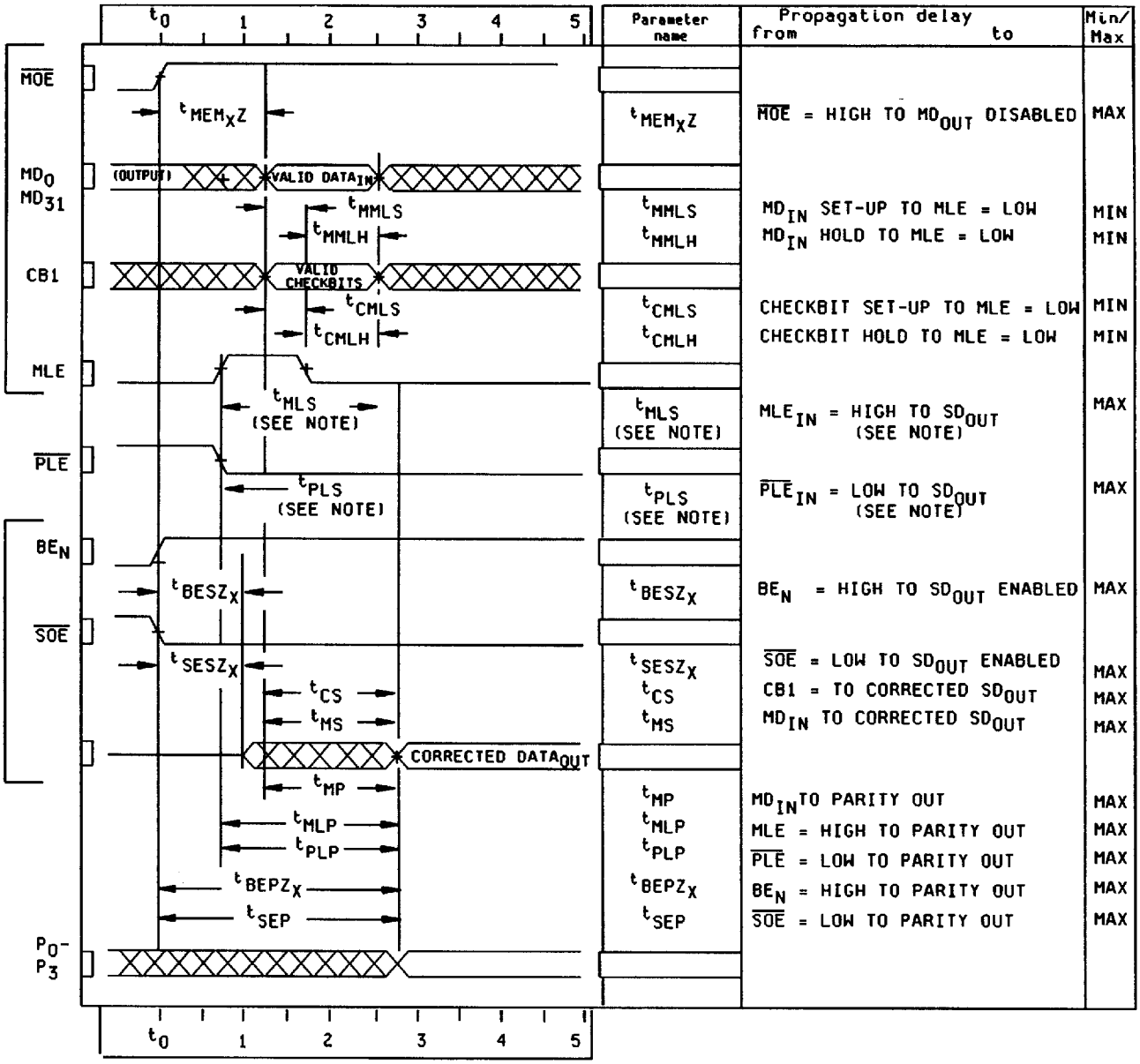
FIGURE 3. Timing waveforms.



32-Bit Configuration

Note:
Assumes that memory data and checkbits are valid at least 4 ns before MLE goes high.

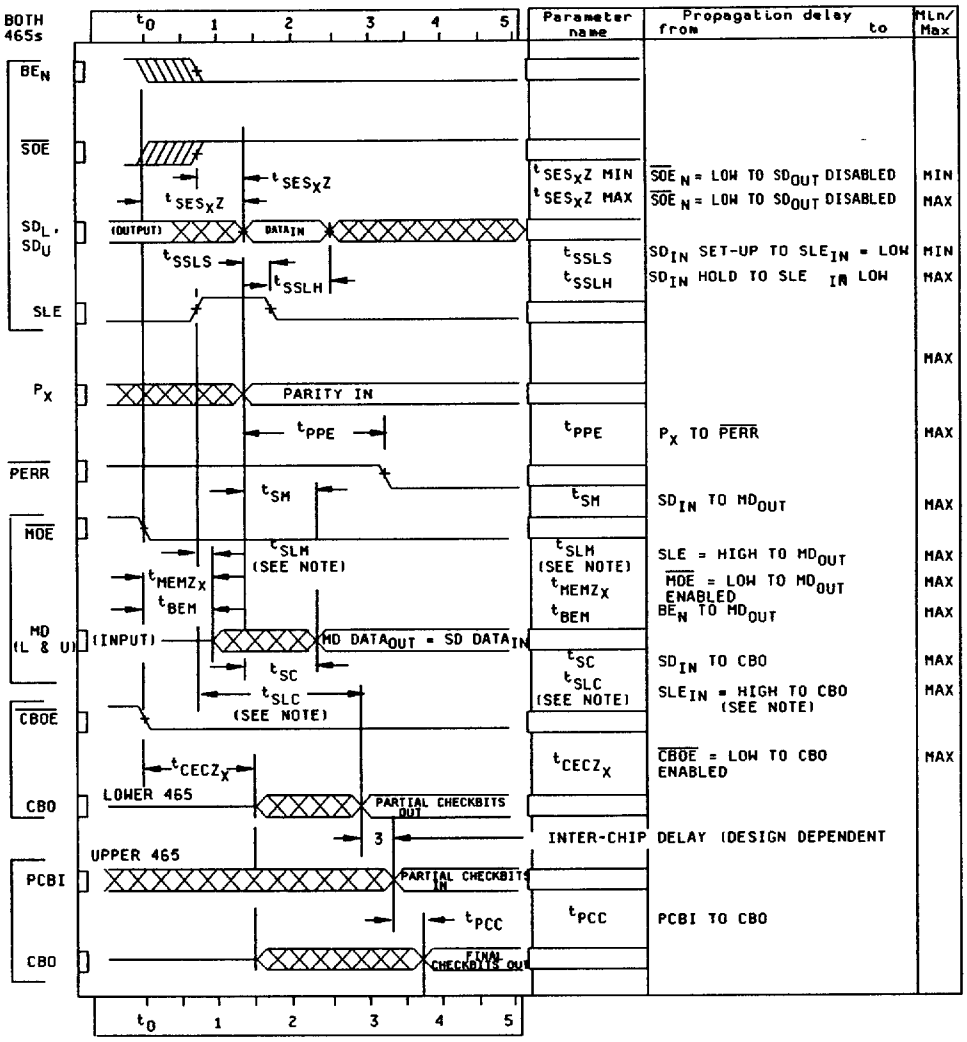
FIGURE 3. Timing waveforms - Continued.



32-Bit Configuration

Note:
Assumes that memory data and checkbits are valid at least 4 ns before MLE goes high

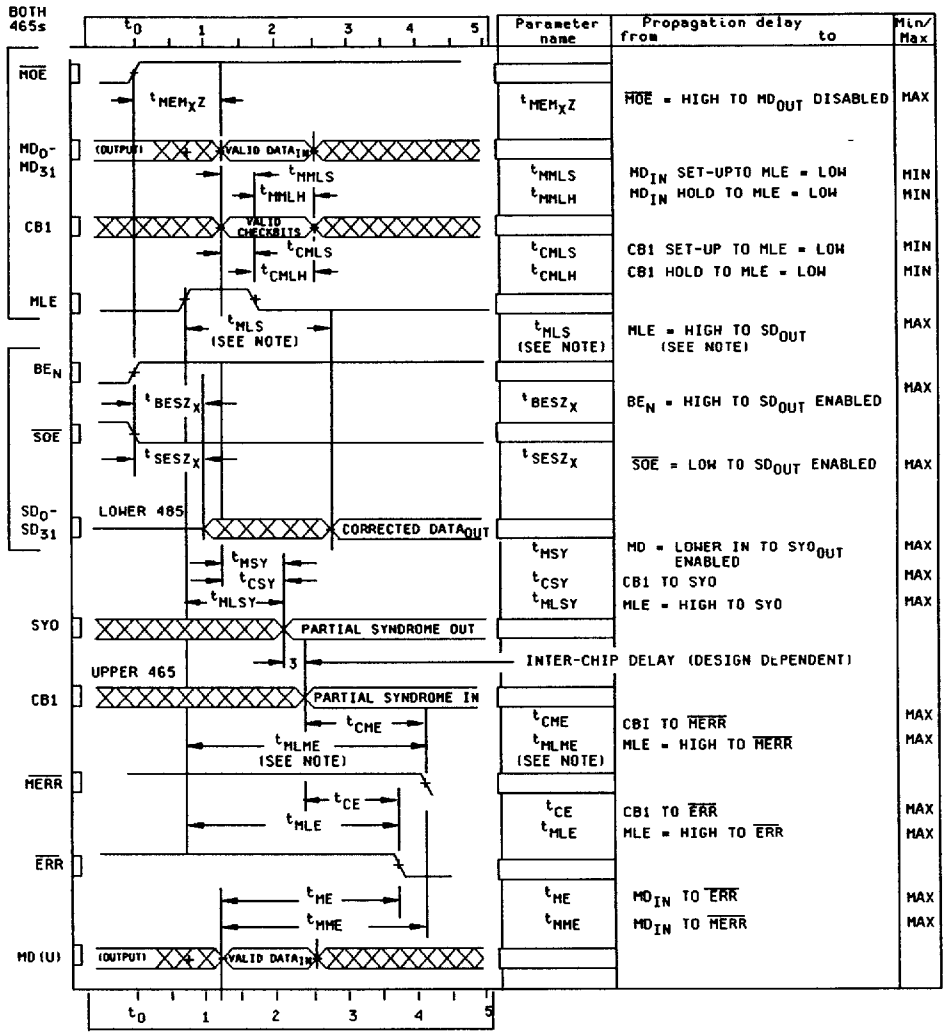
FIGURE 3. Timing waveforms - Continued.



64-Bit Configuration

Note:
Assumes that system data is valid at least 4 ns before SLE goes high

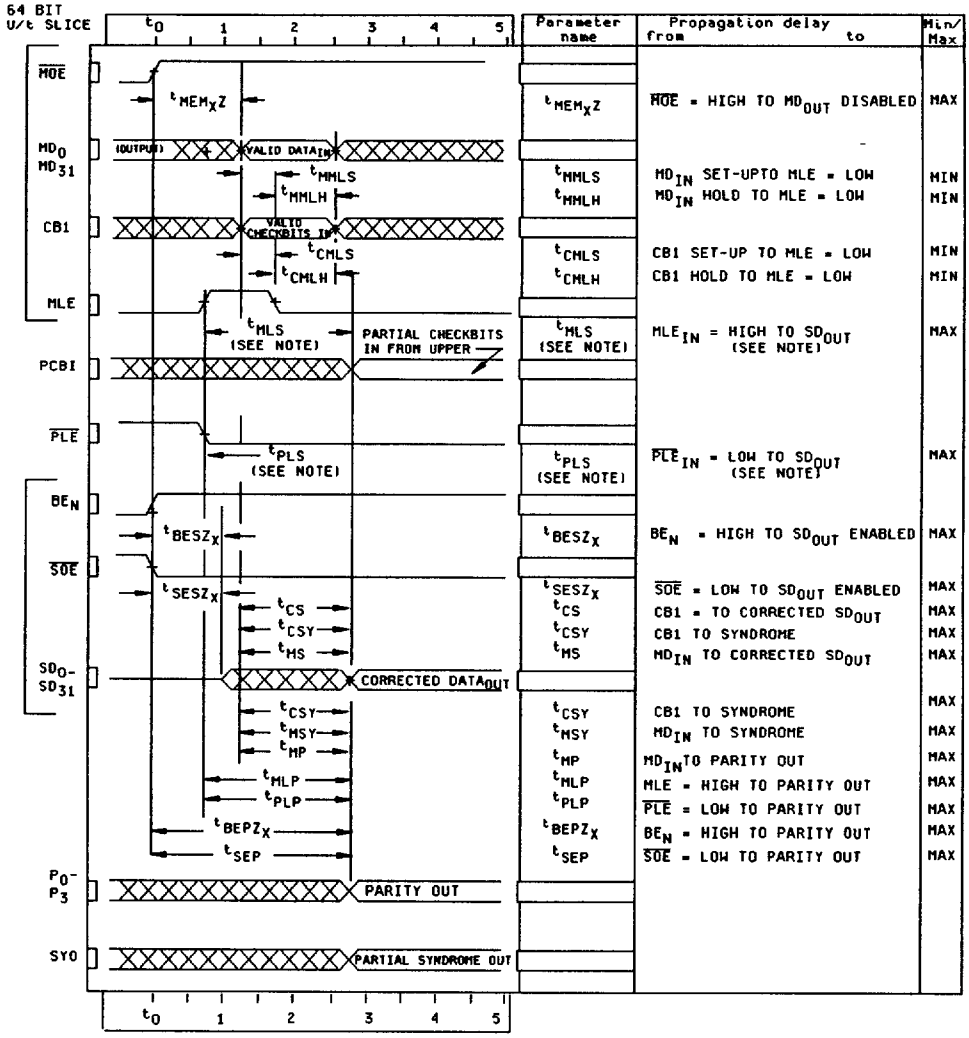
FIGURE 3. Timing waveforms - Continued.



64-Bit Configuration

Note: Assumes that system data is valid at least 4 ns before SLE goes high

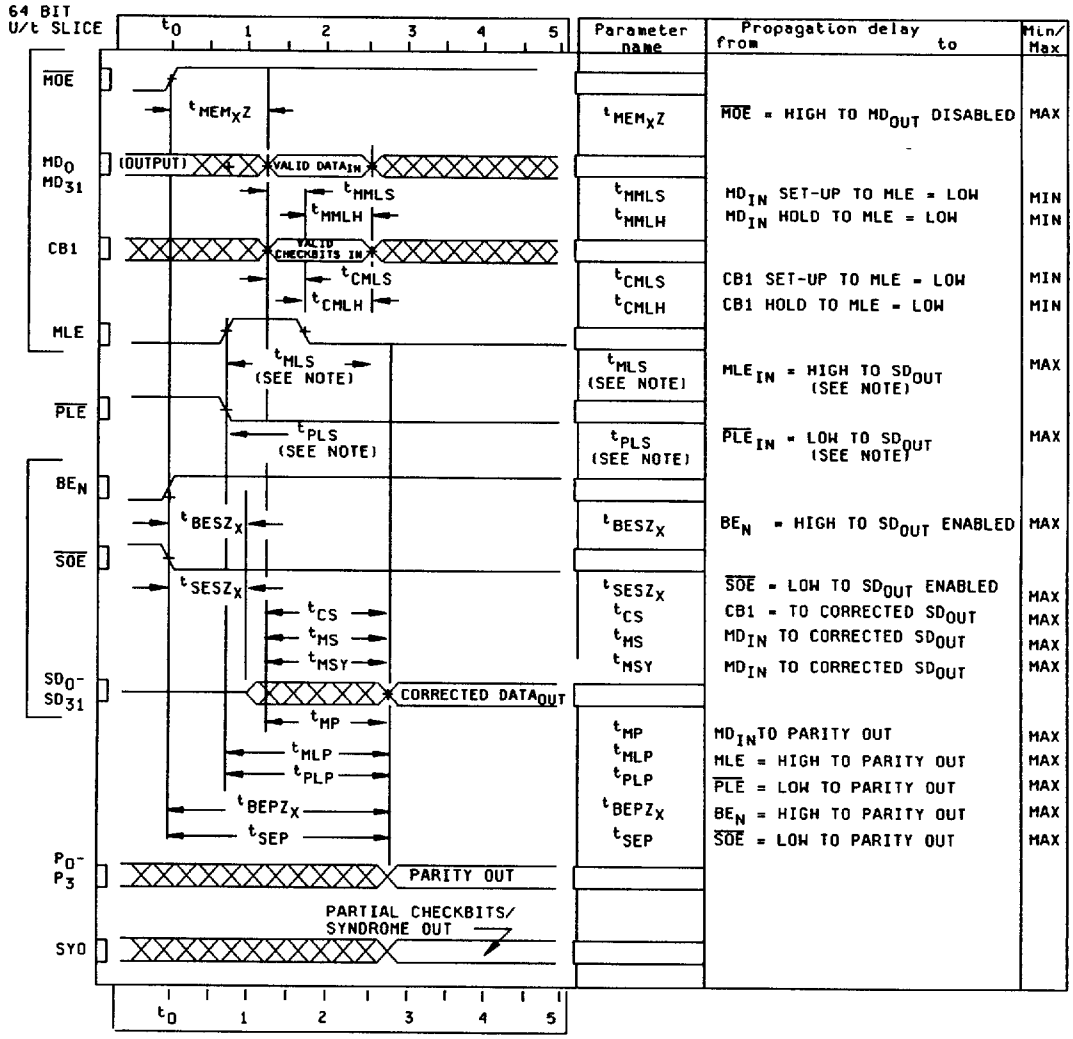
FIGURE 3. Timing waveforms - Continued.



64-Bit Configuration

Note:
Assumes that memory data and checkbits are valid at least 4 ns before MLE goes high

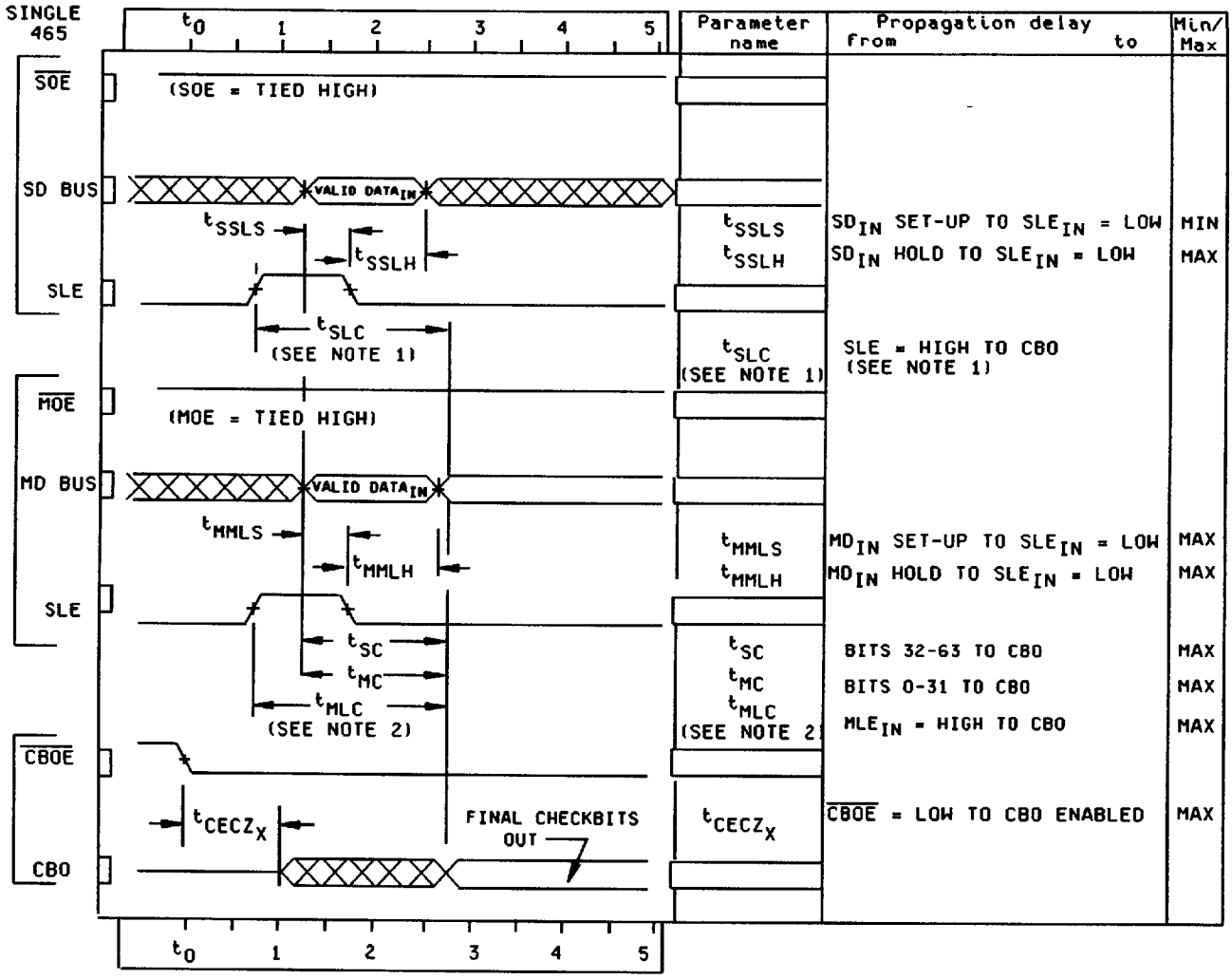
FIGURE 3. Timing waveforms - Continued.



64-Bit Configuration

Note:
Assumes that memory data and checkbits are valid at least 4 ns before MLE goes high

FIGURE 3. Timing waveforms - Continued.



64-Bit Configuration

Note:
1. Assumes that system data is valid at least 4 ns before SLE goes high
2. Assumes that memory data is valid at least 4 ns before MLE goes high.

FIGURE 3. Timing waveforms - Continued.

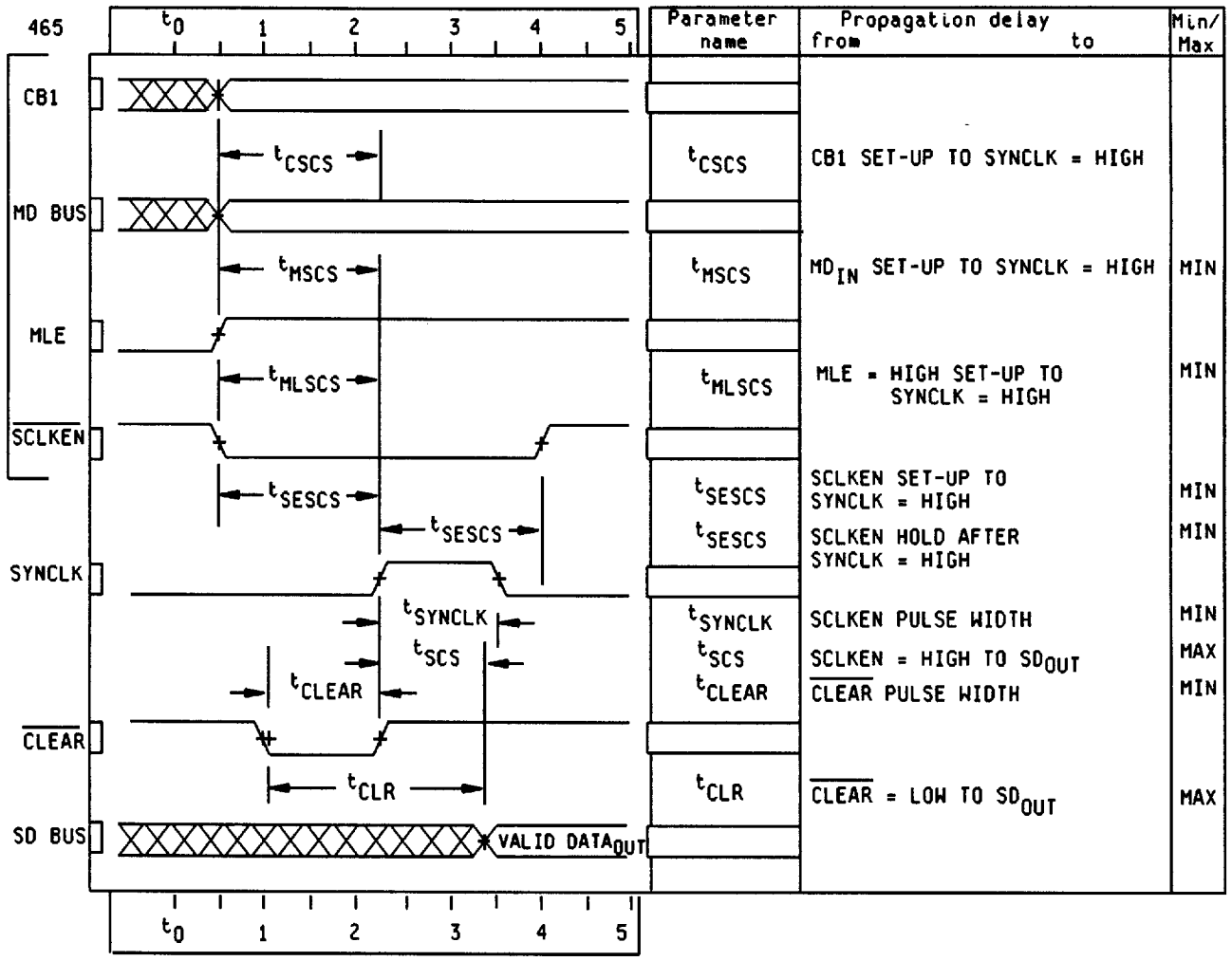
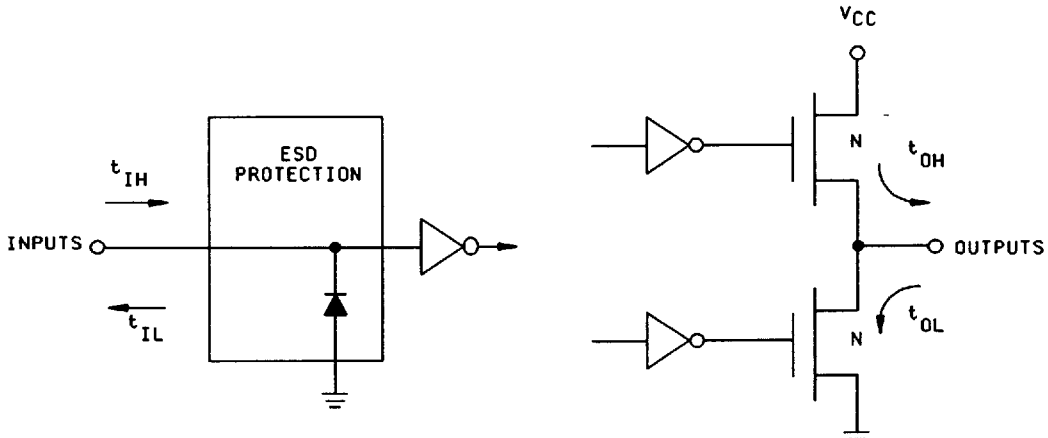


FIGURE 3. Timing waveforms - Continued.

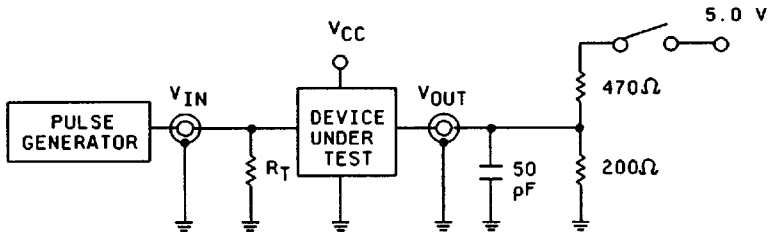
INPUT/OUTPUT INTERFACE CIRCUITS



INPUT STRUCTURE
(ALL INPUTS)

OUTPUT STRUCTURE

AC TEST CIRCUIT



Test	Switch
Disable low Enable low	Closed Closed
All other tests	Open

R_T = Termination resistance: should be equal to Z_{OUT} of the pulse generator.

FIGURE 3. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4(C_{IN} and C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1,2,3, 7,8,9 1/ 10,11	1,2,3, 7,8,9 1/ 10,11	1,2,3, 7,8,92/ 10,11	1,2,3, 7,8,9 1/ 10,11	1,2,3, 7,8,9 2/ 10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9 10,11	1,2,3,4, 7,8,9 10,11	1,2,3,4, 7,8,9 10,11	1,2,3,4, 7,8,9 10,11	1,2,3,4, 7,8,9 10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9		1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	---	---	---	---	---

1/ PDA applies to subgroup 1 and 4 (i.e., I_{CCD1}, I_{CCD2} only)
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

TABLE III. Pin descriptions.

Symbol	I/O		Name and Function
Outputs and enables			
CBO_{0-7}	O		**Checkbits-out** (00, 01) Partial-checkbits-out (10) Checkbits-out (11): In a single EDC system, the checkbits are output to the checkbit memory on these outputs. In the lower slice in a cascaded EDC system, the "partial-checkbits" used by the upper slice are output by these outputs (generate path only.) In the upper slice in a cascade, the "final-checkbits: appear at these outputs (generate path only.)
$\overline{CBOE}$	I		**Checkbits Out Enable:** Enables checkbit output drivers when low.
SYO_{0-7}	O		**Syndrome-Out** (00) Partial-Syndrome-Out (10) Partial-Checkbits-Out (11): In a 32-bit EDC system, the syndrome bits are output on these pins. In the lower slice in a 64-bit cascaded system, the "Partial-Syndrome" bits appear at these outputs (detect/correct path.) In the upper slice in a cascaded EDC system, the "Partial-Checkbits" appear at these outputs (correct path only.) In a 64-bit cascaded system, the "Final-Syndrome" may be accessed in the "Diagnostic-Output" mode from either the lower or the upper slice since the final syndrome is contained in both.
$\overline{ERR}$	O		**Error:** When in "normal" and "detect only" modes, a low on this pin indicates that one or more errors have been detected. ERR is not gated or latched internally.
$\overline{MERR}$	O		**Multiple Error:** When in "normal" and "detect only" modes, a low on this pin indicates that two or more errors have been detected. MERR is not gated or latched internally.
$\overline{PERR}$	O		**Parity Error:** A low on this pin indicates a parity error which has resulted from the active bytes defined by the 4 Byte Enable pins. Parity Error (PERR) is not gated or latched internally (see byte Enable definition.)
Power supply pins			
$V_{CC\ 1-10}$	P		+5 Volts
GND_{1-12}	P		Ground

Symbol	I/O		Name and Function
I/O buses and controls			
SD_{0-7} SD_{8-15} SD_{16-23} SD_{24-31}	I/O		**System data bus:** Data from MD_{0-31} appears at these pins corrected if MODE 2-0 = x11, or uncorrected in the other modes. The BE_n inputs must be high and the $\overline{SOE}$ pin must be low to enable the SD output buffers during a read cycle. **Separate I/O memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is output on SD_n to n+7 for re-writing to memory, if BE_n is high and $\overline{SOE}$ is low. The new bytes to be written to memory are input on the SD_n pins, for writing checkbits to memory, if BE_n is low. **Bi-directional memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is re-directed to the MD I/O pins, if BE_n is high, for checkbit generation and rewriting to memory via the MD I/O pins. $\overline{SOE}$ must be high to avoid enabling the output drivers to the system bus in this mode. The new bytes to be written are input on the SD_n pins for checkbit generation and writing to memory. BE_n must be low to direct input data from the system data bus to the MD I/O pins for checkbit generation and writing to the checkbit memory.
SLE	I		**System latch enable:** SLE is an input used to latch data at the SD inputs. The latch is transparent when SLE is high; the data is latched when SLE is low.
$\overline{PLE}$	I		**Pipeline latch enable:** $\overline{PLE}$ is an input which controls a pipeline latch, which in turn controls data to be output on the SD bus and the MD bus during byte merges. Use of this latch is optional. The latch is transparent when PLE is low; the data is latched when PLE is high.
$\overline{SOE}$	I		**System output enable:** When low, enables system output drivers and parity output drivers if corresponding byte enable inputs are high.
BE_{0-3}	I		**Byte enables:** In systems using separate I/O memory buses, BE_n is used to enable the SD and parity outputs for byte n. The BE_n pins also control the "byte mux." When BE_n is high, the corrected or uncorrected data from the memory data latch is directed to the MD I/O pins and used for checkbit generation for byte n. This is used in partial-word-write operations or during correction cycles. When BE_n is low, the data from the system data latch is directed to the MD I/O pins and used for checkbit generation for byte n. BE_0 controls SD_{0-7} BE_2 controls SD_{16-23} BE_1 controls SD_{8-15} BE_3 controls SD_{24-31}
MD_{0-31}	I/O		**Memory data bus:** These I/O pins accept a 32-bit data word from main memory for error detection and/or correction. They also output corrected old data or new data to be written to main memory when the EDC unit used in a bi-direction configuration.
MLE	I		**Memory latch enable:** MLE is used to latch data from the MD inputs and checkbits from the CBI inputs. The latch is transparent when MLE is high; data is latched when MLE is low. when identified as the upper slice in a 64-bit cascade, the checkbit latch is bypassed.
$\overline{MOE}$	I		**Memory output enable:** $\overline{MOE}$ enable memory data bus output drivers when low.
P_{0-3}	I/O		**Parity I/O:** The parity I/O pins for bytes 0 to 3. These pins output the parity of their respective bytes when that byte is being output on the SD bus. These pins also serve as parity inputs and are used in generating the parity error ($\overline{PERR}$) signal under certain conditions (see Byte enable definition.) The parity is odd or even depending on the state of the parity select pin (PSEL.)
PSEL	I		**Parity select:** If the parity select pin is low, the parity is even. If the parity select pin is high, the parity is odd.
Inputs			
CBI_{0-7}	I		**Checkbits-in (00) Checkbits-in-1 (10) Partial-syndrome-in (11):** In a single EDC system or in the lower slice of a cascaded EDC system, these inputs accept the checkbits from the checkbit memory. In the upper slice in a cascaded EDC system, these inputs accept the "partial-syndrome" from the lower slice (Detect/correct path.)

Symbol	I/O		Name and Function
Inputs (cont.)			
$PCBI_{0-7}$	I		**Partial-checkbits-in (10) Partial-checkbits-in (11):** In a single EDC system, these inputs are unused but should not abe allowed to float. IN a cascaded EDC system, the "partial-checkbits" used by the lower slice are accepted by these inputs (correction path only.) In the upper slice of a cascaded EDC system, "partial-checkbits" generated by the lower slice are accepted by these inputs (generate path.)
CODE $ID_{1,0}$	I		**CODE identity:** Inputs which identify the slice position/functional mode of the device. (00) Single 32-bit EDC unit (10) Lower slice of a 64-bit cascade (01) 64-bit "checkbit-generate-only" unit (11) Upper slice of a 64-bit cascade
$MODE_{2-0}$	I		**Mode select:** Selects one of four operating modes.
		x11	**"Normal" mode:** Normal EDC operation (flow-through correction and generation.)
		x10	**"Generate-detect" mode:** In this mode, error correction is disabled. Error generation and detection are normal.
		000	**"Error-data-output" mode:** Allows the uncorrected data captured from an error event by the error-data register to be read by the system for diagnostic purposes. the error-data register is cleared by toggling CLEAR low. The syndrome register and error-data register record the syndrome and uncorrected data from the first error that occurs after they are reset by the CLEAR pin. The syndrome register and error-data register are updated when there is a positive edge on SYNCLK, an error condition is indicated (ERR = low), and the error counter indicates zero. **All-zero-data source:** In error-data-output mode clearing the error-data register provides a source of all-zero-data for hardware initialization of memory, if this is desired.
		x01	**Diagnostic-output mode:** In this mode, the contents of the syndrome register, error counter, and error-type register are output on the SD bus. This allows the syndrome bytes for an indicated error to be read by the system for error-logging purposes. The syndrome register and the error-data register are updated when there is a positive edge on SYNCLK, and error condition is indicated and the error counter indicates zero errors. Thus, the syndrome Register saves the syndrome that was present when the fist error occurred after the Error Counter was cleared. The Syndrome Register and the Error Counter are cleared by toggling CLEAR low. the Error Counter lets the system tell if more than one error has occurred since the last time the Syndrome Register or Error-Data Register was read.
		100	**Checkbit-injection mode:** In the "checkbit-injection" mode, diagnostic checkbits may be input on System Data Bus bits 0-7.
$\overline{CLEAR}$	I		**Clear:** When the $\overline{CLEAR}$ pin is taken low, the Error-Data Register, the Syndrome Register, the Error Counter, and the Error-Type Register are cleared.
SYNCLK	I		**Syndrome clock:** If $\overline{ERR}$ is low, and the Error Counter indicates zero errors, syndrome bits are clocked into the Syndrome Register and data from the outputs of the Memory Data input latch are clocked in to the Error-Data Register on the low-to-high edge of SYNCLK. If $\overline{ERR}$ is low, the Error Counter will increment on the low-to-high edge of SYNCLK, unless the Error Counter indicates fifteen errors.
$\overline{SCLKEN}$	I		**Synclk enable:** The $\overline{SCLKEN}$ enables the SYNCLK signal. SYNCLK is ignored if $\overline{SCLKEN}$ is high.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.