REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thanh V. Nguyen

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
97-03-18

REVISION LEVEL

DEFENSE SUPPLY CENTER, COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, SCAN PATH SELECTOR WITH 8-BIT BIDIRECTIONAL DATA BUS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96747

SHEET 1 OF 31

DESC FORM 193
JUL 94

5962-E327-96

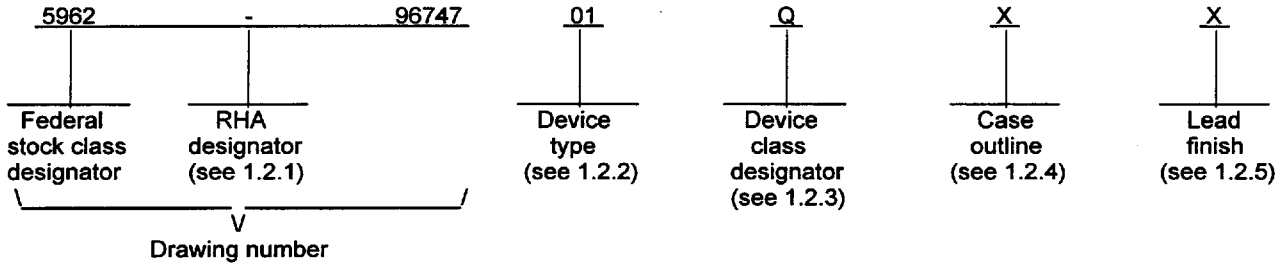
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0028065 692

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT8999	Scan path selector with 8-bit bidirectional data bus, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The cases outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP4-T28	28	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} +0.5 V dc 4/
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V or V_I > V_{CC})	±20 mA
DC output clamp current (I_{OK})(V_{IN} < 0.0 V or V_I > V_{CC})	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	85 mW 5/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	+0.8 V
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum high level output current (I_{OH}):	
ID (1-8)	-1.6 mA
TDO, DTDO, MCO	-8.5 mA
DTMS (1-4), DCO (three-state), DTRST, DTCK	-13.6 mA
Maximum low level output current (I_{OL}):	
ID (1-8)	+1.6 mA
TDO, DTDO, MCO	+8.5 mA
DTMS (1-4), DCO (three-state or open drain)	+13.6 mA
DTRST	+20.4 mA
DTCK	+40.8 mA
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C. Unused inputs must be held high or low.

4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.

5/ Power dissipation values are derived using the formula $P_D = V_{CC}I_{CC} + \sum_{x=1}^{n} V_{OL}I_{OLx}$ where V_{CC} and I_{OL} are as specified in 1.4 above, I_{CC} and V_{OL} are as specified in table I herein, and n represents the total number of outputs.

6/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Test access port controller and scan test registers The test access port (TAP) controller and scan test registers shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage, IDn 3006	V_{OH1}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V	I_{OH} = -1.6 mA	4.5 V	1, 2, 3	3.7		V
High level output voltage, TDO, DTDO, MCO 3006	V_{OH2}		I_{OH} = -8.5 mA	4.5 V	1, 2, 3	3.7		
High level output voltage, DTMSm, DCO (three-state), DTRST, DTCK 3006	V_{OH3}		I_{OH} = -13.6 mA	4.5 V	1, 2, 3	3.7		
Low level output voltage, IDn 3007	V_{OL1}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V	I_{OL} = 1.6 mA	4.5 V	1, 2, 3		0.5	V
Low level output voltage, TDO, DTDO, MCO 3007	V_{OL2}		I_{OL} = 8.5 mA	4.5 V	1, 2, 3		0.5	
Low level output voltage, DTMSm, DCO (three-state or open drain) 3007	V_{OL3}		I_{OL} = 13.6 mA	4.5 V	1, 2, 3		0.5	
Low level output voltage, DTRST 3007	V_{OL4}		I_{OL} = 20.4 mA	4.5 V	1, 2, 3		0.5	
Low level output voltage, DTCK 3007	V_{OL5}		I_{OL} = 40.8 mA	4.5 V	1, 2, 3		0.5	
Three-state output leakage current high, IDn, DTDO, DTMSm, DCO, DTCK 3021	I_{OZH} 4/	For control input affecting output under test, V_{IN} = 2.0 V or 0.8 V $V_{OUT} = V_{CC}$		5.5 V	1, 2, 3		+10.0	µA
Three-state output leakage current low, IDn, DTDO, DTMSm, DCO, DTCK 3020	I_{OZL} 4/	For control input affecting output under test, V_{IN} = 2.0 V or 0.8 V V_{OUT} = GND		5.5 V	1, 2, 3		-10.0	µA
Output current high, DCO (open drain)	I_{OH}	$V_{OUT} = V_{CC}$		5.5 V	1, 2, 3		20.0	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input current high, MCI, DCI, TCK 3010	I_{IH1}	For input under test, $V_{IN} = V_{CC}$		5.5 V	1, 2, 3		+1.0	µA
Input current high, TDI, DTDI, TMS, OTMS, TRST 3010	I_{IH2}	For input under test, $V_{IN} = V_{CC}$		5.5 V	1, 2, 3		+1.0	µA
Input current low, MCI, DCI, TCK 3009	I_{IL1}	For input under test, V_{IN} = GND		5.5 V	1, 2, 3		-1.0	µA
Input current low, TDI, DTDI, TMS, OTMS, TRST 3009	I_{IL2}	For input under test, V_{IN} = GND		5.5 V	1, 2, 3	-0.1	-20.0	µA
Quiescent supply current 3005	I_{CC}	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0 A		5.5 V	1, 2, 3		100.0	µA
Quiescent supply current delta, TTL input level 3005	ΔI_{CC} 5/	For input under test, V_{IN} = 3.4 V For all other inputs, $V_{IN} = V_{CC}$ or GND		5.5 V	1, 2, 3		1.0	mA
Input capacitance 3012	C_{IN}	T_C = +25°C See 4.4.1c		5.0 V	4		5.0	pF
Output capacitance 3012	C_{OUT}	T_C = +25°C See 4.4.1c		5.0 V	4		8.0	pF
Functional test 3014	6/	V_{IH} = 2.0 V, V_{IL} = 0.8 V Verify output V_O See 4.4.1b		4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Clock frequency	f_{clk}	C_L = 50 pF minimum R_L = 500Ω See figure 5	TCK	4.5 V and 5.5 V	9, 10, 11	0	20	MHz
			DCI (count mode)			0	20	
Pulse duration, TCK high or low	t_{w1}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	16.0		ns
Pulse duration, DCI high or low (count mode)	t_{w2}			4.5 V and 5.5 V	9, 10, 11	9.0		
Pulse duration, TRST low	t_{w3}			4.5 V and 5.5 V	9, 10, 11	10.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Setup time, high or low, TMS before TCK↑	t_{s1}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	9.0		ns
Setup time, high or low, OTMS before TCK↑	t_{s2}		4.5 V and 5.5 V	9, 10, 11	12.0		
Setup time, high or low, TDI before TCK↑	t_{s3}		4.5 V and 5.5 V	9, 10, 11	11.0		
Setup time, high or low, DTDI before TCK↑	t_{s4}		4.5 V and 5.5 V	9, 10, 11	5.0		
Setup time, high or low, MCI before TCK↑	t_{s5}		4.5 V and 5.5 V	9, 10, 11	5.0		
Setup time, high or low, DCI before TCK↑	t_{s6}		4.5 V and 5.5 V	9, 10, 11	9.0		
Setup time, high or low, IDn before TCK↑	t_{s7}		4.5 V and 5.5 V	9, 10, 11	3.0		
Hold time, hgih or low, TMS after TCK↑	t_{h1}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	2.0		ns
Hold time, high or low, OTMS after TCK↑	t_{h2}		4.5 V and 5.5 V	9, 10, 11	2.0		
Hold time, high or low, TDI after TCK↑	t_{h3}		4.5 V and 5.5 V	9, 10, 11	4.0		
Hold time, high or low, DTDI after TCK↑	t_{h4}		4.5 V and 5.5 V	9, 10, 11	4.0		
Hold time, high or low, MCI after TCK↑	t_{h5}		4.5 V and 5.5 V	9, 10, 11	5.0		
Hold time, high or low, DCI after TCK↑	t_{h6}		4.5 V and 5.5 V	9, 10, 11	5.0		
Hold time, high or low, IDn after TCK↑	t_{h7}		4.5 V and 5.5 V	9, 10, 11	5.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Maximum frequency	f_{MAX}	C_L = 50 pF minimum R_L = 500Ω See figure 5	TCK	4.5 V and 5.5 V	9, 10, 11	20.0		MHz
			DCI (count mode)			20.0		
Propagation delay time, TCK to DTCK 3003	t_{PLH1}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	3.0	16.0	ns
	t_{PHL1}			4.5 V and 5.5 V	9, 10, 11	3.0	19.0	
Propagation delay time, TCK↓ to TDO 3003	t_{PLH2}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	7.0	30.0	ns
	t_{PHL2}			4.5 V and 5.5 V	9, 10, 11	7.0	29.0	
Propagation delay time, TCK↓ to DTDO 3003	t_{PLH3}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	7.0	31.0	ns
	t_{PHL3}			4.5 V and 5.5 V	9, 10, 11	7.0	29.0	
Propagation delay time, TCK↓ to DTMSm 3003	t_{PLH4}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	11.0	40.0	ns
	t_{PHL4}			4.5 V and 5.5 V	9, 10, 11	11.0	37.0	
Propagation delay time, TCK↓ to DTRST 3003	t_{PLH5}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	9.0	35.0	ns
	t_{PHL5}			4.5 V and 5.5 V	9, 10, 11	9.0	35.0	
Propagation delay time, TCK↓ to IDn 3003	t_{PLH6}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	20.0	65.0	ns
	t_{PHL6}			4.5 V and 5.5 V	9, 10, 11	22.0	65.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, TCK↓ to MCO 3003	t_{PLH7}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	9.0	34.0	ns
	t_{PHL7}			4.5 V and 5.5 V	9, 10, 11	9.0	31.0	
Propagation delay time, TCK↓ to DCO 3003	t_{PLH8}	C_L = 50 pF minimum R_L = 500Ω See figure 5	Open drain	4.5 V and 5.5 V	9, 10, 11	14.0	45.0	ns
			Three-state			10.0	40.0	
	t_{PHL8}		Open drain	4.5 V and 5.5 V	9, 10, 11	10.0	39.0	
			Three-state			10.0	37.0	
Propagation delay time, TMS to DTMSm 3003	t_{PLH9}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	5.0	22.0	ns
	t_{PHL9}			4.5 V and 5.5 V	9, 10, 11	4.0	23.0	
Propagation delay time, OTMS to DTMSm 3003	t_{PLH10}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	5.0	22.0	ns
	t_{PHL10}			4.5 V and 5.5 V	9, 10, 11	4.0	23.0	
Propagation delay time, MCI to MCO 3003	t_{PLH11}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	7.0	26.0	ns
	t_{PHL11}			4.5 V and 5.5 V	9, 10, 11	6.0	25.0	
Propagation delay time, DCI to DCO 3003	t_{PLH12}	C_L = 50 pF minimum R_L = 500Ω See figure 5	Open drain	4.5 V and 5.5 V	9, 10, 11	8.0	32.0	ns
			Three-state			8.0	30.0	
	t_{PHL12}		Open drain	4.5 V and 5.5 V	9, 10, 11	8.0	34.0	
			Three-state			8.0	30.0	
Propagation delay time, TRST to DTRST 3003	t_{PLH13}	C_L = 50 pF minimum R_L = 500Ω See figure 5		4.5 V and 5.5 V	9, 10, 11	4.0	20.0	ns
	t_{PHL13}			4.5 V and 5.5 V	9, 10, 11	5.0	25.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Propagation delay time, output disable, TCK↓ to TDO 3003	t_{PHZ1}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	3.0	17.0	ns
	t_{PLZ1}		4.5 V and 5.5 V	9, 10, 11	3.0	18.0	
Propagation delay time, output disable, TCK↓ to DTDO 3003	t_{PHZ2}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	3.0	18.0	ns
	t_{PLZ2}		4.5 V and 5.5 V	9, 10, 11	7.0	26.0	
Propagation delay time, output disable, TCK↓ to DTMSm 3003	t_{PHZ3}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	7.0	26.0	ns
	t_{PLZ3}		4.5 V and 5.5 V	9, 10, 11	7.0	28.0	
Propagation delay time, output disable, TCK↓ to DCO 3003	t_{PHZ4}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	9.0	28.0	ns
	t_{PLZ4}		4.5 V and 5.5 V	9, 10, 11	7.0	31.0	
Propagation delay time, output disable, TCK↓ to IDn 3003	t_{PHZ5}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	12.0	38.0	ns
	t_{PLZ5}		4.5 V and 5.5 V	9, 10, 11	9.0	34.0	
Propagation delay time, output disable, DCI to IDn 3003	t_{PHZ6}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	8.0	27.0	ns
	t_{PLZ6}		4.5 V and 5.5 V	9, 10, 11	10.0	33.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Propagation delay time, output enable, TCK↓ to TDO 3003	t_{PZH1}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	9.0	35.0	ns
	t_{PZL1}		4.5 V and 5.5 V	9, 10, 11	9.0	36.0	
Propagation delay time, output enable, TCK↓ to DTDO 3003	t_{PZH2}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	10.0	39.0	ns
	t_{PZL2}		4.5 V and 5.5 V	9, 10, 11	10.0	40.0	
Propagation delay time, output enable, TCK↓ to DTMSm 3003	t_{PZH3}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	8.0	34.0	ns
	t_{PZL3}		4.5 V and 5.5 V	9, 10, 11	8.0	34.0	
Propagation delay time, output enable, TCK↓ to DCO 3003	t_{PZH4}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	12.0	46.0	ns
	t_{PZL4}		4.5 V and 5.5 V	9, 10, 11	10.0	38.0	
Propagation delay time, output enable, TCK↓ to IDn 3003	t_{PZH5}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	20.0	73.0	ns
	t_{PZL5}		4.5 V and 5.5 V	9, 10, 11	22.0	58.0	
Propagation delay time, output enable, MCI to IDn 3003	t_{PZH6}	C_L = 50 pF minimum R_L = 500Ω See figure 5	4.5 V and 5.5 V	9, 10, 11	18.0	65.0	ns
	t_{PZL6}		4.5 V and 5.5 V	9, 10, 11	20.0	62.0	

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \ge 3.0$ V.

TABLE I. Electrical performance characteristics - Continued.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ For I/O ports, the limit includes the input leakage current. For the DCO, the limit includes the open drain output leakage current.

5/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0.0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\ V$ (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.0 mA, and the preferred method and limits are guaranteed.

6/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth tables and other logic patterns used for fault detection. The test vectors used to verify the truth tables shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth tables in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, $V_{IL} = 0.4\ V$ and $V_{IH} = 2.4\ V$. For outputs, $L \le 0.8\ V$, $H \ge 2.0\ V$.

Device type	01	
Case outlines	X	3
Terminal number	Terminal symbol	
1	DTDI	ID5
2	OTMS	ID4
3	DCO	ID3
4	MCO	ID2
5	DTDO	ID1
6	DTCK	MCI
7	GND	DCI
8	DTMS1	DTDI
9	DTMS2	OTMS
10	DTMS3	DCO
11	DTMS4	MCO
12	$\overline{\text{DTRST}}$	DTDO
13	TDO	DTCK
14	TMS	GND
15	TCK	DTMS1
16	TDI	DTMS2
17	$\overline{\text{TRST}}$	DTMS3
18	ID8	DTMS4
19	ID7	$\overline{\text{DTRST}}$
20	ID6	TDO
21	V_{CC}	TMS
22	ID5	TCK
23	ID4	TDI
24	ID3	$\overline{\text{TRST}}$
25	ID2	ID8
26	ID1	ID7
27	MCI	ID6
28	DCI	V_{CC}

FIGURE 1. Terminal connections.

Terminal descriptions	
Terminal symbol	Description
IDn (n = 1 to 8)	Identification I/Os
DCI	Device condition input
DCO	Device condition output
DTCK	Device test clock output
DTDI	Device test data input
DTDO	Device test data output
DTMSm (m = 1 to 4)	Device test mode select outputs
$\overline{\text{DTRST}}$	Device test reset output
MCI	Master condition input
MCO	Master condition output
OTMS	Optional test mode select input
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
$\overline{\text{TRST}}$	Test reset input

FIGURE 1. Terminal connections - Continued.

DCO function table

DCI	Internal signals			Control register bits 1/							DCO
	$\overline{\text{I RERR}}$	$\overline{\text{SRERR}}$	$\overline{\text{CE}}$	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	
X	X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	X	1	0	X	Z
X	X	X	X	0	0	0	X	X	1	X	H
X	X	X	X	1	0	0	X	X	1	X	L
X	X	X	X	0	0	1	1	X	1	X	H
X	X	X	X	1	0	1	1	X	1	X	L
X	0	X	X	0	0	1	0	X	1	X	L in pause-IR 2/, otherwise
X	X	0	X	0	0	1	0	X	1	X	L in pause-DR 2/, otherwise
X	1	1	X	0	0	1	0	X	1	X	H
X	0	X	X	1	0	1	0	X	1	X	H in pause-IR 2/, otherwise
X	X	0	X	1	0	1	0	X	1	X	H in pause-DR 2/, otherwise
X	1	1	X	1	0	1	0	X	1	X	L
X	X	X	0	0	1	0	X	X	1	X	L
X	X	X	0	1	1	0	X	X	1	X	H
X	X	X	1	0	1	0	X	X	1	X	H
X	X	X	1	1	1	0	X	X	1	X	L
0	X	X	X	1	1	1	X	X	1	0	H
0	X	X	X	1	1	1	X	X	1	1	L
0	X	X	X	0	1	1	X	X	1	0	L
0	X	X	X	0	1	1	X	X	1	1	H
1	X	X	X	1	1	1	X	X	1	0	L
1	X	X	X	1	1	1	X	X	1	1	H
1	X	X	X	0	1	1	X	X	1	0	H
1	X	X	X	0	1	1	X	X	1	1	L

H = High voltage level
L = Low voltage level
X = Irrelevant

1/ The control register must contain these values after the TAP has passed through its most recent update-DR state.

2/ DCO becomes active on the falling edge of TCK as the TAP enters the appropriate pause state (pause-IR or pause-DR) and becomes inactive on the falling edge of TCK as the TAP enters the appropriate exit2 state (exit-IR or exit-DR).

FIGURE 2. Truth tables.

$\overline{\text{I RERR}}$ function table

Number of instruction register bits = 1	$\overline{\text{I RERR}}$
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

$\overline{\text{SRERR}}$ function table

Select register bits								$\overline{\text{SRERR}}$
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0	X	0	X	0	X	0	X	1
1	X	0	X	0	X	0	X	1
0	X	1	X	0	X	0	X	1
0	X	0	X	1	X	0	X	1
0	X	0	X	0	X	1	X	1
1	X	1	X	X	X	X	X	0
1	X	X	X	1	X	X	X	0
1	X	X	X	X	X	1	X	0
X	X	1	X	1	X	X	X	0
X	X	1	X	X	X	1	X	0
X	X	X	X	1	X	1	X	0

FIGURE 2. Truth tables - Continued.

$\overline{\text{RSRERR}}$ function table

Select register bits								$\overline{\text{RSRERR}}$	MCO 1/
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
0	X	0	X	0	X	0	X	1	MCI
1	X	0	X	0	X	0	X	1	MCI
0	X	1	X	0	X	0	X	1	MCI
0	X	0	X	1	X	0	X	1	MCI
0	X	0	X	0	X	1	X	1	MCI
1	X	1	X	X	X	X	X	0	L
1	X	X	X	1	X	X	X	0	L
1	X	X	X	X	X	1	X	0	L
X	X	1	X	1	X	X	X	0	L
X	X	1	X	X	X	1	X	0	L
X	X	X	X	1	X	1	X	0	L

L = Low voltage level
X = Irrelevant

1/ This table is valid only when the remote TAP is in the pause-state. Under any other condition, MCO = MCI.

FIGURE 2. Truth tables - Continued.

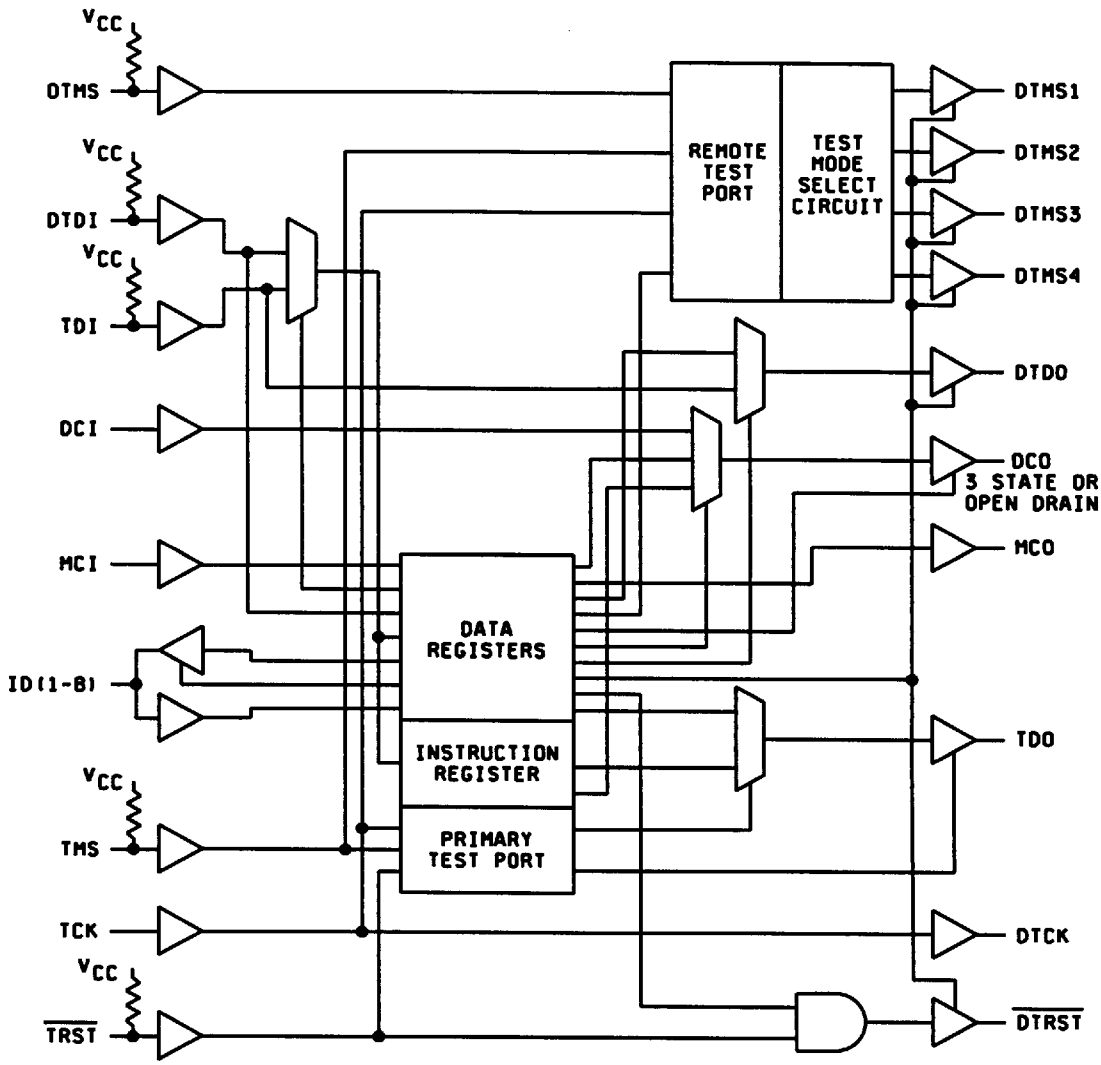


FIGURE 3. Block diagram.

Test access port (TAP) controller state diagram

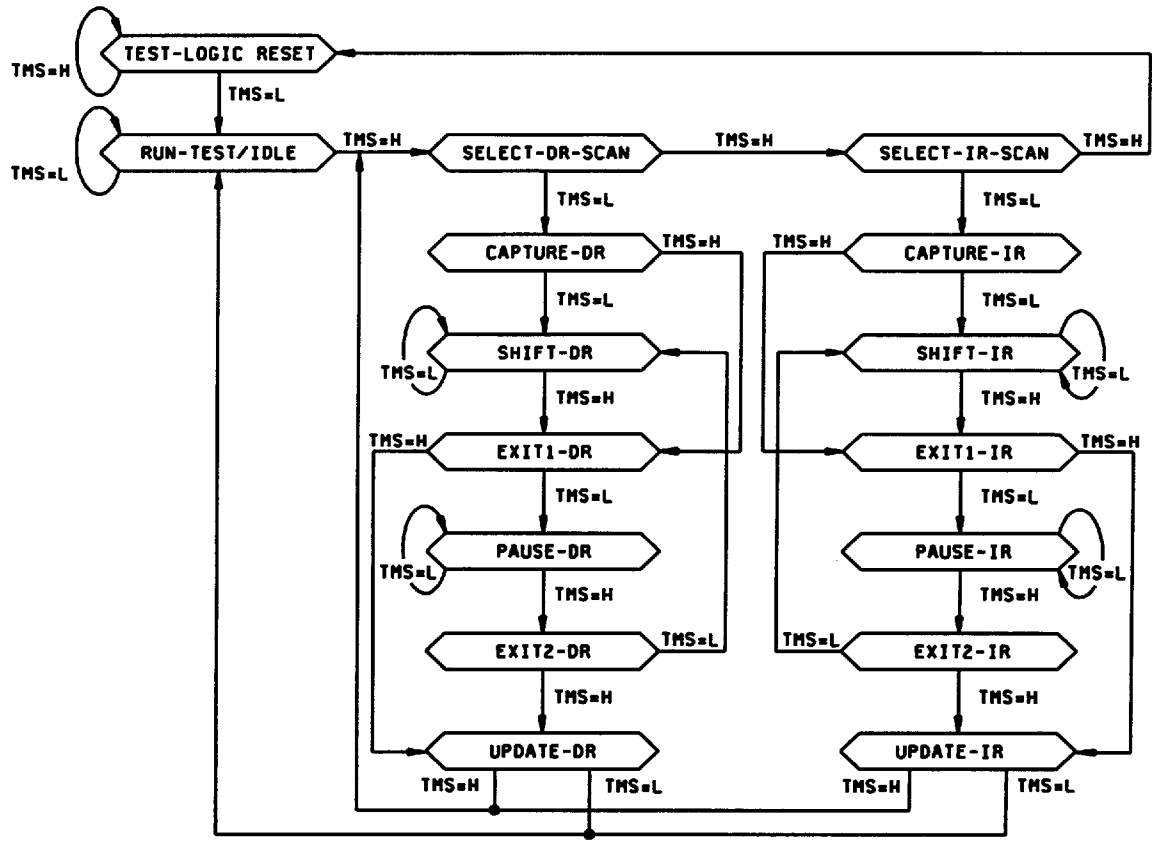
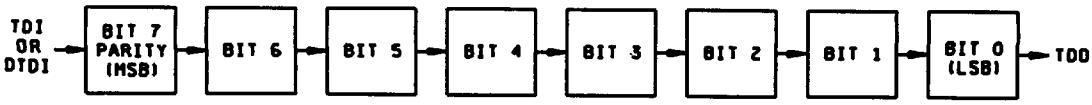


FIGURE 4. Test access port controller and scan test registers.

Instruction register (IR) order of scan



NOTE: The MSB of the IR is an even-parity bit. If the value scanned into the IR during shift-IR does not contain even parity, an error signal (I RERR) is generated internally as shown in figure 2 of I RERR function table. The device can be configured to output I RERR via DCO if the TAP enters the pause-IR state.

During the capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instructionand select registers and the logic level present at the DCI input. The IR status word is encoded as shown in the IR status word table on next sheet.

Instruction-register opcodes

Binary code 1/ Bit 7 → Bit 0 MSB → LSB	Hex value	Scope opcode	Description	Selected data Register
00000000	00	EXTEST	Boundary scan	Boundary scan
10000001	81	BYPASS	Bypass scan	Bypass
10000010	82	SAMPLE/PRELOAD	Sample boundary	Boundary scan
00000011	03	INTEST	Boundary scan	Boundary scan
10000100	84	BYPASS 2/	Bypass scan	Bypass
00000101	05	BYPASS 2/	Bypass scan	Bypass
00000110	06	BYPASS 2/	Bypass scan	Bypass
10000111	87	BYPASS 2/	Bypass scan	Bypass
10001000	88	COUNT	Count	Bypass
00001001	09	COUNT	Count	Bypass
00001010	0A	BYPASS 2/	Bypass scan	Bypass
10001011	8B	BYPASS 2/	Bypass scan	Bypass
00001100	0C	BYPASS 2/	Bypass scan	Bypass
10001101	8D	BYPASS	Bypass scan	Bypass
10001110	8E	SCANCN	Control register scan	Control
00001111	0F	SCANCT	Control register scan	Control
11111010	FA	SCANCNT	Counter scan	Counter
01111011	7B	READCNT	Counter read	Counter
11111100	FC	SCANIDB	ID bus register scan	ID bus
01111101	7D	READIDB	ID bus register read	ID bus
01111110	7E	SCANSEL	Select register scan	Select
All others		BYPASS	Bypass scan	Bypass

1/ Bit 7 is used to maintain even parity in the 8-bit instruction.
2/ A scope opcode exists but not supported by this device.

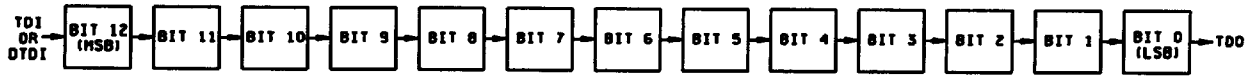
FIGURE 4. Test access port controller and scan test registers - Continued.

Instruction-register status word

IR Bit	Value 1/
7	$\overline{\text{I RERR}}$ (see figure 2 of $\overline{\text{I RERR}}$ function table)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	$\overline{\text{SRERR}}$ (see figure 2 of $\overline{\text{SRERR}}$ function table)
1	0
0	1

1/ This value is loaded in the instruction register during the capture-IR TAP state.

Control-register (CTLR) bits and order of scan



NOTE: A reset operation forces all bits to a logic 0. The contents of the control register are latched and decoded during the update-DR TAP state. The specific function of each bit is listed in the control-register bit mapping below. Several control-register bits affect the functionality of the DCO output. The DCO function table is given in figure 2 herein.

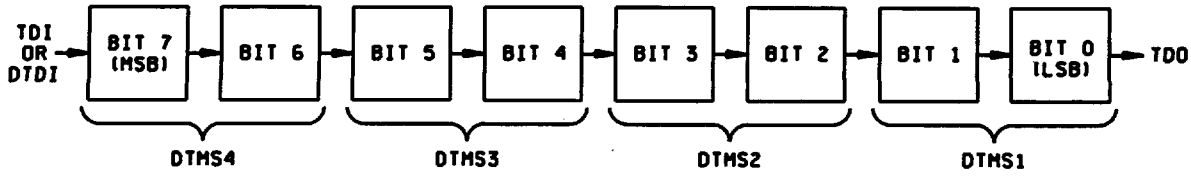
FIGURE 4. Test access port controller and scan test registers - Continued.

Control-register bit mapping

Bit	Value	Function
12	0	Configure counter to count up
	1	Configure counter to count down
11	0	Do not stop counting when the count reaches 00000000
	1	Stop counting when the count reaches 00000000 (count down only)
10	0	Configure DCO as an active-low output
	1	Configure DCO as an active-high output
9, 8	00	DCO = Inactive (level depends on CTLR bit 10)
	01	DCO = ($\overline{\text{I RERR}}$•$\overline{\text{SRERR}}$)
	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111(count up)
	11	DCO = DCI
7	0	Do not mask $\overline{\text{I RERR}}$ and $\overline{\text{SRERR}}$ from DCO
	1	Mask $\overline{\text{I RERR}}$ and $\overline{\text{SRERR}}$ from DCO
6	0	Configure DCO as an open-drain output
	1	Configure DCO as a three-state output
5	0	Disable DCO
	1	Enable DCO
4	0	DCI = DCI
	1	DCI = $\overline{\text{DCI}}$ (invert DCI the signal before applying it to the internal logic)
3	0	Enable DTCK, DTDO, and DTMSm (m = 1 to 4)
	1	Disable DTCK, DTDO, and DTMSm (m = 1 to 4)
2	0	Disable IDn (n = 1 to 8)
	1	Enable IDn (n = 1 to 8)
1	0	Disable RBC
	1	Enable RBC
0	0	$\overline{\text{DTRST}}$ = $\overline{\text{TRST}}$
	1	$\overline{\text{DTRST}}$ = L

FIGURE 4. Test access port controller and scan test registers - Continued.

Select-register (SR) bits and order of scan



NOTE: A reset operation forces all bits to a logic 0. The register is divided into four 2-bit sections, each of which controls one DTMS output. For each DTMS pin, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB and bit 2 is the LSB of DTMS2).

Only one of the four DTMS outputs can be selected to drive the secondary scan path with TMS or OTMS. If the SR is loaded with an invlid value, an error signal (SRERR) is generated internally as shown in figure 2 of SRERR function table. If the TAP enters the pause-DR state, SRERR may be output via DCO. If the TAP enters the update-DR state while an invalid value is in the SR, all four DTMS outputs are set to a high level.

The SR can be accesssed from a remote bus controller (RBC). A test port in the register contains a TAP that can be enabled by the control register to monitor the values of TCK and OTMS to perform scan operations on the SR. The SR bit decoding is shown in the following table:

Select-register bit decoding

MSB	LSB	DTMS source
0	0	H
0	1	L
1	0	OTMS
1	1	TMS

Boundary-scan register (BSR) bits and order of scan

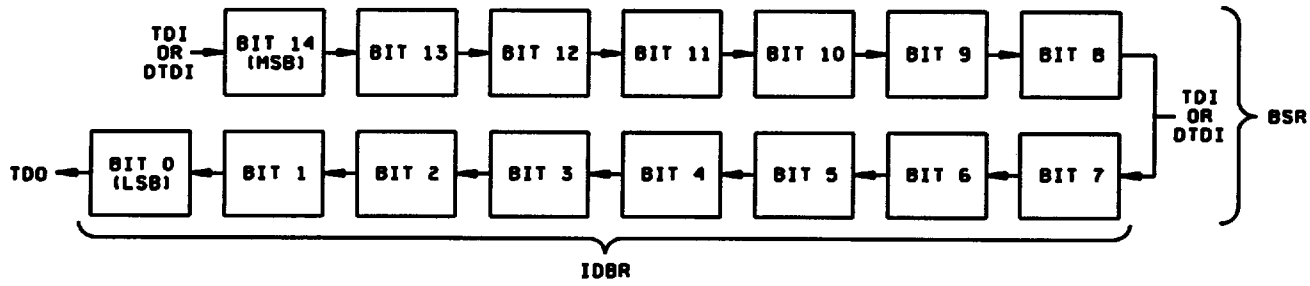


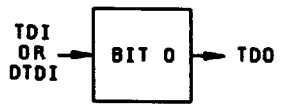
FIGURE 4. Test access port controller and scan test registers - Continued.

Boundary-scan register bit mapping

Bit	Terminal name	Signal description
14	MCI	Master condition in
13	MCO	Master condition out
12	DCI	Device condition in
11	$\overline{\text{DCOTS}}$ 1/	Enable control for DCO in three-state configuration (active low)
10	$\overline{\text{DCOOD}}$ 1/	Enable control for DCO in open-drain configuration (active low)
9	DCO	Device condition out
8	$\overline{\text{IDBOE}}$ 1/	Enable control for ID bus (active low)
7	ID 8	Identification bus bit 8
6	ID7	Identification bus bit 7
5	ID6	Identification bus bit 6
4	ID5	Identification bus bit 5
3	ID4	Identification bus bit 4
2	ID3	Identification bus bit 3
1	ID2	Identification bus bit 2
0	ID1	Identification bus bit 1

1/ This internal signal cannot be observed from the I/O pins of the device.

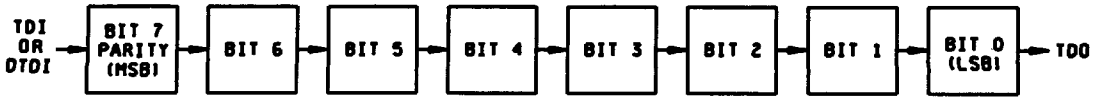
Bypass-register (BR) bit and order of scan



NOTE: The function of the BR is to provide a means of effectively removing the device from the primary scan path when it is not needed for the current test operation or other function of the primary bus controller. At power up, the BR is placed in the scan path.

FIGURE 4. Test access port controller and scan test registers - Continued.

Counter-register (CNTR) bits and order of scan



NOTE: A reset operation forces all bits of the shift register to logic 0 but does not affect the counter.

An internal signal, $\overline{CE}$, is generated as a logic 0 when the count reaches its end value (i.e., 00000000 for count down, 11111111 for count up). For any other count value, CE is a logis 1. Many of the features of the CNTR are configured by a bit in the CNTR including:

Count direction up or down (control register bit 12; reset condition count up).

Stop counting up counting down to 00000000 (control register bit 11; reset conditon = do not latch on zero).

Output $\overline{CE}$ signal at DCO (control register bits 8 and 9; reset conditon = do not output $\overline{CE}$ at DCO).

Edge of DCI on which to trigger (control register bit 4; reset condition = positive edge).

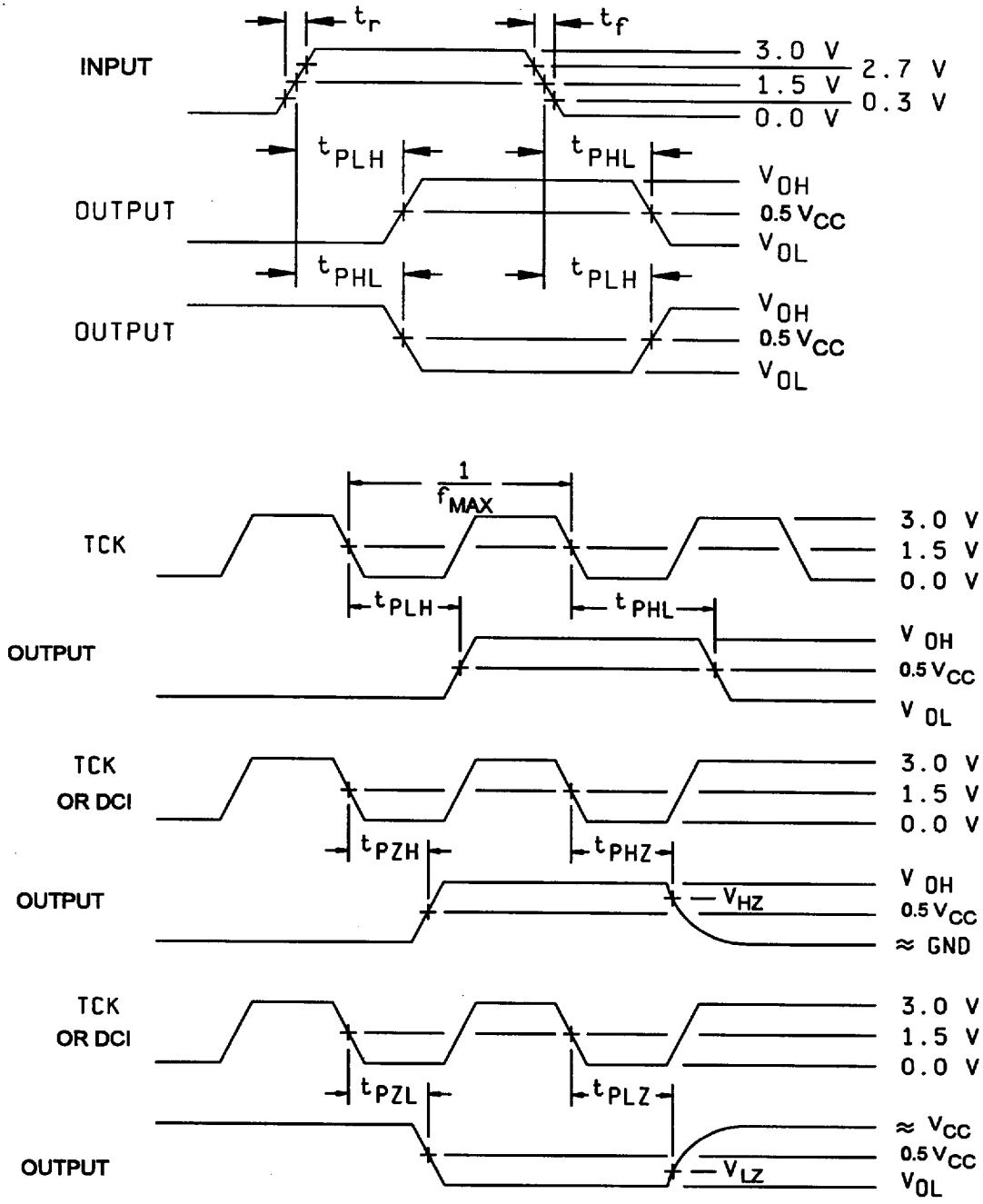
Remote-test-port instruction-register opcodes

Binary code Bit 7 → Bit 0 MSB → LSB	Scope opcode	Description	Selected data register
01111110	SCANSEL	Select-register scan	Select
All other	BYPASS	Bypass scan	Bypass

NOTE: Bit 1 in the control register allows a remote bus controller (RBC) to control parts of the device. When an RBC is enabled, the remote test port (RTP) in the select register is activated. The RTP does not have access to the control register, so it cannot disable itself. The primary bus controller (PBC) must reset bit 1 in the control register to return control of the select register to the primary test port.

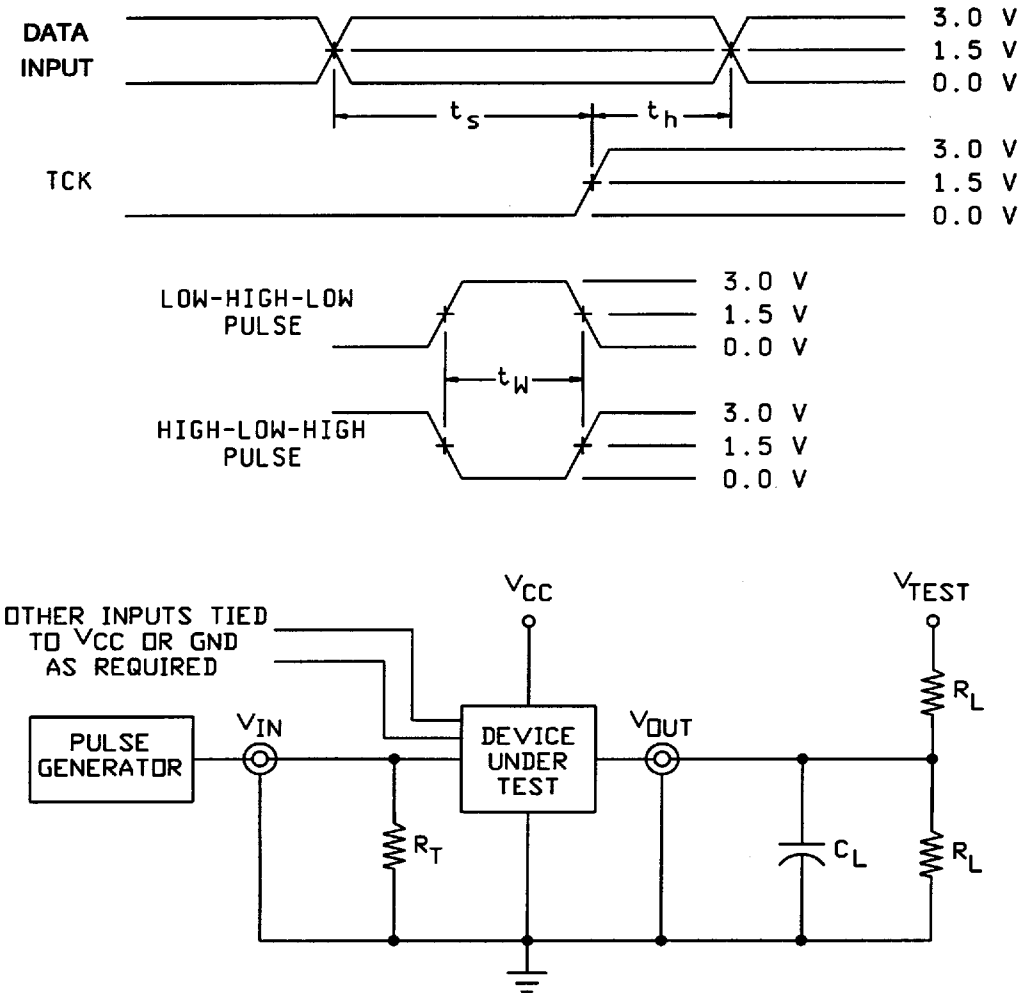
An internal error signal ($\overline{RSRERR}$) is generated if an RBC loads an invalid value in the select register, and the MCO output goes low if the RSRERR is active and the remote TAP enters the pause-DR state. The RSRERR function table is shown in figure 2 herein.

FIGURE 4. Test access port controller and scan test registers - Continued.



NOTE: V_{HZ} = 0.9 V_{CC} for ID-bus pins and V_{HZ} = 0.8 V_{CC} for all other pins. V_{LZ} = 0.1 V_{CC} for ID-bus pins and V_{LZ} = 0.2 V_{CC} for all other pins.

FIGURE 5. Switching waveforms and test circuit.



NOTES:
1. When measuring t_{PLZ} and t_{PZL}: $V_{TEST} = V_{CC}$ for ID-bus pins and $V_{TEST} = 2 \times V_{CC}$ for all other pins.
2. When measuring t_{PLH} and t_{PHL}: V_{TEST} = open.
3. When measuring t_{PHZ} and t_{PZH}: V_{TEST} = 0.0 V.
4. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
5. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
6. R_L = 500Ω or equivalent.
7. R_T = 50Ω or equivalent.
8. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r = 3.0 ns; t_f = 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
9. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
10. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth tables in figure 2 herein. The test vectors used to verify the truth tables shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth tables in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center, Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-03-18

Approved sources of supply for SMD 5962-96747 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9674701QXA	3/	
5962-9674701Q3A	01295	SNJ54ACT8999FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved of supply as of the date of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

9004708 0028096 266