

1.1 Scope.

This specification covers the detail requirements for complete 8-bit and 10-bit resolution A/D converters with full microprocessor interface.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD673SD/883B
- 2	AD573SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-20.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Digital Common		+7V
V_{EE} to Digital Common		-16.5V
Analog Common to Digital Common		$\pm 1\text{V}$
Analog Input to Analog Common		$\pm 15\text{V}$
Control Inputs		0 to V_{CC}
Digital Outputs (High Impedance State)		0 to V_{CC}
Power Dissipation		800mW
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)		300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C/W}$
 $\theta_{JA} = 85^\circ\text{C/W}$

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Table 1.

Test	Symbol	Device ²	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	-1	0.195	0.195	0.195		Unipolar and Bipolar Major Transitions ± 3 Codes	± % of FS max
		-2	0.098	0.195	0.098	0.098		
Differential Nonlinearity ³	DNL	-1	8	8	8		All codes test Unipolar and Bipolar	Bits min
		-2	10	8	10	10		
Full-Scale Error ⁴	A _{FE}	-1, 2	40	40			Unipolar	± mV max
		-1, 2	20	20			Bipolar	± mV max
Full-Scale Temperature Drift	TCA _{FE}	-1	0.781		0.781			± % of FS max
		-2	0.488		0.488			
Offset Error	V _{OS}	-1	20	20			First Transition	± mV max
		-2	10	20		10		
Offset Temperature Drift	TCV _{OS}	-1	0.391		0.391			± % of FS max
		-2	0.195		0.195			
Bipolar Zero Error	BPZE	-1	20	20			Low Side MSB Transition Bipolar	± mV max
		-2	10	20		10		
Bipolar Zero Temperature Drift	TCBPZE	-1	0.391		0.391		Low Side MSB Transition Bipolar	± % of FS max
		-2	0.195		0.195			
Input Resistance	R _{IN}	-1, 2	3	3	3			kΩ min
			7	7	7			kΩ max
Conversion Time ⁵	t _C	-1, 2	10	10	10			μs min
			30	30	30			μs max
Three-State Leakage Current	I _{OLT}	-1	40	40	40		V _{OH} = 5.0V V _{OL} = 0.0V, DB0-DB7	± μA max
		-2	40	40	40		V _{OH} = 5.0V V _{OL} = 0.0V, DB0-DB9	
Power Supply Rejection Ratio	PSRR	-1	78.1	78.1	78.1		V _{CC} = 5V, -15.75V ≤ V _{EE} ≤ -14.25V V _{CC} = 5V, -12.6V ≤ V _{EE} ≤ -11.4V	± mV max
		-2	19.5	78.1	78.1	19.5	V _{EE} = -15V, 4.5V ≤ V _{CC} ≤ 5.5V	
Power Supply Current	I _{CC}	-1, 2	15	15			DR LOW	+ mA max
			15	15			DR HIGH (During Conversion)	
	I _{EE}	-1, 2	15	15				- mA max
Digital Input High Voltage	V _{IH}	-1, 2	2.0	2.0	2.0		Convert, HBE, LBE, DE	+ V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8		Convert, HBE, LBE, DE	+ V max
Digital Input High Current	I _{IH}	-1, 2	100	100	100		Convert, HBE, LBE, DE V _{IH} = 5.0V	± μA max
Digital Input Low Current	I _{IL}	-1, 2	100	100	100		Convert, HBE, LBE, DE V _{IL} = 0.0V	± μA max
Digital Output Low Voltage	V _{OL}	-1	0.4	0.4	0.4		I _{OL} = +3.2mA, DR, DB0-DB7	+ V max
		-2	0.4	0.4	0.4		I _{OL} = +3.2mA DR, DB0-DB9	
Digital Output High Voltage	V _{OH}	-1	2.4	2.4	2.4		I _{OH} = -0.5mA, DB0-DB7	+ V min
		-2	2.4	2.4	2.4		I _{OH} = -0.5mA, DB0-DB9	

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Convert Pulse Width ⁵	t_{CS}	-1, 2	500		500	500		ns min
DR Delay Convert ⁵	t_{DSC}	-1, 2	1.5			1.5		μs max
Data Valid After $\overline{DE}$, HBE or $\overline{LBE}$ High ⁶	t_{HD}	-1, 2	50					ns min
Output Float Delay ⁶	t_{HL}	-1, 2	200			200		ns max
Data Access Time ⁶	t_{DD}	-1, 2	250			250		ns max

NOTES

¹ $V_{CC} = +5V$, $V_{EE} = -15V$, analog input through 15Ω resistor to Pin 13, Unipolar configuration.

$T_A = 25^\circ C$ unless otherwise indicated.

Unipolar configuration Pin 16 (Bipolar Offset Control) is grounded.

Bipolar configuration Pin 16 is not connected.

²For -1 (8-Bit resolution Device), 0.391% of full scale = 1 LSB (least significant bit). For -2 (10-Bit resolution device), 0.098% of full scale = 1 LSB.

³Minimum resolution for which no missing codes are guaranteed.

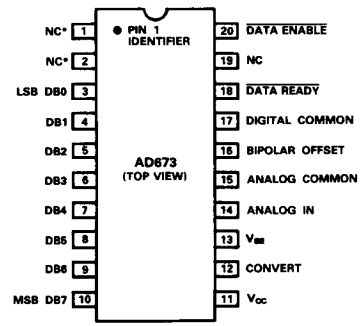
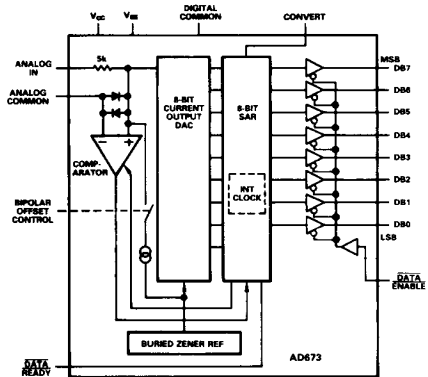
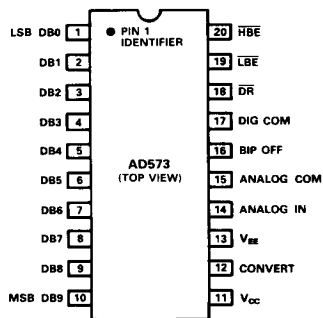
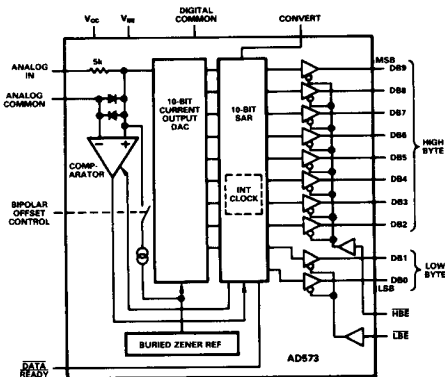
⁴-1 device full scale error guaranteed trimmable with 500Ω potentiometer.

-2 device full scale error guaranteed trimmable with 200Ω potentiometer.

⁵See Figure 1.

⁶See Figures 2 and 3.

3.2.1 Functional Block Diagram and Terminal Assignments.



*PINS 1 & 2 ARE INTERNALLY CONNECTED TO TEST POINTS AND SHOULD BE LEFT FLOATING

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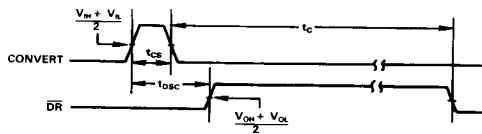


Figure 1. AD573 and AD673 CONVERT Timing

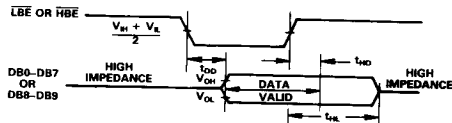


Figure 2. AD573 READ Timing

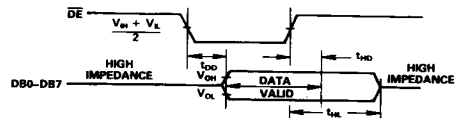


Figure 3. AD673 READ Timing

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

