Features

- High-performance, Low-power AVR[®] 8-bit Microcontroller
 - 130 Powerful Instructions Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 8 MIPS Throughput at 8 MHz
 - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
- Self-programming In-System Programmable Flash Memory
 - 16K Bytes with Optional Boot Block (256 2K Bytes) Endurance: 1,000 Write/Erase Cycles
 - Boot Section Allows Reprogramming of Program Code without External Programmer
 - Optional Boot Code Section with Independent Lock Bits
 - 512 Bytes EEPROM
 - Endurance: 100,000 Write/Erase Cycles
 - 1024 Bytes Internal SRAM
 - Programming Lock for Software Security
- Peripheral Features
 - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
 - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
 - Real Time Clock with Separate Oscillator and Counter Mode
 - Three PWM Channels
 - 8-channel, 10-bit ADC
 - Byte-oriented Two-wire Serial Interface
 - Programmable Serial UART
 - Master/Slave SPI Serial Interface
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - Analog Comparator
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Four Sleep Modes: Idle, ADC Noise Reduction, Power-save, and Power-down
- Power Consumption at 4 MHz, 3.0V, 25°C
 - Active 5.0 mA
 - Idle Mode 1.9 mA
 - Power-down Mode < 1 μA
- I/O and Packages
 - 32 Programmable I/O Lines
 - 40-pin PDIP and 44-pin TQFP
- Operating Voltages
 - 2.7 5.5V for ATmega163L
 - 4.0 5.5V for ATmega163
- Speed Grades
 - 0 4 MHz for ATmega163L
 - 0 8 MHz for ATmega163



8-bit **AVR**[®] Microcontroller with 16K Bytes In-System Programmable Flash

ATmega163 ATmega163L

Summary

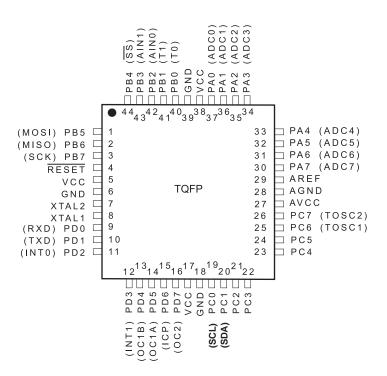
Not Recommend for New Designs. Use ATmega16.

Rev.1142ES-AVR-02/03





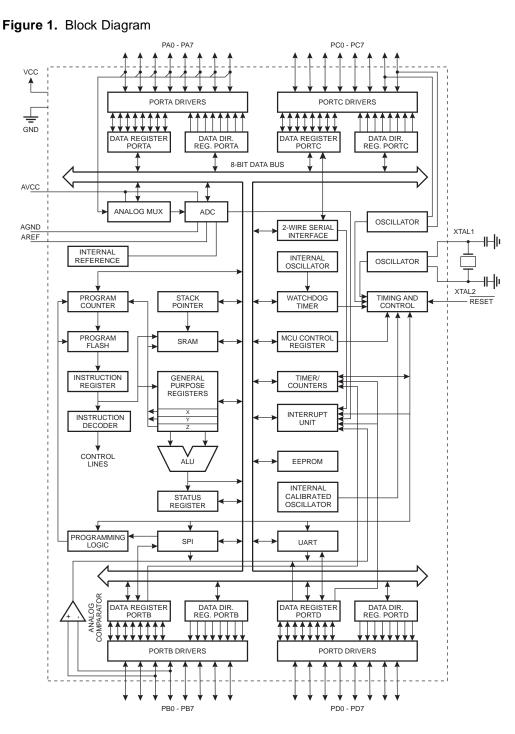
Pin Configurations



Description

The ATmega163 is a low-power CMOS 8-bit microcontroller based on the AVR architecture. By executing powerful instructions in a single clock cycle, the ATmega163 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock





cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega163 provides the following features: 16K bytes of In-System Self-Programmable Flash, 512 bytes EEPROM, 1024 bytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, a programmable serial UART, an SPI serial port, and four software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous Timer Oscillator continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions.

The On-chip ISP Flash can be programmed through an SPI serial interface or a conventional programmer. By installing a Self-Programming Boot Loader, the microcontroller can be updated within the application without any external components. The Boot Program can use any interface to download the application program in the Application Flash memory. By combining an 8-bit CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega163 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega163 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

Pin Descriptions

VCC	Digital supply voltage.
GND	Digital ground.
Port A (PA7PA0)	Port A serves as the analog inputs to the A/D Converter. Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers can sink 20mA and can drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull- up resistors are activated. The Port A pins are tristated when a reset condition becomes active, even if the clock is not running.
Port B (PB7PB0)	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. Port B also serves the functions of various special features of the ATmega83/163 as listed on page 117. The Port B pins are tristated when a reset condition becomes active, even if the clock is not running.
Port C (PC7PC0)	Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tristated when a reset condition becomes active, even if the clock is not running.

4 ATmega163(L)

Port C also serves the functions of various special features of the ATmega163 as listed on page 124.

- Port D (PD7..PD0) Port D is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. Port D also serves the functions of various special features of the ATmega163 as listed on page 128. The Port D pins are tristated when a reset condition becomes active, even if the clock is not running.
- **RESET**Reset input. A low level on this pin for more than 500 ns will generate a Reset, even if
the clock is not running. Shorter pulses are not guaranteed to generate a Reset.
- **XTAL1** Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.
- XTAL2 Output from the inverting Oscillator amplifier.
- **AVCC** This is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. See page 105 for details on operation of the ADC.
- AREF
 AREF is the analog reference input pin for the A/D Converter. For ADC operations, a voltage in the range 2.5V to AVCC can be applied to this pin.
- AGND Analog ground. If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND.



AIMEL®

Register Summary

Address Name Bit 7 Bit 6 Bit 7 H S V N Z C C 20 55E (55C) SPH SP10 SP5 SP1 SP2 C C 20 55E (55C) SPH SP7 SP6 SP4 SP3 SP10 SP5 SP2 211 55C (55C) Reserved SP10 SP2 SP1 SP2		News	D:/ 7	Dit o	D% 5	D'' 4	D'' 0	Dit 0	D'' 4	Dit o	Dama
Size (Sec) SPH SPI			Bit /								-
SDB SED SPL SPS SPA SP3 SP2 SP1 SP0 21 SDB SGD SER MIT INTO - - - - - - - - - - - 30 SSB SSD SER SER SER CCIE2 TOE2 TOE1 - - - - - 30 SSB SSD SER CCIE2 TOE2 TOE2 TOE1 CCIE18 TOE11 - - - 30 SSB SSD MCCR WINT TWER AVEX - <			1	T	н	S	V				
S2C (SC) Reserved Intro Intro <thintro< th=""> Intro Intro</thintro<>			-	-	-	-					
S88 GMBK INTI INTO - 0 0 0 2 1 0 0 - <t< td=""><td></td><td></td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td><td>21</td></t<>			SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	21
38A (SA) OFR INTFI INTF0 <			INIT4	INITO	1	1	1	1	1	1	20
389 (58) TMBK OCIE2 TOLE2 TOLE1 OCIE18 OCIE18 TOLE1 TOLE1 TOLE1 TOLE3 T						-		_			
338 1FR OCF2 TOV2 ICF1 OCF18 OCF18 TOV1 TOV1 TOV1 TOV3 32 357 6570 SPUCR TWIRT TWER TWER TWER TWER TWER TWER TWER TWER TWER State State<									_		
Str SPMCR									-		
Sige Sige TWCR TWCR TWSTA TSTA TSTA TSTA TSTA TSTA TS											
328 (359) MCUGR - SE SM1 SM0 ISC11 ISC10 ISC01 ISC00 34 S34 (354) MCUSR - - - - - CS02 CS01 CS00 41 S33 (553) TCCR0 Tmer/Counter0 (Bts) - <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>											
334 (53) MCUSR - - - WDF BORF EXTFF PORF 28 333 (53) TORTO Tmer/Counter() (B Bis) -											
S33 DCR0 - - - - CS02 CS01 CS00 41 S32 DS2 DS2 CS01 CS01 CS00 41 S31 DS10 - - - - CS02 CS01 CS01 42 S31 DS10 - - - - ACME PUD PSR2 44 S32 DS41 CON141 COM141 COM141 COM141 PMM10 44 S20 DS40 TCNT11 Timer/Counter1 - Counter Register Migh Byte - CS11 CS1 CS1 46 S20 G440 TCNT11 Timer/Counter1 - Output Compare Register High Byte - 47 - 47 S28 G464 COR14L Timer/Counter1 - Noput Capture Register High Byte - 47 - 47 S28 G464 TCR24 FOC2 PVM2 COM20 CT2 CS21 CS20 S2 - 48						31010					
322 (32) TONTO Timer/Countrator (0 Bits) 37 331 (551) OSCAL Osellator Calibration Register 37 320 (550) SFIOR					_	_					
3511 0.95CCAL Oscillator Calibration Register				ter0 (8 Bits)				0002	0001	0000	
Sa0 (So) SFIOR					ter						
S2F GAH1 COM140 COM180 FOC1A FOC1A <thf< td=""><td></td><td></td><td></td><td>· · · · ·</td><td></td><td>-</td><td>ACME</td><td>PUD</td><td>PSR2</td><td>PSR10</td><td></td></thf<>				· · · · ·		-	ACME	PUD	PSR2	PSR10	
SZE (S4E) TCCR1B CKC1 CES1 - CTC1 CS12 CS11 CS10 45 SZD (S4D) TCNT1H Timer/Countert - Counter Register High Byte - 46 SZB (S4B) OCR1AH Timer/Counter 1 - Output Compare Register A Low Byte 47 SZB (S4B) OCR1BL Timer/Counter 1 - Output Compare Register A Low Byte 47 SZB (S4B) OCR1BL Timer/Counter 1 - Output Compare Register B Low Byte 47 SZB (S4B) OCR1BL Timer/Counter 1 - Output Compare Register I Sub Byte 47 SZB (S4B) OCR1BL Timer/Counter 1 - Input Capture Register I Sub Byte 48 SZB (S4B) OCR1BL Timer/Counter 2 (Btr) 53 SZB (S4B) OCR2 FOC2 PWM2 COM2 CTC2 CS21 CS20 52 SZB (S4B) OCR2 Timer/Counter 2 (Btr) 53 54 53 53 54 53 54 53 54 54 52 54 54 52 54 52 54 52 54			COM1A1	COM1A0	COM1B1	COM1B0					
\$20.640) TCNT1H Timer/Counterl - Counter Register High Pyre 46 \$26.640) CRN1L Timer/Counterl - Counter Register A High Pyre 47 \$26.6461) OCR1AH Timer/Counterl - Output Compare Register A High Pyre 47 \$26.6461) OCR1BH Timer/Counterl - Output Compare Register B High Pyre 47 \$26.6461) OCR1BH Timer/Counterl - Output Compare Register B High Pyre 48 \$26.6461) ICR1L Timer/Counterl - Output Compare Register Low Pyre 48 \$26.6461 TCOR2 FOC2 PVM2 COM20 CTC2 CS21 CS20 52 \$24.6451 TOR2 FOC2 PVM42 COM20 CTC2 CS21 CS20 52 \$24.6451 TOR2 Timer/Counter2 (Output Compare Register Low Pyre 53 54 54 52 \$24.6451 WDTCR - - MOTE VDP1 WDP0 60 \$25.04401 UBRR/113 - - - - EEAR8 62 \$26.6350 EEAR1 <t< td=""><td></td><td></td><td></td><td></td><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td></t<>					-						
SZC (S4C) TCNT1L Tmer/Counter1 - Output Compare Register A Low Brie 447 SZA (S4B) OCR1AL Tmer/Counter1 - Output Compare Register A Low Brie 477 SZB (S4B) OCR1BL Tmer/Counter1 - Output Compare Register B Low Brie 477 SZB (S4B) OCR1BL Tmer/Counter1 - Output Compare Register B Low Brie 47 SZB (S4B) OCR1BL Timer/Counter1 - Input Capture Register Low Brie 48 SZB (S4B) ICR1L Timer/Counter2 - Output Compare Register 53 SZB (S4B) ICR1L Timer/Counter2 Output Compare Register 53 SZB (S4B) ICR1Z Timer/Counter2 Output Compare Register 53 SZB (S4B) ICR1Z Timer/Counter2 Output Compare Register 53 SZB (S4B) UBRR1HI - - ASZ TCN2UB TCR2UB 57 SZB (S4B) UBRR1HI - - - UBRR1HI 78 54 SZB (S4B) UBRR1HI - - - - - - - - - - - <					Register High E						
S2B (S4A) OCR1AH Timer/Counter1 - Output Compare Register A High Byte 47 S2B (S4A) OCR1BH Timer/Counter1 - Output Compare Register B High Byte 47 S2B (S4B) OCR1BH Timer/Counter1 - Output Compare Register B High Byte 47 S2B (S4B) OCR1BH Timer/Counter1 - Input Capture Register B High Byte 48 S2B (S4B) ICR1H Timer/Counter1 - Input Capture Register High Byte 48 S2B (S4B) OCR1Z Timer/Counter2 (B lits) 52 S24 (S4A) TCR2Z PVM2 COM20 CTC2 CS21 CS20 52 S24 (S4A) TCR2Z Timer/Counter2 (B lits) 53 53 53 53 54 52 S24 (S4A) MDTCR - - - AS2 TCN2UB OCR2UB TCR2UB 57 S22 (S4A) MDTCR - - - - EEARB 62 51 53 S20 (S4D) UBRRHI - - - - EEARB 62 51 53					<u> </u>						
\$28(4A) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte 47 \$29(549) OCR1BL Timer/Counter1 - Output Compare Register B Low Byte 47 \$27(547) Inter/Counter1 - Output Compare Register B Low Byte 48 \$26(546) ICR1L Timer/Counter1 - Input Copure Register Low Byte 48 \$26(546) ICR1L Timer/Counter1 - Input Copure Register Low Byte 53 \$24(544) TCR1Z Timer/Counter2 (8 Bits) 53 \$23(543) OCR2A Timer/Counter2 (0 Bits) 53 \$24(544) TCN1Z Timer/Counter2 (0 Bits) 57 \$21(541) VDTCR - - AS2 TCN2UB OCR2UB TCN2UB 57 \$21(543) UBRRHI - - - UBRRHI - - 100000 000000 0000000 0000000000 000000000000000000000000000000000000											
\$29.(54) OCR1BH Timer/Counter1 - Output Compare Register 1 Map Byte 47 \$28.(548) OCR1BL Timer/Counter1 - Input Capture Register Low Byte 47 \$26.(546) ICR1L Timer/Counter1 - Input Capture Register Low Byte 48 \$26.(546) ICCR2 FOC2 PVM2 COM20 CTC2 CS21 CS20 52 \$24.(541) Timer/Counter2 (6 Bits) - - - AS2 TCN2UB OCR2UB TCR2UB 57 \$21.(541) WDTCR - - - WDTCE WDP1 WDP0 60 \$20.(540) UBRR1H -<											
\$27(\$47) ICR1H Timer/Counter1 - Input Capture Register High Byte 48 \$26(\$46) ICR1L Timer/Counter2 (B Bits) 648 \$24(\$44) TCNT2 Timer/Counter2 (B Bits) 53 \$24(\$44) TONT2 Timer/Counter2 (D Bits) 53 \$24(\$44) TONT2 Timer/Counter2 (D Bits) 53 \$23(\$43) OCR2 Timer/Counter2 (D Bits) 54 \$24(\$42) ASSR - - - AS2 TCN2UB OCR2UB TCR2UB 57 \$21(\$41) WDTCR WDTCE WDP2 WDP2 WDP1 WDP0 60 \$20(\$40) UBRRH1 - - - WDTCE WDE WDP2 WDP1 WDP0 60 \$21(\$41) WDTCR WD WDTCE WDE WDP2 WDP1 62 21 51 53 51 53 51 53 51 53 51 53 53 53 53 53 53 53 53 53 53 53 53 53 53 53 53	\$29 (\$49)	OCR1BH									
S26 (546) ICR1L Timer/Counter1 - Input Capture Register Low Byte 53 <td>\$28 (\$48)</td> <td>OCR1BL</td> <td>Timer/Count</td> <td>ter1 – Output C</td> <td>ompare Regist</td> <td>er B Low Byte</td> <td></td> <td></td> <td></td> <td></td> <td>47</td>	\$28 (\$48)	OCR1BL	Timer/Count	ter1 – Output C	ompare Regist	er B Low Byte					47
S25 (S45) TCCR2 FOC2 PWM2 COM21 COM20 CTC2 CS22 CS21 CS20 52 S24 (S44) TCNT2 Timer/Counter2 (B Bits) 53 53 53 S23 (S43) OCR2 Timer/Counter2 (Duput Compare Register 54 53 S21 (S41) MOTCE - - - - 54 S22 (S42) ASSR - - - - AS2 TCN2UB CCR2UB TCR2UB 57 S21 (S41) WDTCR - - - - - - EEARH - 78 S20 (S40) UBRRHI - - - - - EEARB EEAR1 EEAR1 EEAR1 EEAR1 - - EEAR1	\$27 (\$47)	ICR1H	Timer/Count	ter1 – Input Ca	pture Register I	High Byte					48
\$24 (\$44) TCNT2 Timer/Counter2 (8 lits) 53 \$23 (\$43) OCR2 Timer/Counter2 Output Compare Register 54 \$22 (\$42) ASSR - - - AS2 \$21 (\$41) WDTCR - - - WDTE WDP0 60 \$21 (\$41) WDTCR - - - WDTE WDP1 WDP0 60 \$21 (\$41) WDTCR - - - - UBRRHI - 78 \$20 (\$40) UBRRHI -	\$26 (\$46)		Timer/Count	ter1 – Input Ca	pture Register I	_ow Byte					
\$23 OCR2 Timer/Counter/2 Output Compare Register 54 \$22 (\$42) ASSR - - - AS2 TCN2UB OCR2UB TCR2UB 57 \$21 (\$41) WDTCR - - - WDTC WDP2 WDP1 WDP0 60 \$20 (\$40) UBRRHI - - - - UBR(118) 78 \$21 (\$41) WDTCR - - - - EEARB 62 \$15 (\$35) EEAR EEARA EEAR6 EEAR5 EEAR4 EEAR3 PORTA1 PORTA1 PORTA2 PORTA4 PORTA3 PORTA2 PORTA1 PORTA0 115 \$16 (\$30) DDRA DDA7 DDA4 DDA1 DDA0 115 \$16 (\$30) PORTB PORTB6 PORTB5 PORTB3 PORTB3 PORTB2 PORTB1 PORTB0 117 \$16 (\$38) PINB PINB7 PINB6 PINB5 PINB4 PINB3 PINB1 PINB0	\$25 (\$45)				COM21	COM20	CTC2	CS22	CS21	CS20	52
S22 (S42) ASSR - - - AS2 TCN2UB OCR2UB TCR2UB 57 S21 (S41) WDTCR - - - WDT0E WDP2 WDP1 WDP0 60 S20 (S40) UBRRI11 - - - - UBRRI113 78 S1F (S35) EEARH - - - - - - EEAR8 62 S1G (S30) EEDR EERRM E EEAR1 EEAR0 62 S1G (S3C) EECR EECR FEAR4 PORTA7 PORTA6 PORTA7 PORTA6 PORTA7 PORTA6 PORTA5 PORTA1 PORTA2 PORTA1 DDA0 115 S16 (S30) PINA PINA5 PINA4 PINA3 PINA2 PINA1 PINA0 1115 S16 (S30) PORTB PORTB7 PORTB6 PORTB5 PORTB4 PORTB2 PORTB1 PORTB0 1117 S16 (S30) PINB PINB6 PINB5			Timer/Count	ter2 (8 Bits)							
\$21 (\$41) WDTCR - - - WDTOE WDE WDP2 WDP0 60 \$20 (\$40) UBRRHI - - - UBRR[11:3] 78 \$1F (\$3F) EEARH - - - - - EEAR8 62 \$1F (\$3F) EEARL EEAR1 EEAR6 EEAR8 EEAR3 EEAR3 EEAR3 EEAR4 EEAR3 EEAR3 EEAR4 PORTA3 PORTA1 PORTA0 115 \$18 (\$38) PORTA PORTA7 PORTA6 PORTA5 PORTA4 PORTB3 PORTB1 PORTB0 1115 \$18 (\$39) PINA PINA7 PINA6 PINA5 PINA14 PINA3 PINA3 PINA3 PINA14 PINA3 PINA3 PINA3 PINA3 PINA3 PINA3 PINA3 PINA3 PINA14 PINA3 PINA3			Timer/Count	ter2 Output Co	mpare Register		1	1	r		
\$20 (940) UBRRHI - - - - UBR(11:8) 78 \$1F (\$3F) EEARH - - - - EARB 62 \$1F (\$3F) EEARL EEAR EEAR7 EEAR6 EEAR5 EEAR3 EEAR2 EEAR1 EEAR0 62 \$10 (\$3D) EEDR EEPROM Data Register - - - 62 \$11 (\$3A) PORTA PORTB PORTB PORTB PORT			-	-	-	-					
\$1F (\$3F) EEARL - - - - - EEAR3			-	-	-	WDTOE	WDE			WDP0	
STE (\$3E) EEARL EEAR1 EEAR2 EEAR3 EEAR3 EEAR2 EEAR1 EEAR1 62 \$1D (\$3D) EEDR EEPROM Data Register 62 62 \$1D (\$3C) EECR - - - EERIE EEMWE EEWE EERE 63 \$1B (\$3B) DORA DORA DORA PORTA6 PORTA5 PORTA4 PORTA2 PORTA1 PORTA0 115 \$14 (\$3A) DDRA DDA7 DDA6 DDA5 PORTB4 PORTB2 PORTB0 117 \$19 (\$39) PINA PINA7 PINA6 PINA5 PINA4 PINA3 PINA2 PINA1 PINA0 115 \$18 (\$38) PORTB PORTB7 PORT66 PORT55 PORTB3 PORT2 PORTB1 PORTB0 117 \$16 (\$36) PINC PINC7 PINC6 PINC5 PORTC4 PORTC3 PORTC2 PORTC1 PORT00 123 \$16 (\$33) PINC PINC7 PINC6 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>R[11:8]</td> <td></td> <td></td>									R[11:8]		
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	\$03 (\$23)		Two-wire Se	erial Interface [Data Register						84
\$01 (\$21) TWSR TWS7 TWS6 TWS5 TWS4 TWS3 84										TWGCE	
	\$01 (\$21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	-	-	84

Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$00 (\$20)	TWBR	Two-wire Se	wo-wire Serial Interface Bit Rate Register 82							
Note: 1. F	Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses									

 For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.





Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AN	D LOGIC INSTRUC	TIONS			•
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd ullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \lor Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \lor K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow FF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd x Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd x Rr) << 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd x Rr) << 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) << 1$	Z,C	2
BRANCH INSTRU		Tractional multiply Signed with Onsigned	$K1.K0 \leftarrow (K0XK1) \smallsetminus T$	2,0	2
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP	ĸ		$PC \leftarrow PC + K + 1$ $PC \leftarrow Z$	None	2
JMP	k	Indirect Jump to (Z) Direct Jump	$PC \leftarrow Z$ $PC \leftarrow k$	None	3
RCALL	k				3
	к	Relative Subroutine Call	$\frac{PC \leftarrow PC + k + 1}{PC \leftarrow Z}$	None	
ICALL	1.	Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return		None	4
RETI	D I D	Interrupt Return	$PC \leftarrow STACK$		4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC \leftarrow PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC \leftarrow PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC \leftarrow PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC \leftarrow PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC \leftarrow PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC \leftarrow PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
	k	Branch if Minus	if (N = 1) then PC \leftarrow PC + k + 1	None	1/2
BRMI	k	Branch if Plus	if (N = 0) then PC \leftarrow PC + k + 1	None	1/2
BRMI BRPL		Branch if Greater or Equal, Signed	if (N \oplus V= 0) then PC \leftarrow PC + k + 1	None	1/2
BRPL BRGE	k	Dianci il Ofeater of Equal, Olghed			
BRPL	k k	Branch if Less Than Zero, Signed	if (N \oplus V= 1) then PC \leftarrow PC + k + 1	None	1/2
BRPL BRGE			if $(N \oplus V= 1)$ then PC \leftarrow PC + k + 1 if $(H = 1)$ then PC \leftarrow PC + k + 1	None None	1/2
BRPL BRGE BRLT	k	Branch if Less Than Zero, Signed			
BRPL BRGE BRLT BRHS	k k	Branch if Less Than Zero, Signed Branch if Half Carry Flag Set	if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRPL BRGE BRLT BRHS BRHC	k k k	Branch if Less Than Zero, Signed Branch if Half Carry Flag Set Branch if Half Carry Flag Cleared Branch if T Flag Set	if (H = 1) then PC \leftarrow PC + k + 1 if (H = 0) then PC \leftarrow PC + k + 1 if (T = 1) then PC \leftarrow PC + k + 1	None None None	1/2 1/2
BRPL BRGE BRLT BRHS BRHC BRTS	k k k k	Branch if Less Than Zero, Signed Branch if Half Carry Flag Set Branch if Half Carry Flag Cleared	if (H = 1) then PC \leftarrow PC + k + 1if (H = 0) then PC \leftarrow PC + k + 1	None None	1/2 1/2 1/2

Instruction Set Summary (Continued)

BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if ($I = 0$) then PC \leftarrow PC + k + 1	None	1/2
DATA TRAN	SFER INSTRUCTIO	DNS			
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1$, $Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(1+q) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow \operatorname{Rr}, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q,Rr	Store Indirect with Displacement	$(Z+q) \leftarrow Rr$	None	2
		Store Direct to SRAM			2
STS	k, Rr		$(k) \leftarrow Rr$	None	
LPM	D 1 7	Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
	T-TEST INSTRUCTION	ONS		-	
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=06$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	S	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	S	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC	, ~	Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry		C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 1$ $Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable		<u> </u>	1
			↓ ← 1		
CLI		Global Interrupt Disable		1	1
		Set Signed Test Flag	<u>S ← 1</u>	S	1
	1	Clear Signed Test Flag	<u>S</u> ← 0	S	1
CLS			$V \leftarrow 1$	V	1
CLS SEV		Set Twos Complement Overflow.			
CLS SEV CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
CLS SEV CLV SET		Clear Twos Complement Overflow Set T in SREG	$V \leftarrow 0$ $T \leftarrow 1$	Т	1
SES CLS SEV CLV SET CLT		Clear Twos Complement Overflow	$V \leftarrow 0$		





Instruction Set Summary (Continued)

CLH	Clear Half Carry Flag in SREG	$H \leftarrow 0$	Н	1
NOP	No Operation		None	1
SLEEP	Sleep	(see specific descr. for Sleep function)	None	1
WDR	Watchdog Reset	(see specific descr. for WDR/timer)	None	1

10 ATmega163(L) I

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
4	2.7 - 5.5V	ATmega163L-4AC	44A	Commercial
		ATmega163L-4PC	40P6	(0°C to 70°C)
		ATmega163L-4AI	44A	Industrial
		ATmega163L-4PI	40P6	(-40°C to 85°C)
8	4.0 - 5.5V	ATmega163-8AC	44A	Commercial
		ATmega163-8PC	40P6	(0°C to 70°C)
		ATmega163-8AI	44A	Industrial
		ATmega163-8PI	40P6	(-40°C to 85°C)

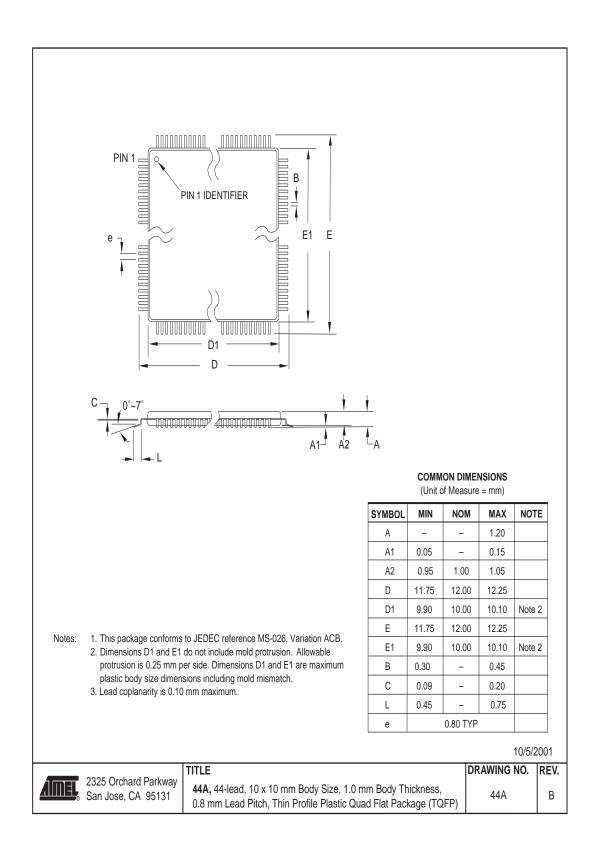
	Package Type					
44A	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)					
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)					



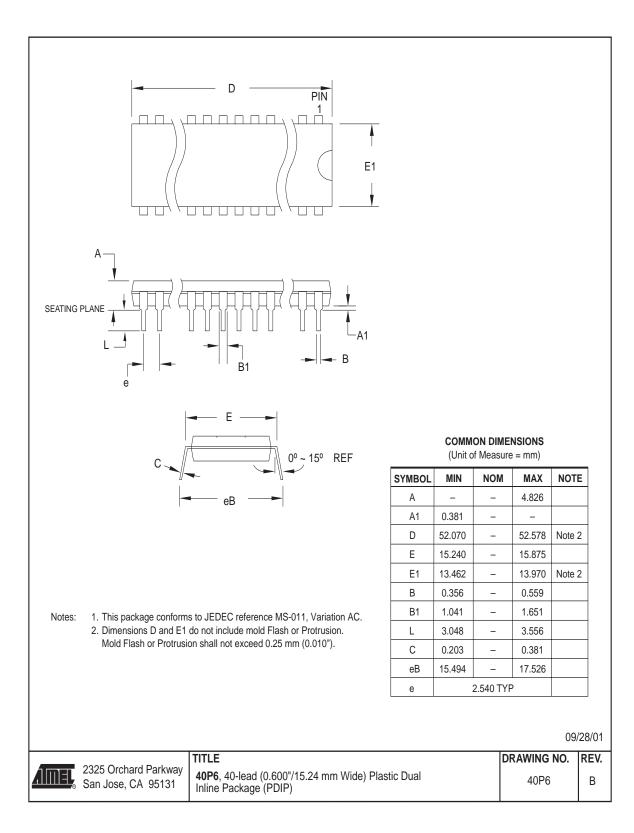


Packaging Information

44A











Erratas

ATmega163(L) Errata Rev. F

- Increased Interrupt Latency
- Interrupts Abort TWI Power-down
- TWI Master Does not Accept Spikes on Bus Lines
- TWCR Write Operations Ignored
- PWM not Phase Correct
- TWI is Speed Limited in Slave Mode

6. Increased Interrupt Latency

In this device, some instructions are not interruptable, and will cause the interrupt latency to increase. The only practical problem concerns a loop followed by a twoword instruction while waiting for an interrupt. The loop may consist of a branch instruction or an absolute or relative jump back to itself like this:

loop: rjmp loop

<Two-word instruction>

In this case, a dead-lock situation arises.

Problem Fix/Workaround

In assembly, insert a nop instruction immediately after a loop to itself. The problem will normally be detected during development. In C, the only construct that will give this problem is an empty "for" loop; "for(;;)". Use "while(1)" or "do{} while (1)" to avoid the problem.

5. Interrupts Abort TWI Power-down

TWI Power-down operation may be aborted by other interrupts. If an interrupt (e.g., INT0) occurs during TWI Power-down address watch and wakes the CPU up, the TWI aborts operation and returns to its idle state.

Problem Fix/Workaround

Ensure that the TWI Address Match is the only enabled interrupt when entering Power-down.

4. TWI Master Does not Accept Spikes on Bus Lines

When the part operates as Master, and the bus is idle (SDA = 1; SCL = 1), generating a short spike on SDA (SDA = 0 for a short interval), no interrupt is generated, and the status code is still \$F8 (idle). But when the software initiates a new start condition and clears TWINT, nothing happens on SDA or SCL, and TWINT is never set again.

Problem Fix/Workaround

Either of the following:

- 1. Ensure that no spikes occur on SDA or SCL lines.
- 2. Receiving a valid START condition followed by a STOP condition provokes a bus error reported as a TWI interrupt with status code \$00.
- 3. In a Single Master systems, the user should write the TWSTO bit immediately before writing the TWSTA bit.

3. TWCR Write Operation Ignored

Repeated write to TWCR must be delayed. If a write operation to TWCR is immediately followed by another write operation to TWCR, the first write operation may be ignored.

Problem Fix/Workaround

Ensure at least one instruction (e.g., nop) is executed between two writes to TWCR.

2. PWM not Phase Correct

In Phase-correct PWM mode, a change from OCRx = TOP to anything less than TOP does not change the OCx output. This gives a phase error in the following period.

Problem Fix/Workaround

Make sure this issue is not harmful to the application.

1. TWI is Speed Limited in Slave Mode

When the two-wire Serial Interface operates in Slave mode, frames may be undetected if the CPU frequency is less than 64 times the bus frequency.

Problem Fix/Workaround

Ensure that the CPU frequency is at least 64 times the TWI bus frequency.





Change Log

Changes from Rev. 1142C-09/01 to Rev. 1142D-09/02

Changes from Rev. 1142D-09/09 to Rev. 1142E-02/03 This section containes a log on the changes made to the data sheet for ATmega163. All refereces to pages in Change Log, are referred to this document.

- 1. Added "Not Recommend for New Designs. Use ATmega16.".
- 1. Updated Table 52, "Boot Reset Fuse," on page 136.
- 2. Corrected pin numbers in Figure 62 on page 113.
- 3. Corrected a constant in the Boot Loader code example on page 141.
- 4. Changed max bit rate for the TWI from 400 kHz to 217 kHz.
- 5. Removed redundant and harmful loop in a code example for Slave Receiver mode for the TWI on page 96.
- 6. Added AGND and AVCC in Figure 81 on page 145 and Figure 86 on page 154.
- 7. Updated the "Packaging Information" on page 12.
- 8. Added "Erratas" on page 14.





Atmel Headquarters

Corporate Headquarters 2325 Orchard Parkway San Jose, CA 95131 TEL 1(408) 441-0311 FAX 1(408) 487-2600

Europe

Atmel Sarl Route des Arsenaux 41 Case Postale 80 CH-1705 Fribourg Switzerland TEL (41) 26-426-5555 FAX (41) 26-426-5500

Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimhatsui East Kowloon Hong Kong TEL (852) 2721-9778 FAX (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan TEL (81) 3-3523-3551 FAX (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway San Jose, CA 95131 TEL 1(408) 441-0311 FAX 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway San Jose, CA 95131 TEL 1(408) 441-0311 FAX 1(408) 436-4314

La Chantrerie BP 70602 44306 Nantes Cedex 3, France TEL (33) 2-40-18-18-18 FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle 13106 Rousset Cedex, France TEL (33) 4-42-53-60-00 FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 TEL 1(719) 576-3300 FAX 1(719) 540-1759

Scottish Enterprise Technology Park Maxwell Building East Kilbride G75 0QR, Scotland TEL (44) 1355-803-000 FAX (44) 1355-242-743

RF/Automotive

Theresienstrasse 2 Postfach 3535 74025 Heilbronn, Germany TEL (49) 71-31-67-0 FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 TEL 1(719) 576-3300 FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom Avenue de Rochepleine BP 123 38521 Saint-Egreve Cedex, France

TEL (33) 4-76-58-30-00 FAX (33) 4-76-58-34-80

e-mail

literature@atmel.com

Web Site http://www.atmel.com

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