Features

- ESD Protect for 4 high-speed I/O lines and one VDD line
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±15kV (air/contact)
  IEC 61000-4-4 (EFT) 50A (5/50ns)
  IEC 61000-4-5 (Lightning) 5A (8/20μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V etc.
- Low capacitance : 1.0pF typical
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Back-drive protection for power-down mode
- Small SOT363 package saves board space
- ***Green part***

Applications

- **Video Graphics Cards**
- **Digital Visual Interface (DVI)**
- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays

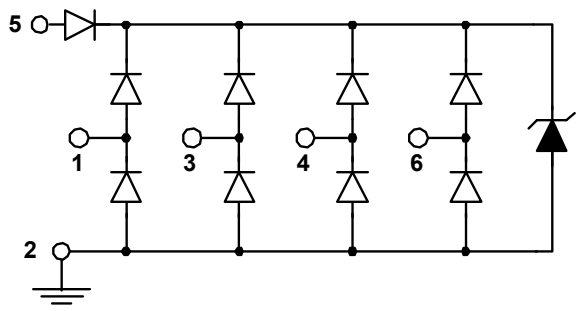
Description

AZC199-04C is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZC199-04C has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

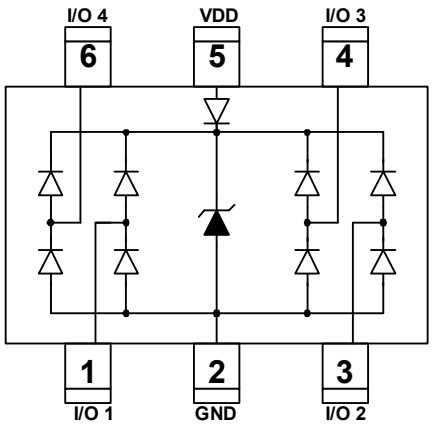
AZC199-04C is a unique design which includes ESD rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. Besides, there is a back-drive protection design in AZC199-04C for power-down mode operation.

AZC199-04C may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



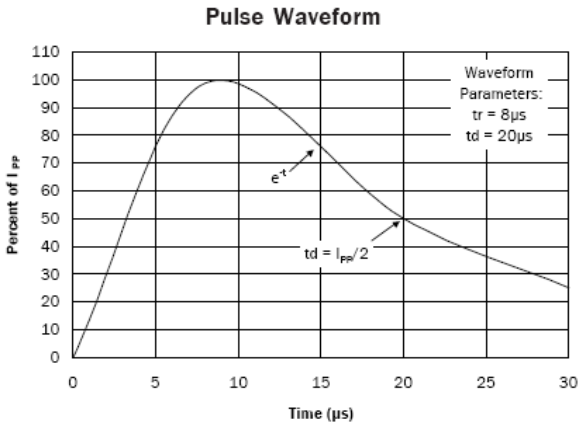
SC70-6L (Top View)
(SOT-363)

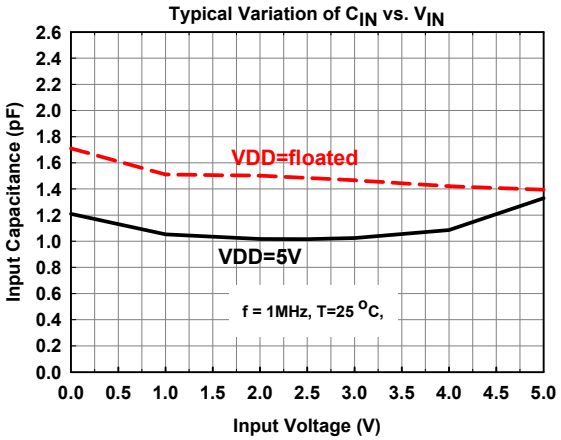
SPECIFICATIONS

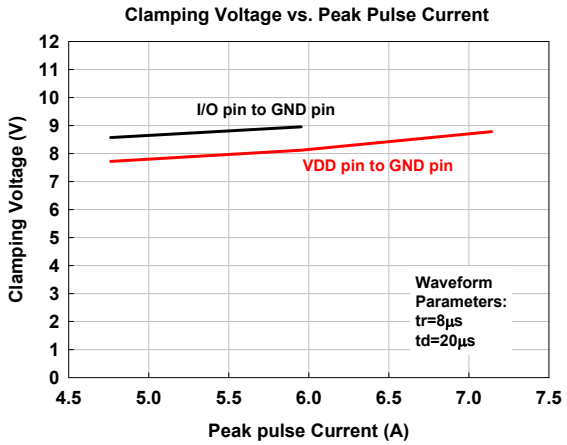
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs) (I/O pins)	I_{PP}	5	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air/Contact)	V_{ESD}	15	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

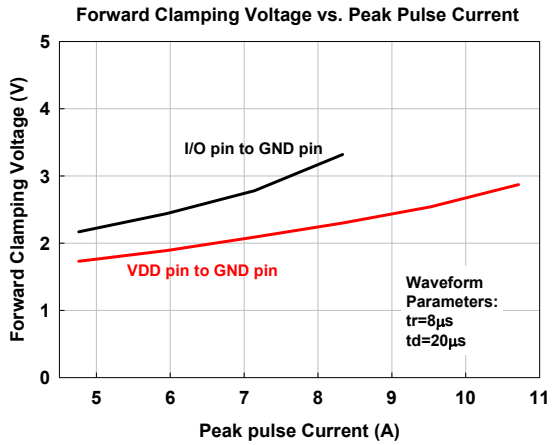
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	**μA**
Channel Leakage Current	$I_{CH-Leak}$	V_{Pin5} = 5V, V_{Pin2} = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin 5 to Pin 2	6		9	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, Pin 2 to Pin 5		0.85	1	**V**
ESD Clamping Voltage –I/O	V_{clamp_io}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		11		**V**
ESD Clamping Voltage –VDD	V_{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		9.5		**V**
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic\_io}$	IEC 61000-4-2 0~+6kV,T=25 °C, Contact mode, any Channel pin to Ground		0.3		**Ω**
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.15		**Ω**
Lightning Clamping Voltage	$V_{lightning\_io}$	I_{PP}=5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		8.5		**V**
Lightning Clamping Voltage	$V_{lightning\_VDD}$	I_{PP}=5A, tp=8/20μs, T=25 °C VDD pin to Ground		7.7		**V**
Channel Input Capacitance -1	C_{IN-1}	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, Any Channel pin to Ground		1.0	1.2	**pF**
Channel Input Capacitance - 2	C_{IN-2}	**V_{pin5}=floated**,V_{pin2}=0V,**V_{IN}=2.5V**,f=1MHz, T=25°C,Any Channel pin to Ground		1.5	1.8	**pF**
Channel to Channel Input Capacitance -1	$C_{CROSS-1}$	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Between Channel pins		0.15	0.2	**pF**
Channel to Channel Input Capacitance -2	$C_{CROSS-2}$	**V_{pin5} =floated**,V_{pin2} =0V,**V_{IN} =2.5V**,f =1MHz,T=25 °C,Between Channel pins		0.18	0.23	**pF**
Variation of Channel Input Capacitance -1	$\triangle C_{IN-1}$	**V_{pin5} =5V**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.08	0.1	**pF**
Variation of Channel Input Capacitance -2	$\triangle C_{IN-2}$	**V_{pin5} =floated**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.06	0.08	**pF**

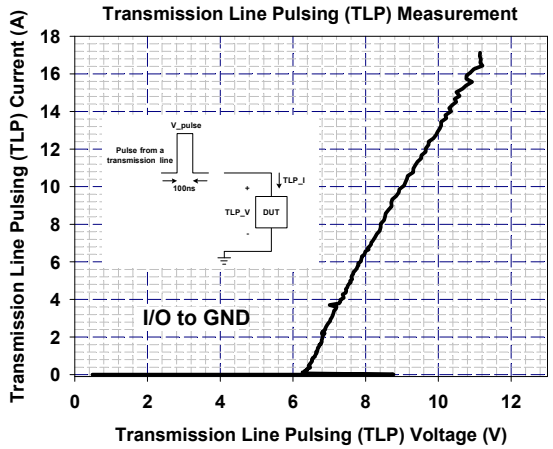
Typical Characteristics

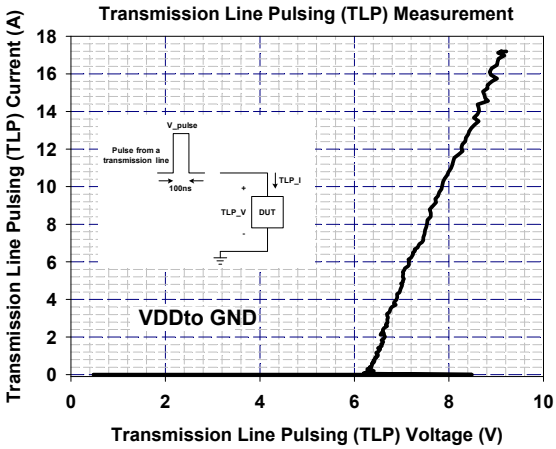












Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + Breakdown voltage drop of D3 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZC199-04C has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

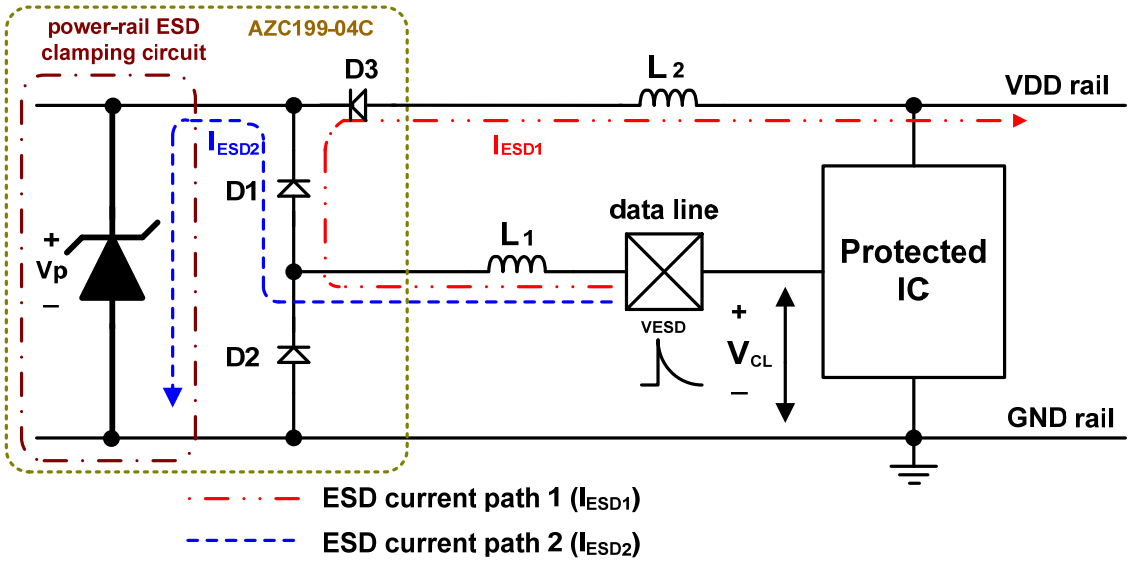


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZC199-04C is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZC199-04C is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZC199-04C. The ground pin (pin2) of AZC199-04C is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZC199-04C is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZC199-04C.

AZC199-04C can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZC199-04C.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZC199-04C can be left as floating. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

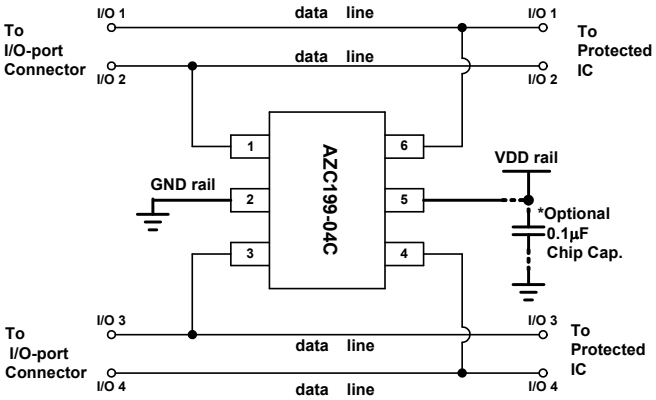


Fig. 2 Data lines and power rails connection of AZC199-04C.

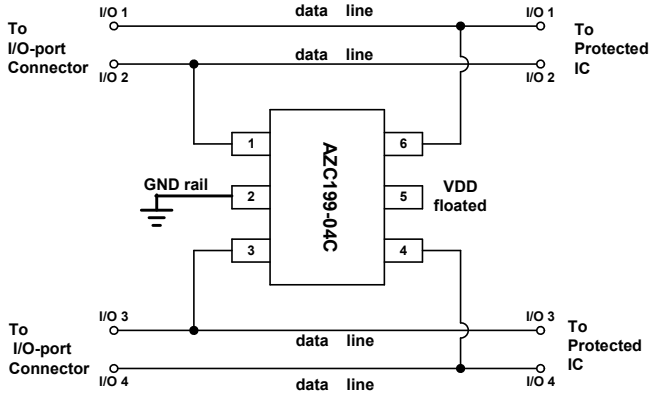


Fig. 3 Data lines and power rails connection of AZC199-04C. VDD pin is left as floating when no power rail presented on the PCB.

C. Application

AZC199-04C is designed for protecting high speed I/O ports from very high over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZC199-04C, especially, the VGA and DVI ports with the ESD spec. of contact-15kV, Class-C above.

The VGA Output Port

Fig. 4 shows the schematic of ESD protection design for a VGA output port on a host system, (e.g. the source, such as MB, NB, Media player…), where two AZC199-04C are used. The AZC199-04C has been integrated with back-drive protection diode for preventing the back-drive current to occur. Thus, no extra BAV70 for preventing the back-drive current to occur is needed.

The back-drive current occurs as shown in Fig, 5. When the source stays at OFF state, at the source connector, the VGA5V pin was wished to be at zero potential. At this moment, if without the integrated back-drive current protection diode, the display device stays at ON state, and the pulled high signals will produce a current back drive to the source's VGA5V power plate as shown in Fig. 5. This back drive current may make VGA5V be not at zero potential, which may lead system to an abnormal state. Therefore, it should be eliminated, and the integrated back-drive protection diode can eliminate this current.

The VGA Input Port

In contrast with the design for a VGA output port, the schematic of ESD protection design for a VGA input port on a display system is shown in Fig. 6. In most of VGA input circuit designs, there are always two power supplies, one is from the connector's DSUB-5V pin which potential comes from another VGA output port, the other is from the own power supply circuit of the VGA input port, system 5V. The VDD pin of AZC199-04C is directly connected to the connector's DSUB-5V pin to block the ESD event which comes from the DSUB-5V pin.

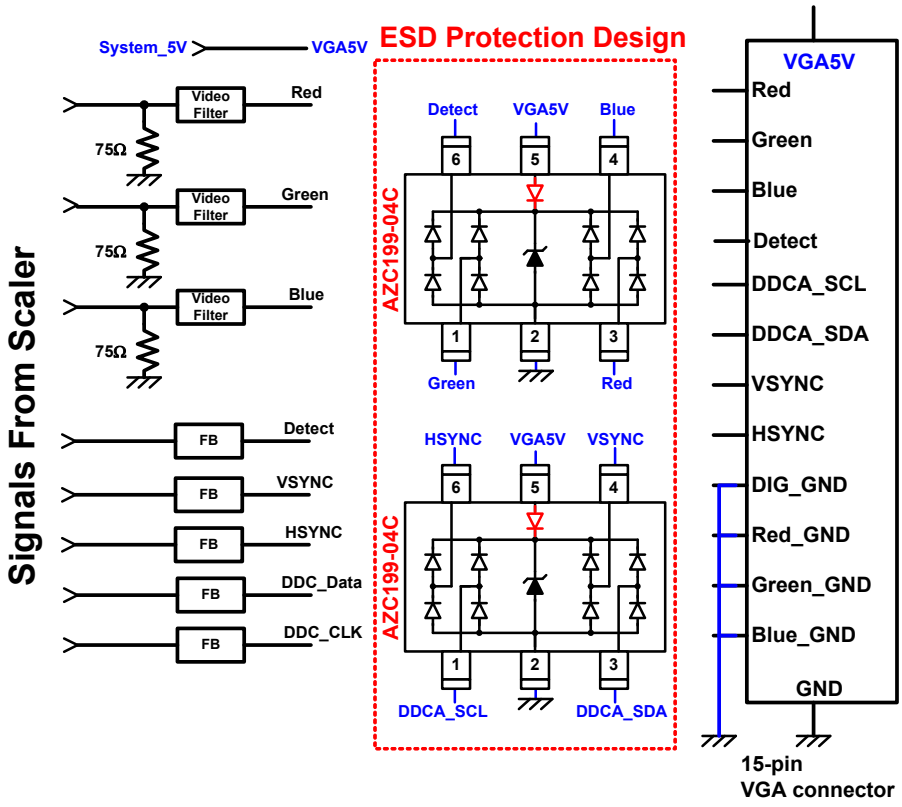


Fig. 4 The ESD design for a VGA *OUTPUT* port which two AZC199-04C are used.

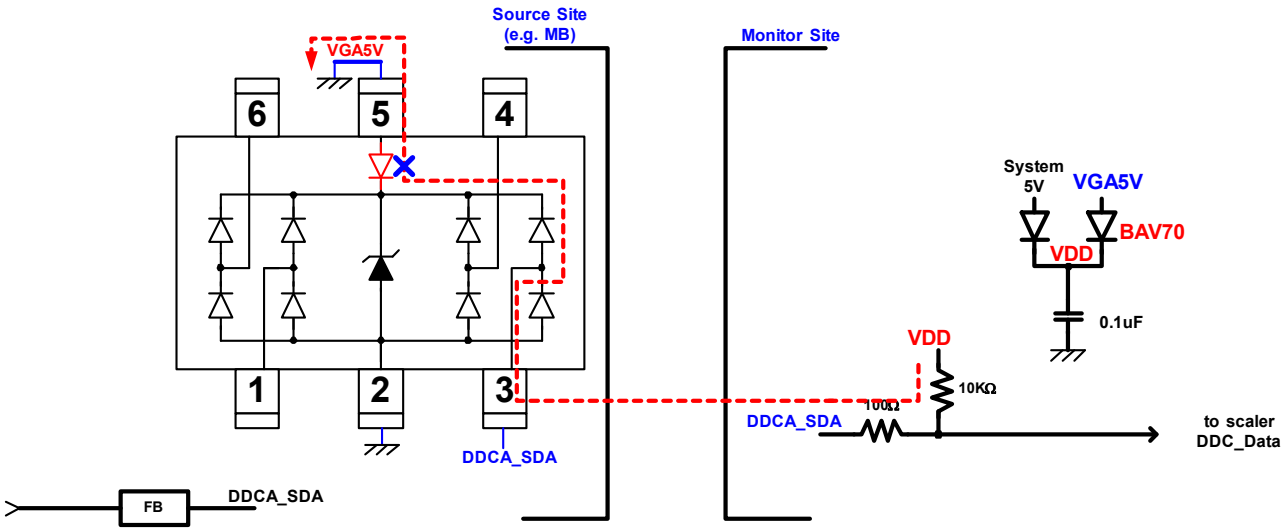


Fig. 5 The occurred back drive current when the source is at OFF state and the display device is at ON state.

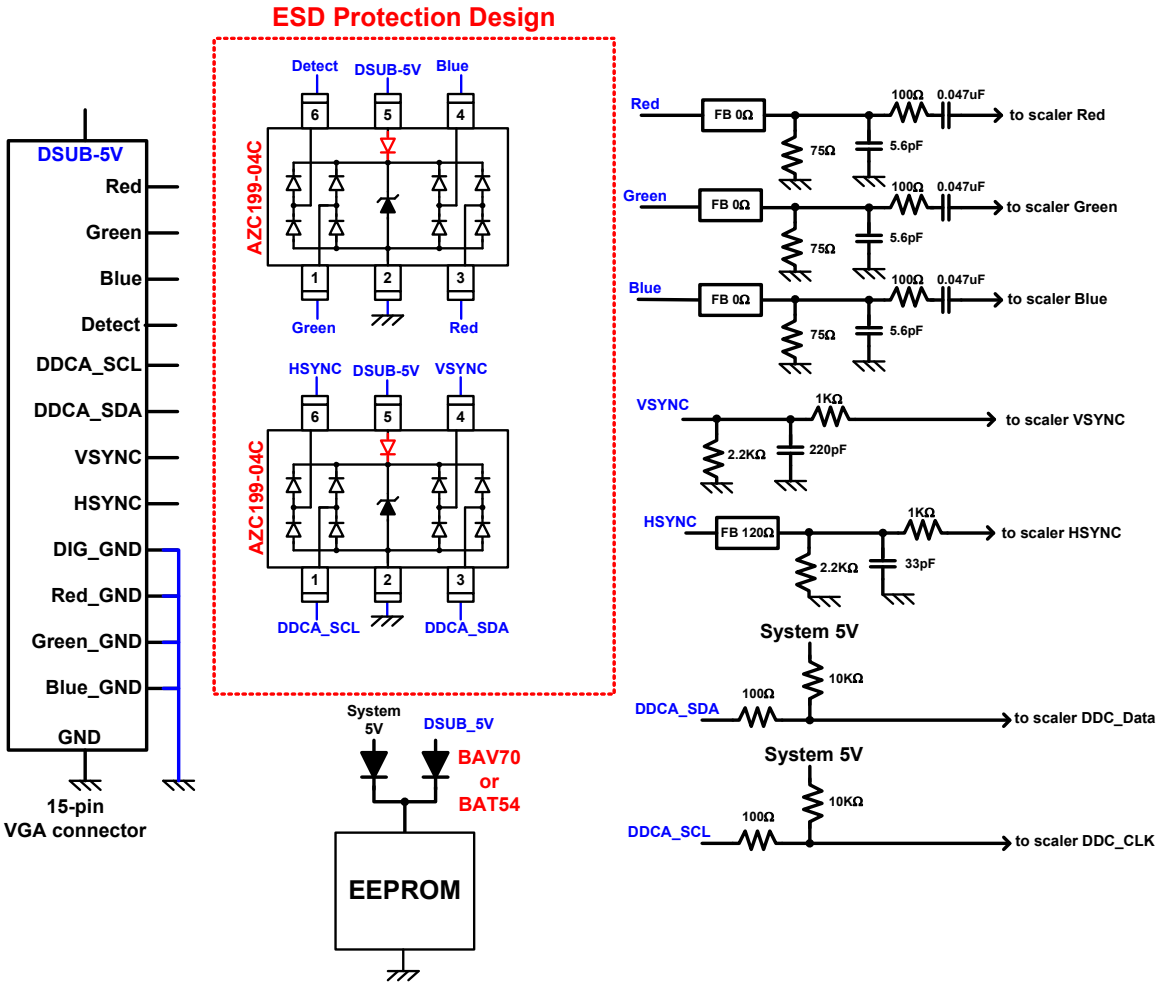


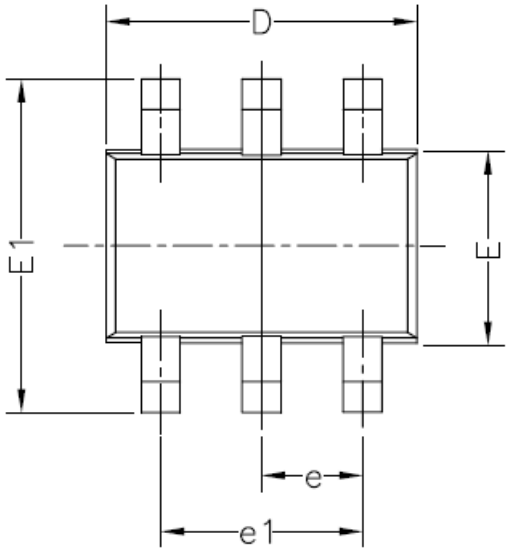
Fig. 6 The ESD design for a VGA *INPUT* port which two AZC199-04C are used.

Mechanical Details

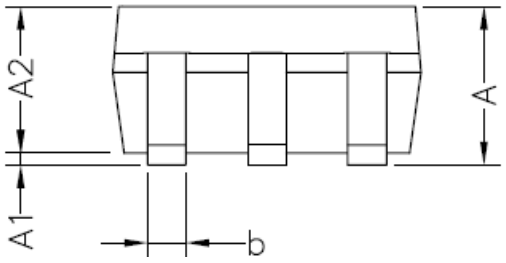
SC70-6L (SOT363)

PACKAGE DIAGRAMS

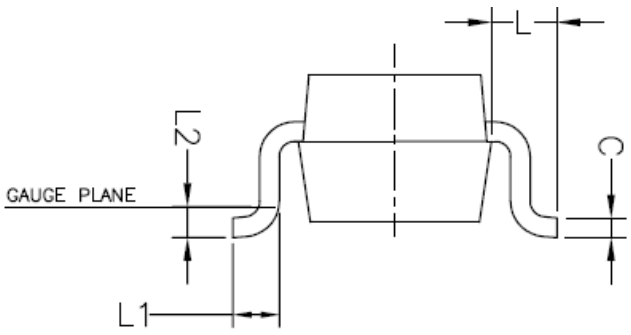
TOP VIEW



SIDE VIEW



END VIEW

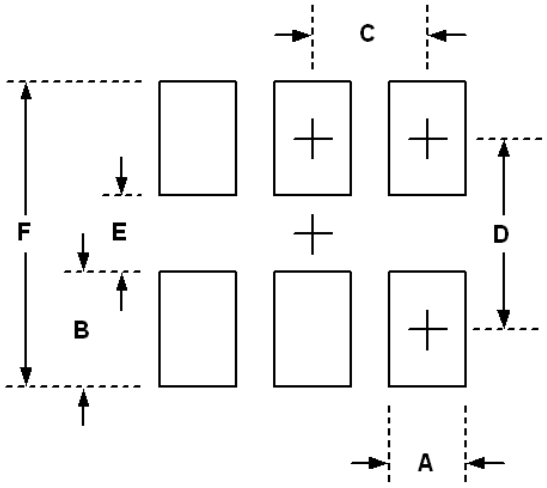


PACKAGE DIMENSIONS

Symbol	Milimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.10	.036	.044
A1	0.025	0.10	.001	.004
A2	0.875	1.00	.035	.040
b	0.20	0.40	.008	.016
C	0.10	0.15	.004	.006
D	1.90	2.10	.076	.084
E	1.15	1.35	.046	.054
E1	2.00	2.20	.080	.088
e	0.65 BSC.		.026 BSC.	
e1	1.30 BSC.		.052 BSC.	
L	0.425 REF.		.017 REF.	
L1	0.300 REF.		.012 REF.	
L2	0.200 REF.		.007 REF.	

Note:
1.All dimensions are in millimeters, and the dimensions in inches are for reference only.
2.1mm=40mils=0.04inches

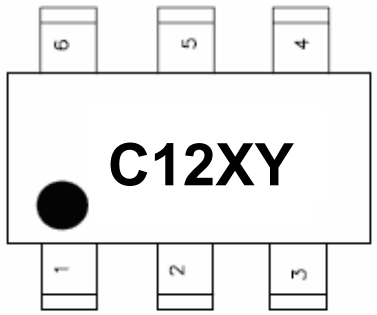
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.40	0.016
B	0.85	0.033
C	0.65	0.026
D	1.85	0.073
E	1.00	0.039
F	2.70	0.106

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



C12 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZC199-04C (Green part)	C12XY

Revision History

Revision	Modification Description
Revision 2010/02/10	Formal Release.