HT82V46
16-Bit, 45MSPS, 3-Channel CCD/CIS Analog Signal Processor

Features

- Operating voltage: 3.3V
- Guaranteed won't miss codes
- 9-bit programmable gain
- Correlated Double Sampling
- 8-bit programmable offset
- Programmable clamp voltage
- 8-bit wide multiplexed data output format
- 8-bit only output mode
- 4-bit multiplexed nibble mode
- Internal voltage reference
- Programmable 4-wire serial interface
- Maximum Conversation rate up to 45 MSPS
- 28-pin SSOP package

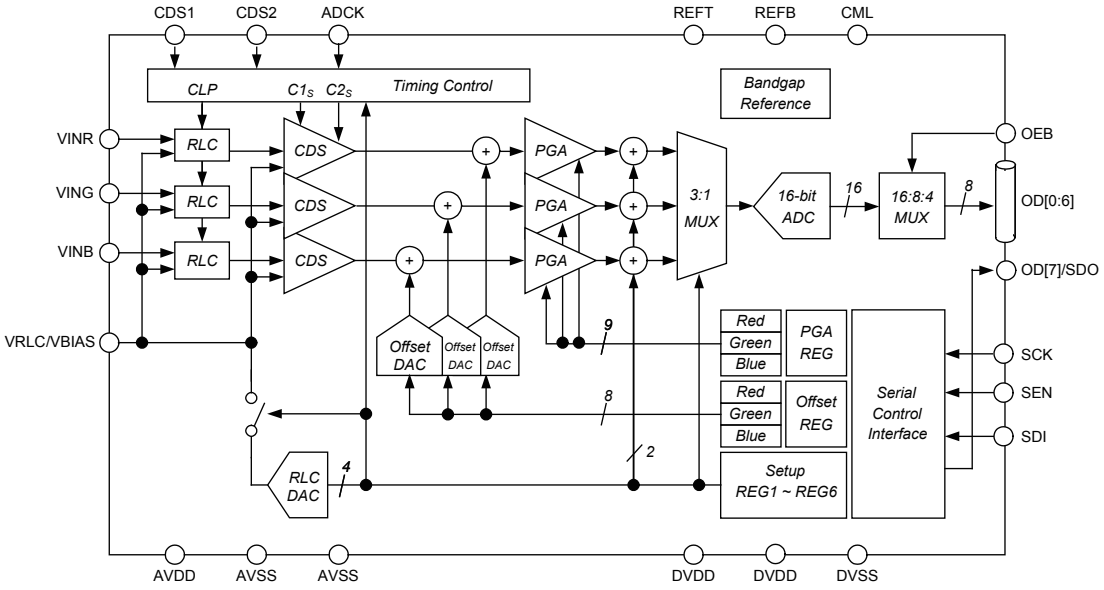
General Description

The HT82V46 is a complete analog signal processor for CCD imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of tri-linear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), and a high performance 16-bit A/D converter. The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS. The 16-bit digital output is available in 8-bit wide multiplexed format. The internal registers are programmed through a 4-wire serial interface, which provides gain, offset and operating mode adjustments. The HT82V46 operates from a single 3.3V power supply, typically consumes 528mW of power.

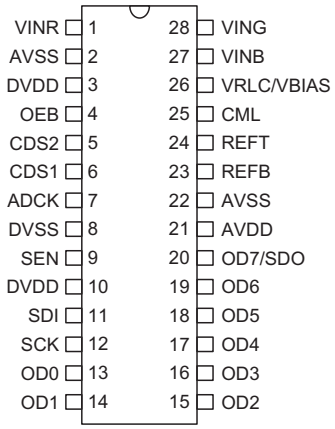
Applications

- Flatbed document scanners
- Film scanners
- Digital color copiers
- Multifunction peripherals

Block Diagram



Pin Assignment



HT82V46
28 SSOP-A

Pin Description

Pin Name	I/O	Description
VINR	AI	Analog Input, Red Channel
AVSS	P	Analog Ground
DVDD	P	Digital Driver Power
OEB	DI	Output Enable, Active Low
CDS2	DI	CDS Video Level Sampling Clock
CDS1	DI	CDS Reference Level Sampling Clock
ADCK	DI	ADC Sampling Clock
DVSS	P	Digital Driver Ground
SEN	DI	Serial Interface Enable, Active High
DVDD	P	Digital Driver Power
SDI	DI	Serial Data Input for Serial Control Interface
SCK	DI	Clock Input for Serial Control Interface
OD0~OD6	DO	Digital Data Output
OD7/SDO	DO	When register bit OEB= 0, OPD= 0 and SEN has been pulsed high, this pin use as Serial Data Output for Serial Control Interface. Otherwise, this pin use as Digital Data Output.
AVDD	P	Analog Supply
AVSS	P	Analog Ground
REFB	AO	ADC Bottom Reference Voltage Decoupling
REFT	AO	ADC Top Reference Voltage Decoupling
CML	AO	Internal Bias Level Decoupling
VRLC/VBIAS	AIO	Selectable analog output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.
VING	AI	Analog Input, Green Channel
VINB	AI	Analog Input , Blue Channel

TYPE: AI= Analog Input; AO= Analog Output; AIO=Analog In/out, DI= Digital Input; DO= Digital Output; P= Power.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS} -0.3V to V_{SS} +4.3V

Input Voltage ..... V_{SS} -0.3V to V_{DD} +0.3V

Storage Temperature ..... -50°C to 125°C

Operating Temperature .....0°C to 70°C

Analogue Supply Power .....3.0V to 3.6V

Digital Supply Power .....3.0V to 3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
AV_{DD}	Analogue Supply Power	—	3.0	3.3	3.6	V
DV_{DD}	Digital Supply Power	—	3.0	3.3	3.6	V
Digital Inputs						
V_{IH}	High Level Input Voltage	—	0.7*DV_{DD}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.2*DV_{DD}	V
I_{IH}	High Level Input Current	—	—	—	1	μA
I_{IL}	Low Level Input Current	—	—	—	1	μA
C_I	Input Capacitance	—	—	5	—	pF
Digital Outputs						
V_{OH}	High Level Output Voltage	I_{OH}= 1mA	DV_{DD}-0.5	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL}= 1mA	—	—	0.5	V
I_{OZ}	High Impedance Output Current	—	—	—	1	μA
Digital I/O Pins						
V_{IH}	Applied High Level Input Voltage	—	0.7*DV_{DD}	—	—	V
V_{IL}	Applied Low Level Input Voltage	—	—	—	0.2*DV_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH}=1mA	DV_{DD}-0.5	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL}=1mA	—	—	0.5	V
I_{IL}	Low Level Input Current	—	—	—	1	μA
I_{IH}	High Level Input Current	—	—	—	1	μA
I_{OZ}	High Impedance Output Current	—	—	—	1	μA

A.C. Characteristics

AV_{DD}=DV_{DD}=3.3V, AV_{SS}=DV_{SS}=0V, Ta=25°C, 3-channel mode, ADCK=45MHz unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Overall system specification (including 16-bit ADC, PGA, Offset and CDS functions)						
	Maximum Conversion Rate	—	—	45	—	MSPS
	Full-scale Input Voltage Range (See Note 1)	LOWREF= 0, G_{MAX}=7.5 typ.	—	0.25	—	V_{P-P}
		LOWREF= 0, G_{MIN}=0.65 typ.		3.03		V_{P-P}
	Full-scale Input Voltage Range (See Note 1)	LOWREF= 0, G_{MAX}=7.5 typ.	—	0.15	—	V_{P-P}
		LOWREF= 0, G_{MIN}=0.65 typ.		1.82		V_{P-P}
V_{IN}	Input Signal Limits (See Note 2)	—	AV_{SS}-0.3	—	AV_{DD}+0.3	V
	Full-scale Transition Error	Gain=0dB; PGA[8:0]=1A(hex)	—	30	—	mV
	Zero-scale Transition Error	Gain=0dB; PGA[8:0]=1A(hex)	—	30	—	mV
DNL	Differential Non-linearity	—	—	2	—	LSB
INL	Integral Non-linearity	—	—	50	—	LSB
	Channel to Channel Gain Matching	—	—	1.5	—	%
	Total Output Noise	Min Gain	—	30	—	LSB rms
		Max Gain		300		LSB rms
References						
V_{RT}	Upper Reference Voltage	LOWREF=0	1.95	2.05	2.25	V
		LOWREF=1		1.85		V
V_{RB}	Lower Reference Voltage	LOWREF=0	0.95	1.05	1.25	V
		LOWREF=1		1.25		V
CML	Input Return Bias Voltage	—	—	1.5	—	V
V_{RTB}	Diff. Reference Voltage (V_{RT} - V_{RB})	LOWREF=0	0.90	1.0	1.10	V
		LOWREF=1		0.6		V
RLC DAC (Reset-Level Clamp D/A Converter)						
	Resolution	—	—	4	—	bits
V_{CSTEP}	Step Size	CDACRNG=0	—	0.173	—	V/step
		CDACRNG=1		0.110		V/step
V_{CBOT}	Output Voltage at Code 0h	CDACRNG=0	—	0.4	—	V
		CDACRNG=1		0.4		V
V_{CTOP}	Output Voltage at Code Fh	CDACRNG=0	—	3.00	—	V
		CDACRNG=1		2.05		V
DNL	Differential Non-linearity	—	-0.5	—	+0.5	LSB
INL	Integral Non-linearity	—	—	+/-1	—	LSB
Offset DAC						
	Resolution	—	—	8	—	bits
	Step Size	—	—	2.04	—	mV/step
	Output Voltage	Code 00(hex)	—	-260	—	mV
		Code FF(hex)		+260		mV

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Programmable Gain Amplifier						
	Resolution	—	—	9	—	bits
	Gain Equation	—	0.66 + PGA[8:0] * 7.34 / 511			V/V
G_{MAX}	Max Gain, Each Channel	—	—	7.5	—	V/V
G_{MIN}	Min Gain, Each Channel	—	—	0.65	—	V/V
	Channel Matching	—	—	1	5	%
A/D Converter						
	Resolution	—	—	16	—	bits
	Speed	—	—	45	—	MSPS
	Full-scale Input Range $2*(V_{RT} - V_{RB})$	LOWREF=0	—	2.0	—	V
		LOWREF=1		1.2		V
Supply Currents						
	Total Supply Current	—	—	160	—	mA
	Analogue Supply Current	—	—	130	—	mA
	Digital Supply Current	—	—	30	—	mA
	Power Down Mode	—	—	130	—	μA

Note: 1. Full-scale input voltage denotes the peak input signal amplitude that can be gained to match the ADC full-scale input range.

2. Input signal limits are the limits within which the full-scale input voltage signal must lie.

Timing Specification

$AV_{DD}=DV_{DD}=3.3V$, $AV_{SS}=DV_{SS}=0V$, TA=25°C, ADCK=45MHz unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Clock Parameter						
t_{ADC}	ADCK Period	—	22	—	—	ns
t_{ADH}	ADCK High Period	—	10	11	—	ns
t_{ADL}	ADCK Low Period	—	10	11	—	ns
t_{C1}	CDS1 Pulse High	—	5	—	—	ns
t_{C2}	CDS2 Pulse High	—	5	—	—	ns
t_{C1FC2R}	CDS1 Falling to CDS2 Rising	—	0	—	—	ns
t_{ADFC2R}	ADCK Falling to CDS2 Rising	—	4	—	—	ns
t_{ADRC2R}	ADCK Rising to CDS2 Rising	—	2.5	—	—	ns
t_{ADFC2F}	ADCK Falling to CDS2 Falling	—	4	—	—	ns
t_{C2FADR}	CDS2 Falling to ADCK Rising [2]	—	1	—	—	ns
t_{ADFC1R}	1st ADCK Falling after CDS2 Falling to CDS1 Rising	—	1	—	—	ns
t_{PR3}	3-channel Mode Pixel Rate	—	66	—	—	ns
t_{PR2}	2-channel Mode Pixel Rate	—	44	—	—	ns
t_{PR1}	1-channel Mode Pixel Rate	—	22	—	—	ns
t_{OD}	Output Propagation Delay	—	—	8	12	ns
LAT	Output Latency. From 1st ADCK Rising Edge after CDS2 Falling to Data Output	—	—	7	—	ADCK periods

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Serial Control Interface						
t_{SCK}	SCK Period	—	83.3	—	—	ns
t_{SCKH}	SCK High	—	37.5	—	—	ns
t_{SCKL}	SCK Low	—	37.5	—	—	ns
t_{SDIS}	SDI Set-up Time	—	6	—	—	ns
t_{SDIH}	SDI Hold Time	—	6	—	—	ns
t_{CKFENR}	SCK Falling to SEN Rising	—	12	—	—	ns
t_{ENFCKR}	SEN Falling to SCK Rising	—	12	—	—	ns
t_{SEN}	SEN Pulse Width	—	60	—	—	ns
t_{ENFSD7}	SEN Falling to OD7/SDO Output the D7 of Register Data	—	—	—	30	ns
t_{CKFSD6}	SCK Falling to OD7/SDO Output the D6 of Register Data	—	—	—	30	ns
t_{CKFOD7}	SCK Falling to OD7/SDO Output OD7	—	—	—	30	ns

Note: 1. Parameters are measured at 50% of the rising/falling edge.

2. In 1-channel mode, if the CDS2 falling edge is placed more than 3ns before the rising edge of ADCK, the output amplitude of the HT82V46 will decrease.

Function Description

Introduction

The HT82V46 can sample up to three inputs, namely VINR, VING and VINB, simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level for signal processing. Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and a 9-bit Programmable Gain Amplifier (PGA). The ADC then converts each resulting analogue signal to a 16-bit digital word. The digital output from the ADC is presented on an 8-bit wide bus. On-chip control registers determine the configuration of the device, including the offsets and gains applied on each channel. These registers are programmable via a serial interface.

Internal Power-On-Reset (POR) Circuit

Internal POR Circuit is powered by AV_{DD} and used reset digital logic into a default state after power-up. POR active from $0.6V_{Typ.}$ of AV_{DD} and release at $1.2V_{Typ.}$ of AV_{DD} (or $0.7V_{Typ.}$ of DV_{DD} if AV_{DD} powered before DV_{DD}). And when AV_{DD} or DV_{DD} back to $0.6V_{Typ.}$ then POR will active again. To ensure the contents of the control registers are at their default values before carrying out any other register writes it is recommended software reset for every time power is cycled.

Power Management

The device default is fully enabled. The Register Bit EN allows the device to be fully powered down when set low. Individual blocks can be powered down using the bits in Setup Register 5. When in 1CH or 2CH mode the unused input channels are automatically disabled to reduce power consumption.

References

The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins REFT and REFB, where they must be decoupled to ground. Pin CML is driven by a similar buffer, and also requires decoupling. The output buffer from the RLCDAC also requires decoupling at pin VRLC/VBIAS.

CDS/Non-CDS Processing

For CCD type input signals, containing a fixed reference level, the signal may be processed using Correlated Double Sampling (CDS), which will remove pixel-by-pixel common mode noise. With CDS processing the input waveform is sampled at two different points in time for each pixel, once during the reference level and once during the video level. To sample using CDS, register bit CDS must be set to 1 (default). This causes the signal reference to come from the video reference level as shown in Figure 1. The video sample is always taken on the falling edge of the input CDS2 signal ($C2_S$). In CDS-mode the reference level is sampled on the falling

edge of the CDS1 input signal ($C1_S$). For input signals that do not contain a reference level (e.g. CIS sensor signals), non-CDS processing is used (CDS=0). In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS. The VRLC/VBIAS voltage is sampled at the same time as CDS2 samples the video level in this mode. In "WS" mode the input video signal is always sampled on the 1st rising edge of ADCK after CDS2 has gone low (Video Sample) regardless of the operating mode. If in non-CDS mode (CDS=0) the voltage on the VRLC/VBIAS pin is also sampled at this point. In CDS-mode (CDS=1) the position of the reference sample ($C1_S$) can be varied, under control of the CDSREF[1:0] register bits, as shown in Figure11.

Line-by-Line Operation

Certain linear sensors give colour output on a line-by-line basis. i.e. a full line of red pixels followed by a line of green pixels followed by a line of blue pixels. Often the sensor will have only a single output onto which these outputs are time multiplexed. The HT82V46 can accommodate this type of input by setting the LNBYLN register bit high. When in this mode the green and blue input PGAs are disabled to save power. The analogue input signal should be connected to the VINR pin. The offset and gain values that are applied to the Red input channel can be selected, by internal multiplexers, to come from the Red, Green or Blue offset and gain registers. This allows the gain and offset values for each of the input colours to be setup individually at the start of a scan. When register bit ACYC=0 the gain and offset multiplexers are controlled via the INTM[1:0] register bits. When INTM=00 the red offset and gain control registers are used to control the Red input channel, INTM=01 selects the green offset and gain registers and INTM=10 selects the blue offset and gain registers to control the Red input channel. When register bit ACYC=1, 'auto-cycling' is enabled, and the input channel switches to the next offset and gain registers in the sequence when a pulse is applied to the CDS1 input pin. The sequence is Red → Green → Blue → Red… offset and gain registers applied to the single input channel. A write to the Auto-cycle reset register (address 05h) will reset the sequence to a known state (Red registers selected). When auto-cycling is enabled, the CDS1 pin cannot be used to control reset level clamping. The CLPCTL bit may be used instead (enabled when high, disabled when low).

When auto-cycling is enabled, the CDS1 pin cannot be used for reference sampling (i.e. CDS must be set to 0).

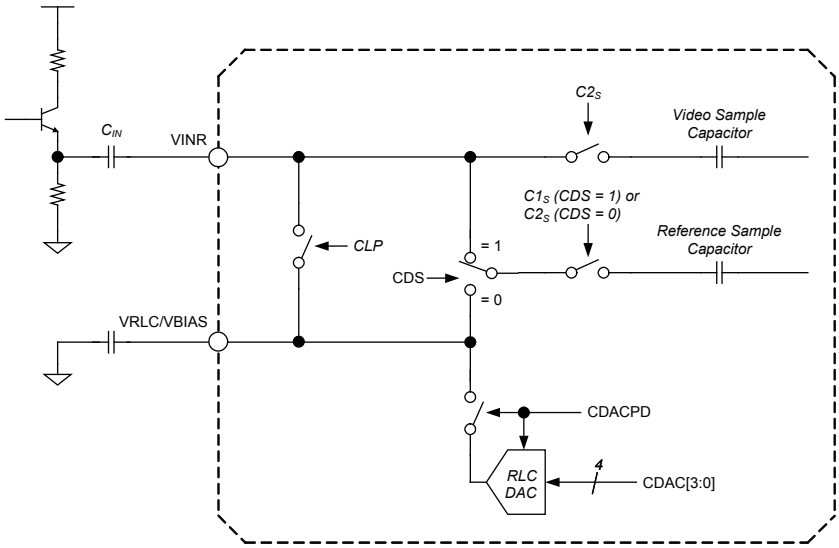


Figure 1 CDS/non-CDS Input Configuration

Analog Input Signal Sampling

There are "NM" and "WS" two operating modes of HT82V46. It can be selected by register bit WS.

"NM" Mode (WS=0; Normal Mode)

The ADCK speed can be specified along with the ADCK:CDS2 ratio to achieve the desired sample rate as table 1.

"NM" Mode Timing Diagram

See Figure 2 , Figure 3 and Figure 4.

"WS" Mode (WS=1)

It requires double rate ADCK and pixel rate CDS2 input. CDS1 pin performs same function as RLC/ ACYC pin.

A programmable detect circuit allows the sampling point derived from CDS2 pin. When set C2DET to 1, the circuit detects either a rising or falling edge (determined by C2POS control bit) on the CDS2 input pin and generates an internal *INTC2* pulse. When C2POS=1, a positive edge transition is detected and when C2POS=0, a falling edge transition is detected. *INTC2* can optionally be delayed by a number of ADCK periods, specified by the C2DLY[2:0] bits. Figure 5 shows the sampling point occurs on the first rising ADCK edge after this internal CDS2 pulse.

"WS" Mode Timing Diagram

See Figure 6 , Figure 7, Figure 8 and Figure 9.

ADCK: 45MHz; CDS: available

ADCK:CDS2	Max. Sample Rate (MSPS)	Register Bit			R/G/B of PGA			Mode
		1CH	2CH	CH[1:0]	Red	Green	Blue	
3:1	15	0	0	XX	V_1	V_1	V_1	3-channel
2:1	22.5	0	1	XX	V_1	V_1	X_1	2-channel
1:1	45	1	0	00	V_1	X_1	X_1	1-channel
				01	X_1	V_1	X_1	
				10	X_1	X_1	V_1	
—	—	1	0	11	—	—	—	Invalid
—	—	1	1	XX	—	—	—	Invalid
Where X_1 : Disable; V_1 : Enable								

Table 1 "NM" Operating Modes

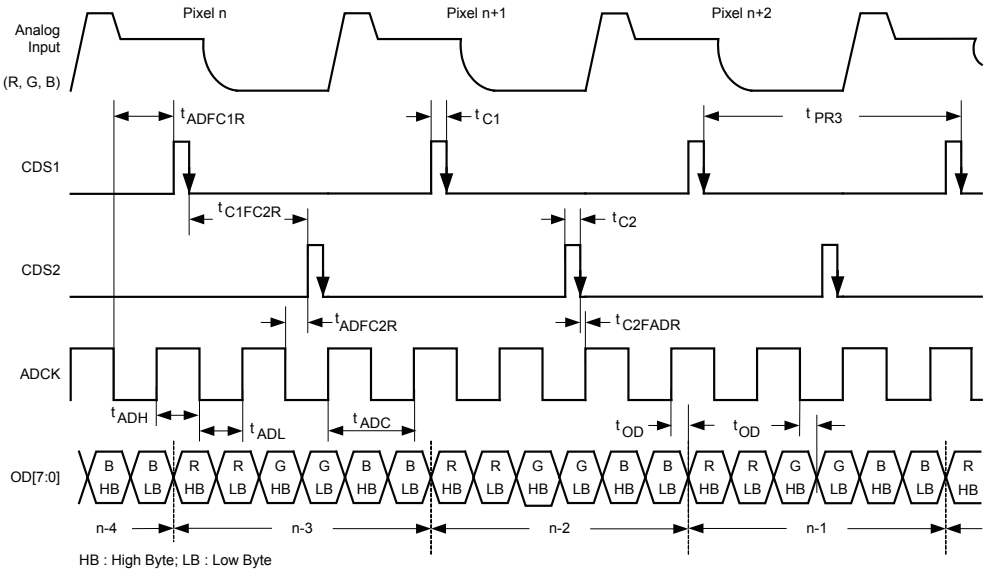


Figure 2 3-channel CDS Analog Input Timing

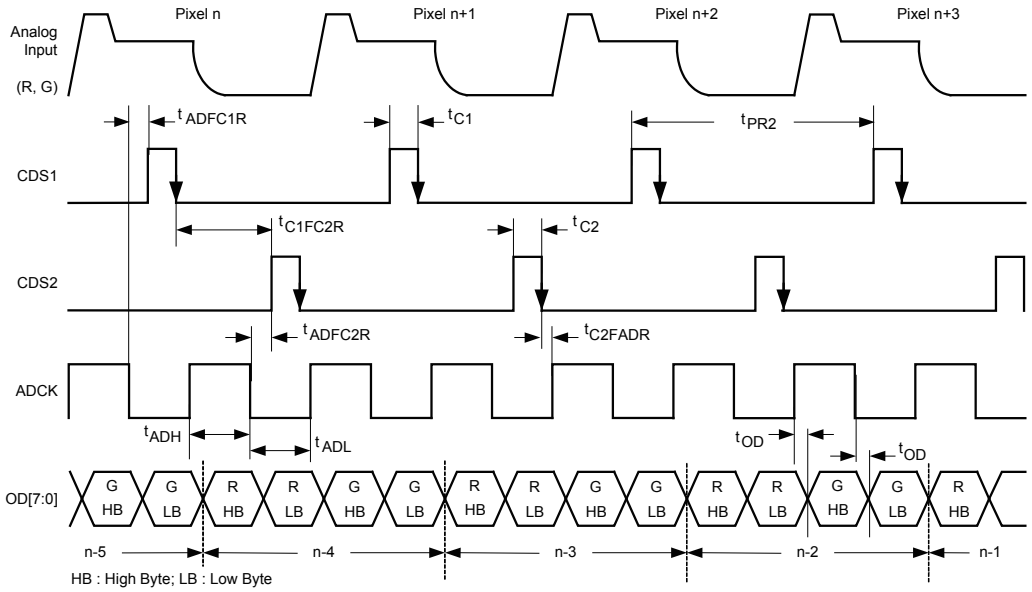


Figure 3 2-channel CDS Analog Input Timing

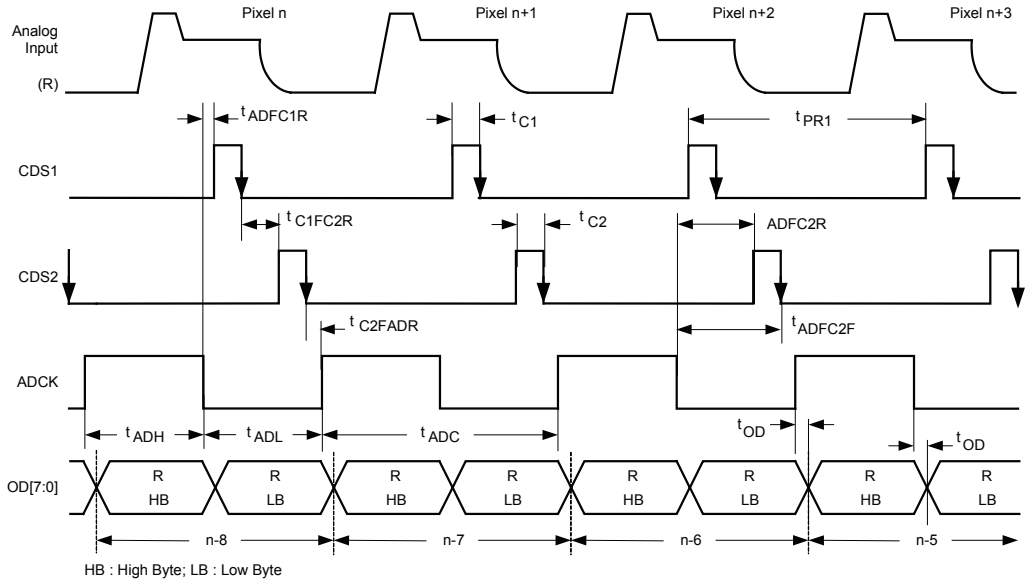


Figure 4 1-channel CDS Analog Input Timing

Note: 1. The relationship between input video and sampling is controlled by CDS2 and CDS1.

2. When CDS2 is high the input video signal is connected to the Video level sampling capacitors.

3. When CDS1 is high the analog input video signal is connected to the Reference level sampling capacitors.

4. CDS1 must not go high before the first falling edge of ADCK after CDS2 goes low.

5. It is required that the falling edge of CDS2 should occur before the rising edge of ADCK.

6. In 1-channel CDS mode it is not possible to have a equally spaced Video and Reference sample points with a 45MHz ADCK.

7. Non-CDS operation is also possible; CDS1 is not required in this mode.

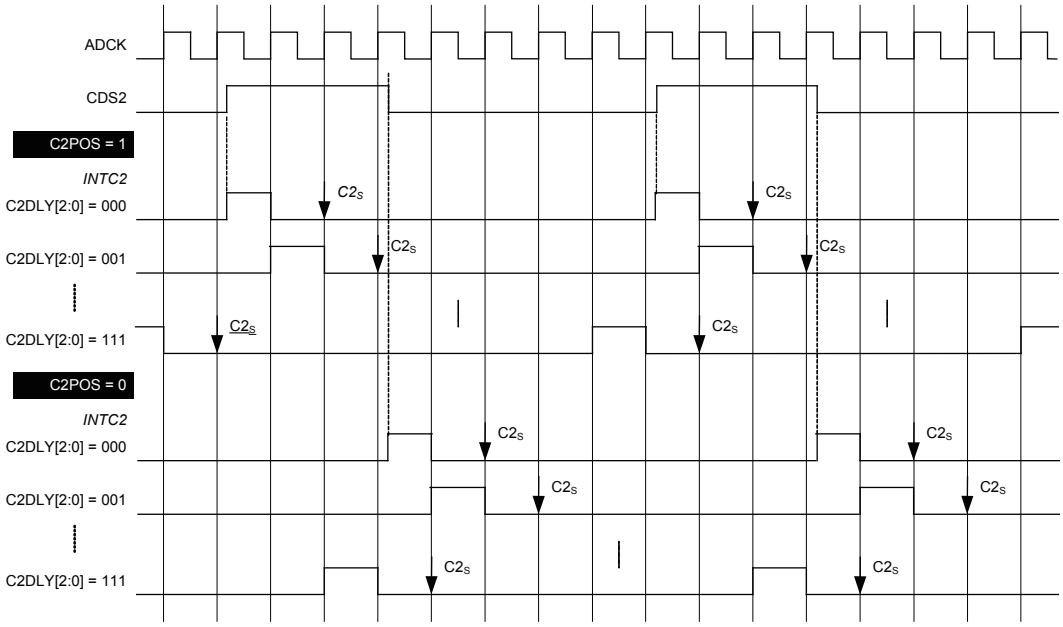


Figure 5 Internal CDS2 Pulses Generated by Programmable CDS2 Detect Circuit

ADCK : 45MHz

Mode	Timing REQ. ADCK:CDS2	Sample Rate (MSPS)	Register Bit						
			CDSREF[1:0]	WS	MODE4	2CH	1CH	CDS	EN
MODE1: 3-CH Pixel-by-Pixel	2n:1, n ≥ 3	7.5	—	1	0	0	0	1	1
								0	
MODE2: 1-CH Line-by-Line	2n:1, n ≥ 3	7.5	—		0		1	1	
								0	
MODE3: 1-CH Line-by-Line	3:1	22.5	00		0		0	1	
								0	
MODE4: 1-CH Line-by-Line	2:1	22.5	—		1		0	0	
								0	

Table 2 "WS" Operating Modes

Note: 1. In 1-channel mode, Setup Register 3 bits 7:6 CH[1:0] determine which input is to be sampled.

2. For Colour Line-by-Line, set Register Bit LNBYLN. For input selection, refer to Table 1, Colour Selection Description in Line-by-Line mode.

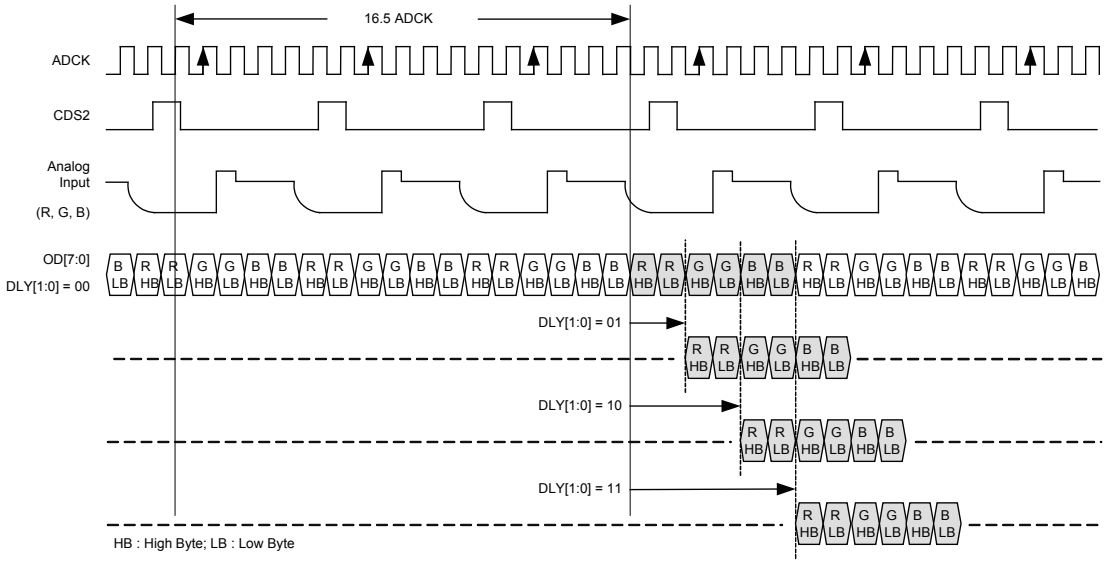


Figure 6 MODE1 : 3-channel Pixel-by-Pixel

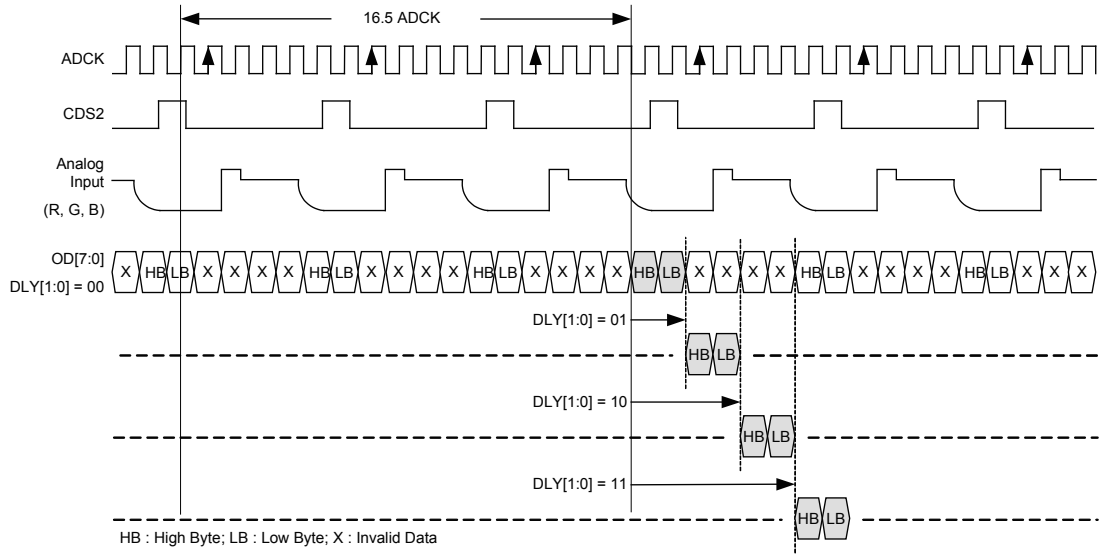


Figure 7 MODE2 : 1-channel Line-by-Line

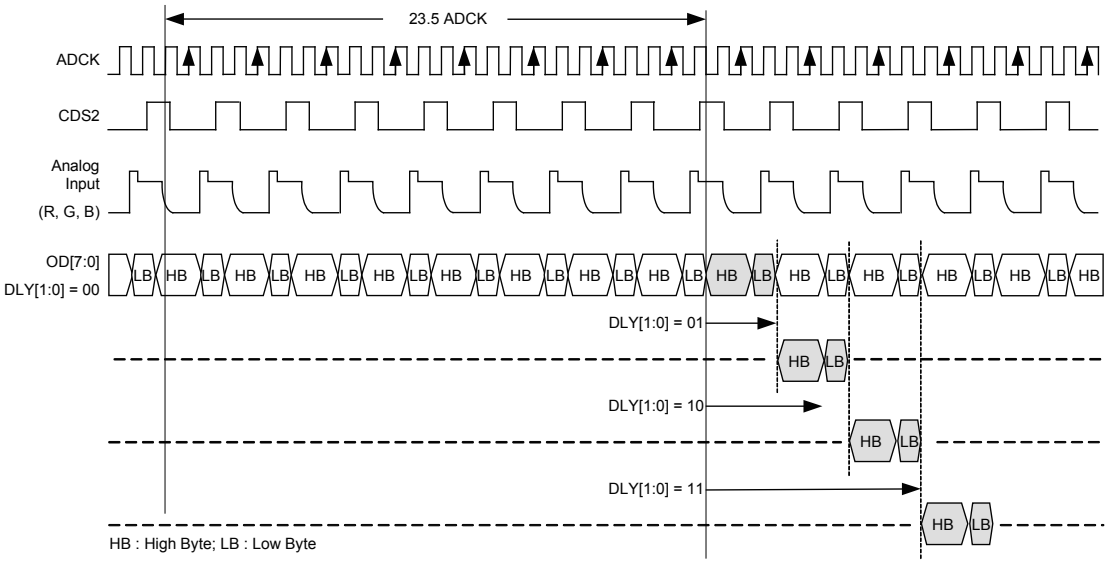


Figure 8 MODE3 : 1-channel Line-by-Line

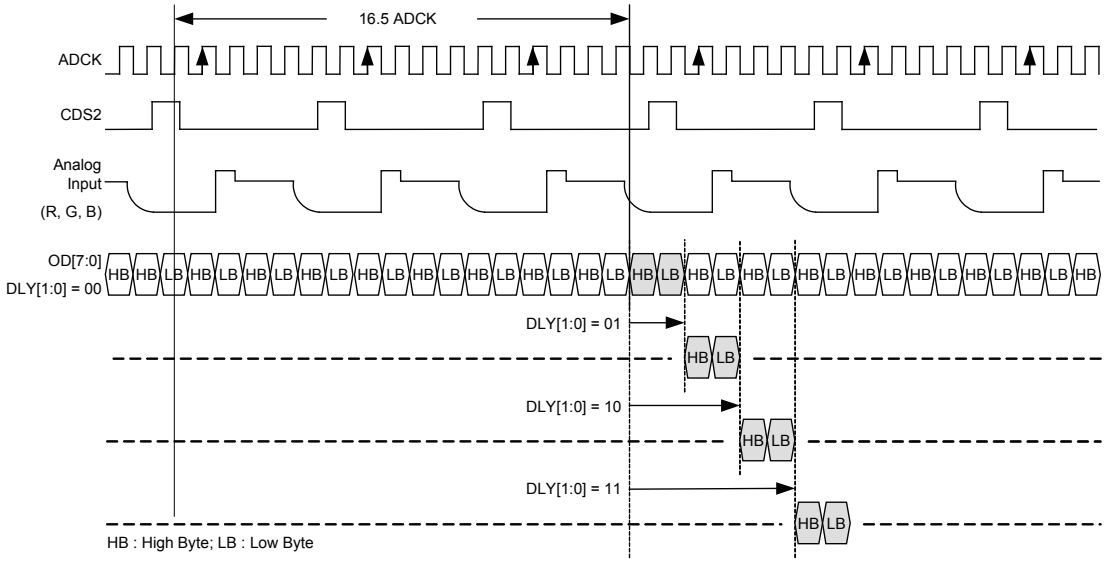


Figure 9 MODE4 : 1-channel Line-by-Line

Reset Level Clamping (RLC)

There are Pixel-Clamping and Line-Clamping two operating modes of HT82V46. It can be selected by register bit CLPCTL. The clamp switch controlled by an internal *CLP* signal, and must set the RLCEN (default=1) register bit to 1 to enable clamping.

Pixel-clamping (CLPCTL=0)

- When WS=0 (Normal Mode) and CDS=X (both for CDS mode and non-CDS mode).

  The RLC switch is closed whenever the CDS1 input pin is high, as shown in Figure 10.

- When WS=1 and CDS=1 (CDS mode only)
  Reset Level Clamping in "WS" mode is only possible in CDS mode and the time at which the clamp switch is closed is concurrent with the reference sample period, $C1_S$, as shown in Figure 11. RLC can be enabled on a pixel by pixel basis under control of the CDS1 input pin. If CDS1 is high when CDS2 is high and is sampled by ADCK then clamping will be enabled for that input sample at the time determined by CDSREF[1:0]. If CDS1 is low at this point then the RLC switch will not be closed for that input sample. If RLC is required on every pixel then the CDS1 pin can be constantly held high in "WS" mode.

Line-clamping (CLPCTL=1)

- WS=0 (Normal Mode) and CDS=0 (Non-CDS mode) only.

  In situations where the input video signal does not have a stable reference level it may be necessary to clamp only during those pixels which have a known state (e.g. the Dummy, or Black pixels at the start or end of a line of most image sensors). This is known as line-clamping and relies on the input capacitor to hold the DC level between clamp intervals. In non-CDS mode (CDS=0) this can be done directly by controlling the CDS1 input pin to go high during the black pixels only. Alternatively it is possible to use CDS1 to identify the black pixels and enable the clamp at the same time as the input is being sampled (i.e. when CDS2 is high and CDS1 is high). This mode is enabled by setting CLPCTL=1 and the operation is shown in Figure 12.

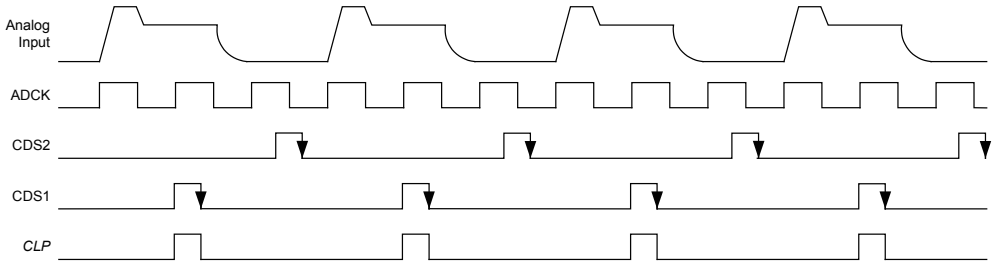


Figure 10 Pixel-Clamping RLC Operation, with CDS (Non-CDS also Possible)

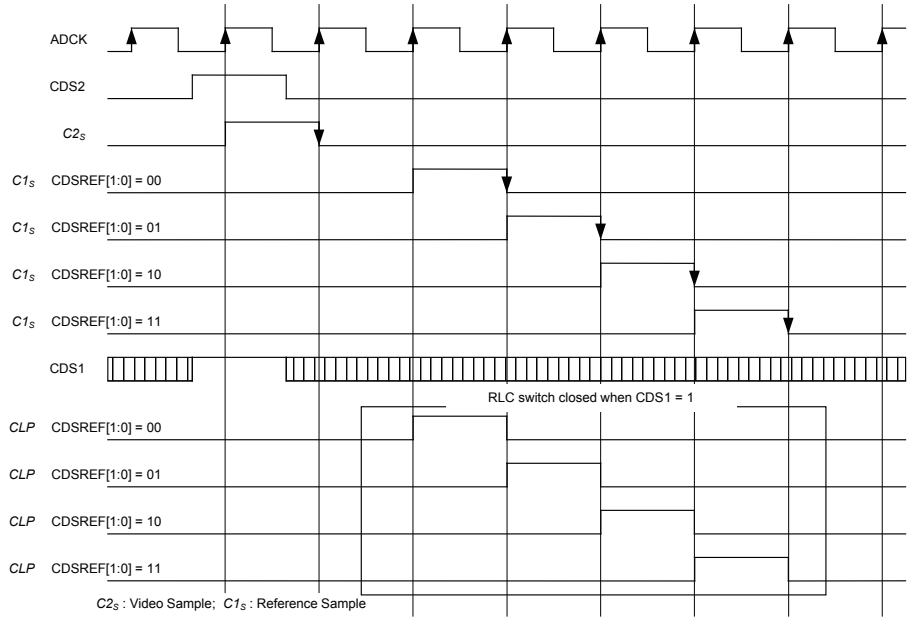


Figure 11 "WS" Mode (WS=1) RLC and Sampling

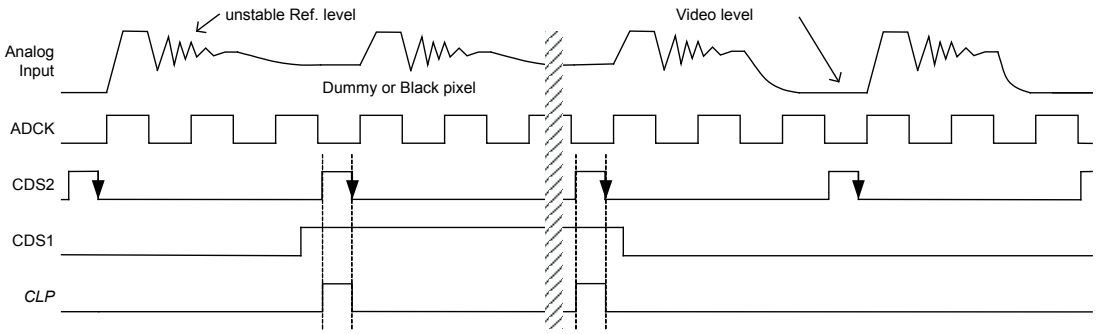


Figure 12 Line-Clamping RLC Operation (Non-CDS Only)

Summaries of the RLC Switch Control

Option	RLC control	Register Bit				
		WS	CLPCTL	RLCEN	ACYC	LNBYLN
Input is DC coupled and within supply range	RLC is not enabled. RLC switch is always open.	X	X	0	X	X
Input video signal has a suitable reference level	RLC switch is controlled by CDS1 pin. CDS1=0/1 : switch is open/closed	0	0	1	X	X
Pixel reference level not stable or need to clamp the black pixels of video period	CDS2 is normal, and CDS1 is used to indicate black pixels location. RLC switch is controlled by CDS1 and CDS2 logical combination. CDS1 & CDS2=0/1: switch is open/closed	0	1	1	X	X
Using “WS” mode	CDS1 pin as RLC/ACYC pin, and the reference sample clock is gated by the “WS” internal timing generator, see Figure 11. CLP is an internal clamp switch control signal. CLP=0/1 : clamp switch open/closed	1	X	1	X	X
Using auto-cycling in “WS” mode	CDS1 pin as auto-cycling control and can’t be clamp control signal. CLPCTL controls whether RLC is enabled or not. CLPCTL=0/1 : RLC is disabled/ enabled; see Figure 11.	1	0 1	X	1	1

Table 3 The Options for the Control of RLC Switch

Offset Adjust and Programmable Gain

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by a 8-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DAC[7:0] and PGA[7:0]. In colour line-by-line mode the gain and offset coefficients for each colour can be multiplexed in order (Red → Green → Blue → Red…) by pulsing the CDS1 pin, or controlled via the ACYC and INTM[1:0] bits. Refer to the Line-by-Line Operation section for more details.

ADC Input Black Level Adjust

The output from the PGA can be offset to match the full-scale range of the differential ADC (2 * (V_{RT} - V_{RB})).

Negative-going Input Cideo Signals

The black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. This will give an output code of FFFF (hex) from the HT82V46 for zero input. If code zero is required for zero differential input then the INVOD bit should be set.

Positive-going Input Video Signals

The black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. This will give an output code of 0000 (hex) from the HT82V46 for zero input.

Bipolar Input Video Signals

It's accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01. Zero differential input voltage gives mid-range ADC output, 7FFF (hex).

Signal Flow Summary

See Figure13 for overall signal flow diagram.

Input Sampling Block

- When CDS=1

  The previously sampled reference level V_{RL} is subtracted from the input video V_{IN}.

  $$V_1 = V_{IN} - V_{RL}$$

- When CDS=0

  The simultaneously sampled voltage on pin VRLC/VBIAS is subtracted instead.

  $$V_1 = V_{IN} - V_{RLC}$$

- If CDACPD=1

  V_{RLC} is an externally applied voltage on pin VRLC/VBIAS.

- If CDACPD=0

  V_{RLC} is the output from the internal RLC DAC.

  $$V_{RLC} = (V_{CSTEP} \times CDAC[3:0]) + V_{CBOT}$$

Where V_{CSTEP}: the step size of the RLC DAC;
V_{CBOT}: the minimum output of the RLC DAC

Offset DAC Block

The resultant signal V_1 is added to the Offset DAC output.

$$V_2 = V_1 + (260mV \times (DAC[7:0] - 127.5)) / 127.5$$

PGA Block

The signal is then multiplied by the PGA gain.

$$V_3 = V_2 + (0.66 + PGA[8:0] \times 7.34 / 511)$$

ADC Block

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

- PGAFS[1:0]=0X

  D_1 [15:0]=INT ((V_3 / V_{FS}) x 65535) + 32767

- PGAFS[1:0]=10

  D_1 [15:0]=INT ((V_3 / V_{FS}) x 65535) + 65535

- PGAFS[1:0]=11

  D_1 [15:0]=INT ((V_3 / V_{FS}) x 65535) + 0

  Where V_{FS}: the ADC full-scale range
  (LOWREF=0 / 1 then V_{FS}= 2V / 1.2V)

Output Invert Block

The polarity of the digital output may be inverted by control bit INVOD.

- INVOD=0

  D_2 [15:0]= D_1 [15:0]

- INVOD=1

  D_2 [15:0]= 65535 − D_1 [15:0]

Output Formats

The output from the HT82V46 can be presented in several different formats under control of the ODFM[1:0] register bits as shown in Figure 14.

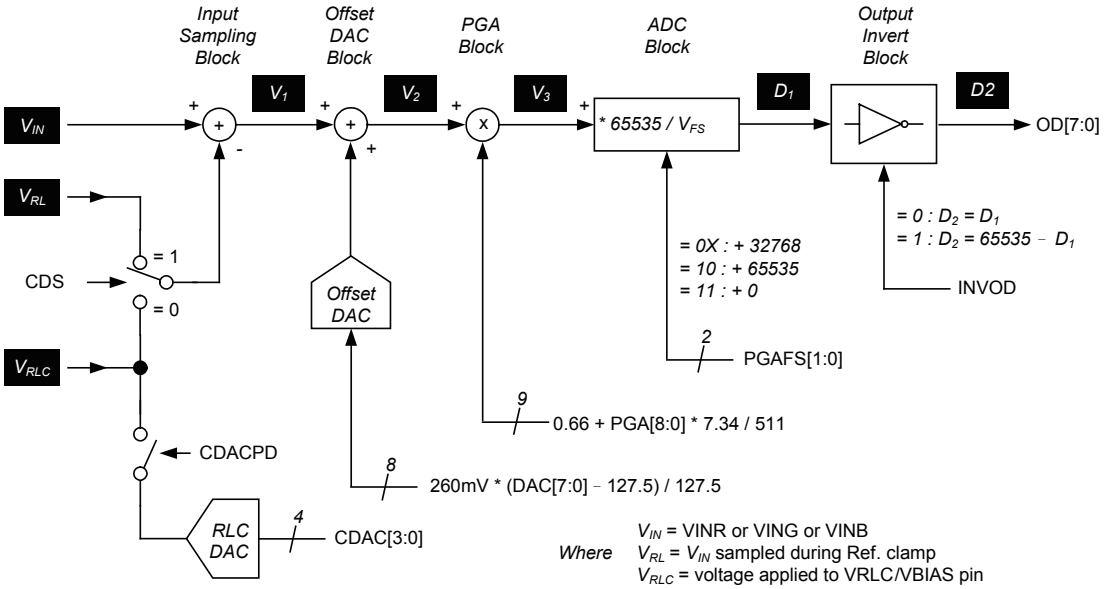


Figure 13 Overall Signal Flow

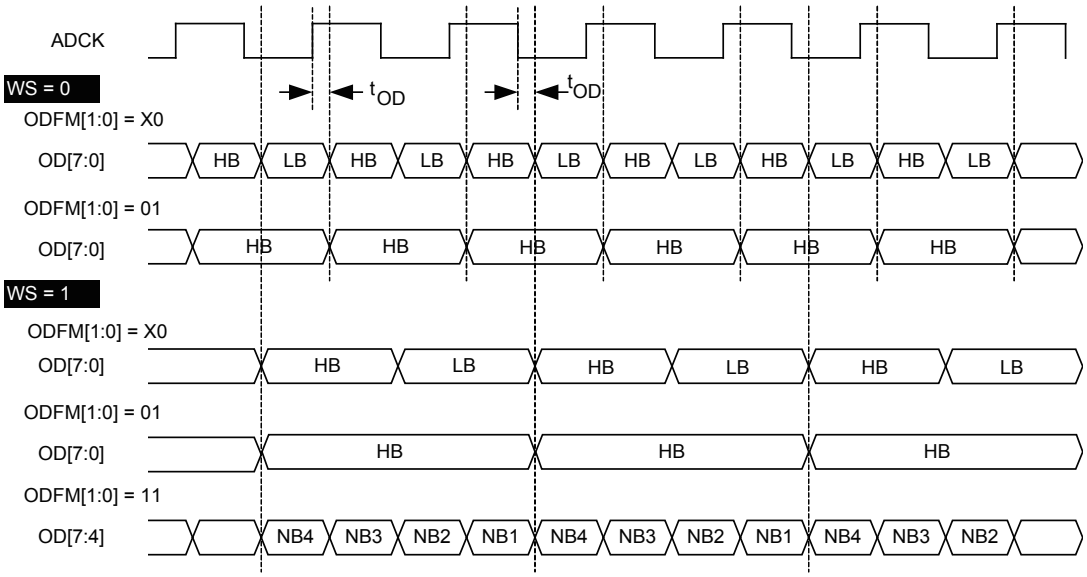


Figure 14 Output Data Format

Serial Control Interface

The internal control registers are programmable and can be read-back via the serial control interface and pin OD[7]/SDO.

Register Write (A4=0)

SCK, SDI and SEN are used for register writing. A address A[5:0] is clocked in through SDI, followed by a data word D[7:0]. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register.

Register Read-back (A4=1 and D[7:0] is don't Cared at Register Write Cycle)

Read-back is initiated by Register Write as described above but with A4 set to 1, followed by an 8-bit dummy data word. Writing address (A5, 1, A3, A2, A1, A0) will cause the contents D[7:0] of corresponding register(A5, 1, A3, A2, A1, A0) to be output D[7:0] on pin SDO/OD[7] at the falling edge of SCK. SDO/OD[7] is shared pin, therefore OEB pin should always be held low and the OPD register bit should be set low when register read-back data is expected on this pin. The next word may be read in to SDI while the previous word is still being output on SDO/OD[7] pin.

Note: To ensure all registers are set to their default values it is recommended that a software-reset is carried out after the power-up sequence, before writing to any other register.

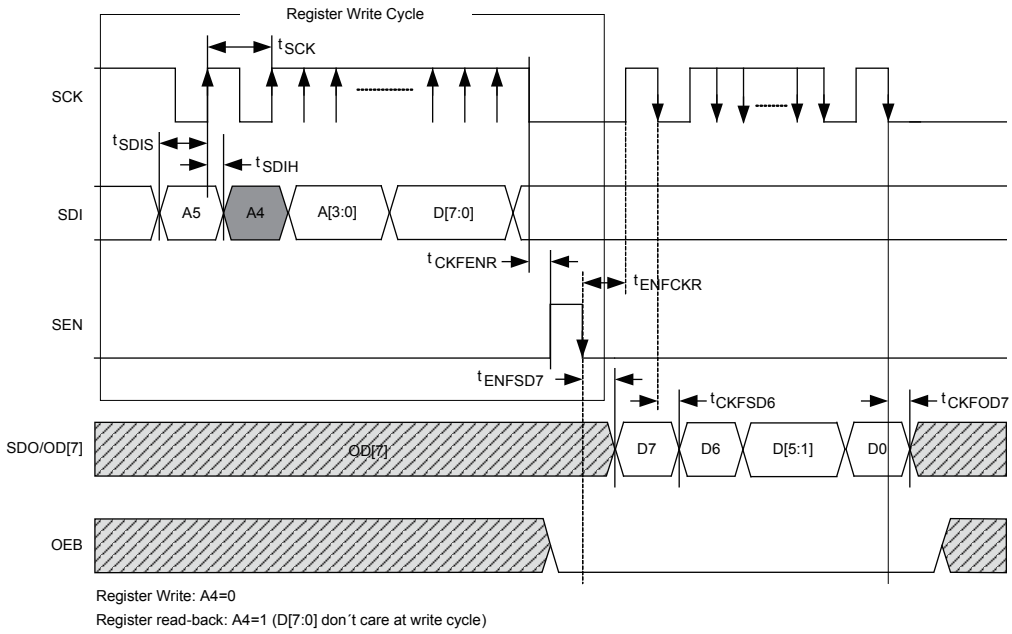


Figure 15 Serial Control Interface Timing

Control Registers

Register Mapping

A[5:0]	Description	POR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
01h	Setup Register 1	03h	RW	WS	MODE4	PGAFS[1:0]		2CH	1CH	CDS	EN
02h	Setup Register 2	20h	RW	DLY[1:0]		CDACRNG	LOWREF	OPD	INVOD	ODFM[1:0]	
03h	Setup Register 3	1Fh	RW	CH[1:0]		CDSREF [1:0]		CDAC[3:0]			
04h	Software Reset	00h	W	—							
05h	Auto-cycle Reset	00h	W	—							
06h	Setup Register 4	00h	RW	0	0	0	0	INTM[1:0]		ACYC	LNBYLN
07h	Setup Register 5	00h	RW	0	CMLPD	REFPD	CDACPD	ADCPD	BPD	GPD	RPD
08h	Setup Register 6	20h	RW	0	CLPCTL	RLCEN	C2POS	C2DLY[2:0]			C2DET
09h	Reserved	00h	RW	0							
0Ah	Reserved	00h	RW	0							
0Bh	Reserved	00h	RW	0							
0Ch	ID	00h	RW	0				ID[3:0]			
0Dh	Reserved	00h	RW	0							
20h	DAC value (Red)	80h	RW	DACR[7:0]							
21h	DAC value (Green)	80h	RW	DACG[7:0]							
22h	DAC value (Blue)	80h	RW	DACB[7:0]							
23h	DAC value (RGB)	80h	W	DAC[7:0]							
24h	PGA gain (Red)	00h	RW	0							PGAR[0]
25h	PGA gain (Green)	00h	RW	0							PGAG[0]
26h	PGA gain (Blue)	00h	RW	0							PGAB[0]
27h	PGA gain (RGB)	00h	W	0							PGA[0]
28h	PGA gain (Red)	0Dh	RW	PGAR[8:1]							
29h	PGA gain (Green)	0Dh	RW	PGAG[8:1]							
2Ah	PGA gain (Blue)	0Dh	RW	PGAB[8:1]							
2Bh	PGA gain (RGB)	00h	W	PGA[8:1]							

Register Description

Register	Bit No.	Name	POR.	Description
Setup Register 1	0	EN	1	Global Enable 0= complete power down 1= fully active
	1	CDS	1	Sampling mode select 0= 2 or 3 channel 1= 1 channel. Input channel selected by CH[1:0] bits and unused channels are powered down.
	2	1CH	0	Sampling mode select 0= 1 or 3 channel 1= 2 channel mode. Input channels are Red and Green. Blue channel is powered down.
	3	2CH	0	Sampling mode select 0= 1 or 3 channel 1= 2 channel mode. Input channels are Red and Green. Blue channel is powered down.
	5:4	PGAFS[1:0]	00	Offsets PGA output to optimize the ADC range for different polarity sensor output signals. Zero differential PGA input signal gives: 0x= Zero output from the PGA, output=32767 10= Full-scale positive output, output=65535; use for negative going video. Set INVOD=1 if zero differential input should give a zero output code with negative going video. 11= Full-scale negative output, output=0; use for positive going video
	6	MODE4	0	This bit has no effect when WS=0. Set this bit when operating in “WS” MODE 4. 0= Other mode 1= “WS” MODE 4
	7	WS	0	Makes the HT82V46 timing to the other operating mode selection 0= Normal timing 1= Enable “WS” timing. Requires double rate ADCK and pixel rate CDS2 input. CDS1 pin performs same function as RLC/ACYC pin.

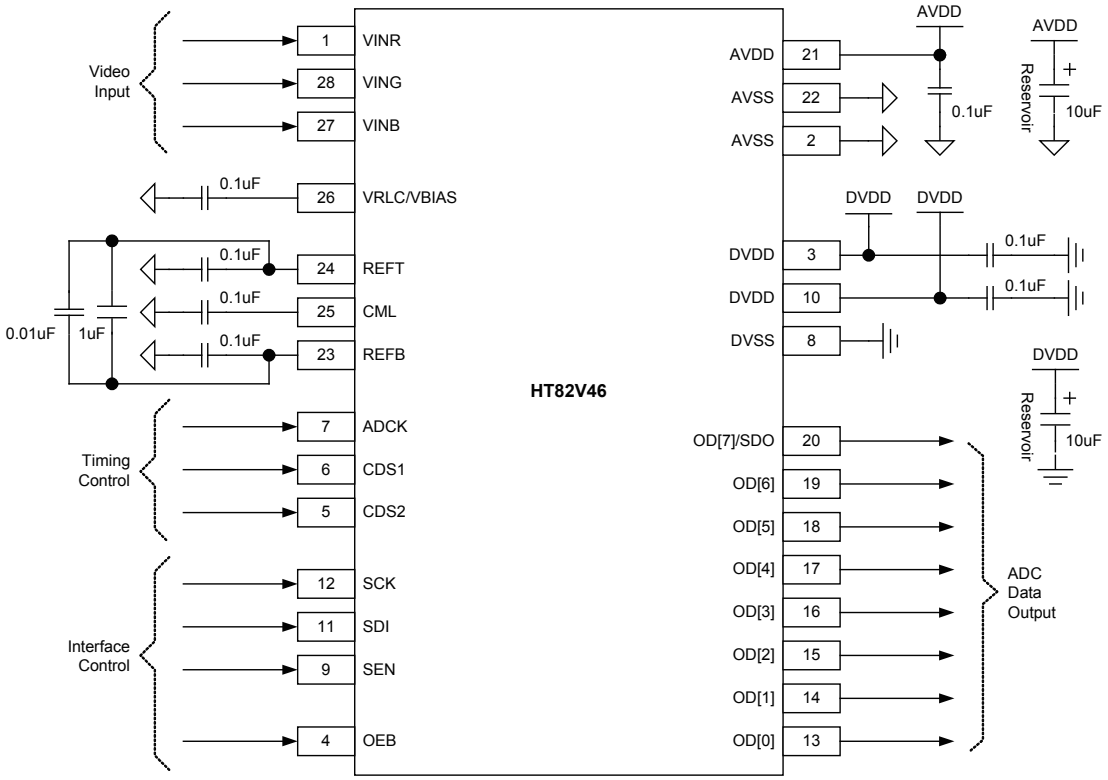
<table>
<tr><th>Register</th><th>Bit No.</th><th>Name</th><th>POR.</th><th>Description</th></tr>
<tr><td rowspan="6">Setup Register 2</td><td>1:0</td><td>ODFM[1:0]</td><td>0</td><td>Determines the output data format
X0= 8 bits multiplexed (8+8 bits)
01= 8 bits parallel (8-MSB only)
11= 4-bit multiplexed mode (4+4+4+4 bits). This mode is only valid when WS=1.</td></tr>
<tr><td>2</td><td>INVOD</td><td>0</td><td>Digitally inverts the polarity of output data</td></tr>
<tr><td>3</td><td>OPD</td><td>0</td><td>Output disable. This works with the OEB pin to control the output pins.
0= Digital outputs enabled
1= Digital outputs high impedence
<table>
<tr><th>OEB</th><th>OPD</th><th>OD</th></tr>
<tr><td>0</td><td>0</td><td>Enabled</td></tr>
<tr><td>0</td><td>1</td><td>Hi-Z</td></tr>
<tr><td>1</td><td>0</td><td>Hi-Z</td></tr>
<tr><td>1</td><td>1</td><td>Hi-Z</td></tr>
</table></td></tr>
<tr><td>4</td><td>LOWREF</td><td>0</td><td>Reduces the ADC reference range 2*(V_{RT} – V_{RB}), thus changing the max/min input voltages.
0= ADC reference range=2V
1= ADC reference range=1.2V</td></tr>
<tr><td>5</td><td>CDACRNG</td><td>1</td><td>Sets the output range of the RLCDAC
0= RLCDAC ranges from 0 to AVDD
1= RLCDAC ranges from 0 to V_{RT}</td></tr>
<tr><td>7:6</td><td>DLY[1:0]</td><td>00</td><td>Controls the latency from sample to data appearing on output pins
<table>
<tr><th>WS</th><th>= 0</th><th>= 1</th><th>= 1</th></tr>
<tr><td>Timing modes</td><td>All</td><td>1-2, 4-6</td><td>3</td></tr>
<tr><td>DLY=00</td><td>7T</td><td>16.5T</td><td>23.5T</td></tr>
<tr><td>DLY=01</td><td>8T</td><td>18.5T</td><td>26.5T</td></tr>
<tr><td>DLY=10</td><td>9T</td><td>20.5T</td><td>29.5T</td></tr>
<tr><td>DLY=11</td><td>10T</td><td>22.5T</td><td>31.5T</td></tr>
<tr><td colspan="4">Where T=ADCK periods</td></tr>
</table></td></tr>
<tr><td>Setup register 3</td><td>3:0</td><td>CDAC[3:0]</td><td>1111</td><td>Controls RLCDAC driving VRLC/VBIAS pin to define ended signal reference voltage or reset level clamp voltage.</td></tr>
<tr><td>—</td><td>5:4</td><td>CDSREF[1:0]</td><td>01</td><td>When WS=0 these register bit have no effect.
CDS mode timing adjust.
00= Advance reference sample by 1 ADCK period
01= Default reference sample position
10= Delay reference sample by 1 ADCK period
11= Delay reference sample by 2 ADCK period</td></tr>
<tr><td>—</td><td>7:6</td><td>CH[1:0]</td><td>00</td><td>When 1CH=0 these register bits have no effect.
Monochrome mode channel select.
00= Select red channel
01= Select green channel
10= Select blue channel
11= Reserved</td></tr>
<tr><td>Software</td><td>—</td><td>—</td><td>—</td><td>Write this register will causes all function to be reset.
It is recommended that a software reset be performed after a power on before any other register writes.</td></tr>
<tr><td>Auto-cycle reset</td><td>—</td><td>—</td><td>—</td><td>Write this register will causes the auto-cycle counter to reset to VINR.
This function is only required when LNBYLN=1.</td></tr>
</table>

Register	Bit No.	Name	POR.	Description
Setup register 4	0	LNBYLN	0	Selects line by line operation. Line by line operation is intended for use with systems which operate one line at a time but with up to three color shared on the one output.
	1	ACYC	0	If LNBYLN=0 then ACYC bit no effect. ACYC bit determines CDS1 pin and offset/gain register controls 0= CDS1 pin is for Reference Sampling or Reset Level Clamp control. And INTM[1:0] bits are for gain/offset multiplexers control. 1= Auto-cycling enabled by pulsing CDS1 pin and input signal switched to next gain/offset register sequentially. And sequence is Red -> Green -> Blue -> Red etc. At this mode, it must set CDS=0 and use CLPCTL bit instead CDS1 pin to control RLC.
	3:2	INTM[1:0	00	When LNBYLN=0 or ACYC=1 this bit has no effect. When LNBYLN=1 and ACYC=0. Controls the offset/gain mux selector. 00= Red offset/gain registers applied to input channel. 01= Green offset/gain registers applied to input channel. 10= Blue offset/gain registers applied to input channel. 11= Reserved.
	7:4	Reserved	0000	
Setup register 5	0	REDPD	0	When set powers down red S/H, PGA
	1	GRNPD	0	When set powers down green S/H, PGA
	2	BLUPD	0	When set powers down blue S/H, PGA
	3	ADCPD	0	When set powers down ADC, allows reduced power consumption without powering down the references which have a long time constant when switching on/off due to the external decoupling capacitors.
	4	CDACPD	0	When set powers down 4-bit RLCDAC, setting the output to a high impedance state and allowing an external reference to be driven in on the VRLC/VBIAS pin.
	5	REFPD	0	When set disables REFT, REFB buffers to allow external references to be used.
	6	CMLPD	0	When set disable CML buffer to allow an externa reference to be used.
	7	Reserved	0	Must be set to 0

Register	Bit No.	Name	POR.	Description
Setup register 6	0	C2DET	0	When WS=0 this register bit has no effect. When WS=1. 0= Normal operation, signal on CDS2 input pin is applied directly to timing control block. 1= Programmable CDS2 detect circuit is enabled. An internal synchronization pulse is generated from signal applied to CDS2 input pin and is applied to timing control block on place of CDS2.
	3:1	C2DLY[2:0]	000	When WS=0 or C2DET=0 these bits have no effect. The C2DLY bits set a programmable delay from the detected edge of the signal applied to the CDS2 pin. The internally generated pulse is delayed by C2DLY ADCK periods from the detected edge.
	4	C2POS	0	When WS=0 or C2DET=0 this bit has no effect When WS=1 and C2DET=1 this bit controls whether positive or negative edges on the CDS2 input pin are detected. 0= Negative edge on CDS2 pin is detected and used to generate internal timing pulse. 1= Positive edge on CDS2 pin is detected and used to generate internal timing pulse.
	5	RLCEN	1	Reset level clamping enable. When set RLCEN is enabled. The method of clamping is determined by CLPCTL and WS. In “WS” mode clamping will still occur on every pixel at a time defined by the CDSREF[1:0] bits.
	6	CLPCTL	0	This bit has no effect if WS=1. See Table 3 for more information. 0= RLC switch is controlled directly from CDS1 input pin. CDS1= 0: switch is open CDS1= 1: switch is close 1= RLC switch is controlled by logical combination of CDS1 and CDS2. CDS1 & CDS2=0 : switch is open. CDS1 & CDS2=1 : switch is close.
	7	Reserved	0	Must be set to 0.
ID	7:4	Reserved	0	Must be set to 0.
	3:0	ID[3:0]	0000	ID[3:0] these bits are storable and can be written from 0000 to 1111 values. But note that ID[3:0] will be cleared to 0000 after Power-On-Reset.
DAC value (Red)	7:0	DACR[7:0]	0	Red channel 8-bit offset DAC MSB value.
DAC value (Green)	7:0	DACG[7:0]	0	Green channel 8-bit offset DAC MSB value.
DAC value (Blue)	7:0	DACB[7:0]	0	Blue channel 8-bit offset DAC MSB value.
DAC value (RGB)	7:0	DAC[7:0]	0	Write to this register will cause the R, G and B offset DAC MSB registers to be overwritten by the new value.
PGA gain (Red)	0	PGAR[0]	0	This register bit forms the LSB of the red channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 28 hex.
PGA gain (Green)	0	PGAG[0]	0	This register bit forms the LSB of the green channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 29 hex.
PGA gain (Blue)	0	PGAB[0]	0	This register bit forms the LSB of the blue channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 2A hex.
PGA gain (RGB)	0	PGA[0]	0	Writing a value to this location causes red, green and blue PGA LSB gain values to be overwritten by the new value.
PGA gain (Red)	7:0	PGAR[8:1]	0D	Red PGA gain setting register. 0.66+PGAR[8:0]*7.34/511
PGA gain (Green)	7:0	PGAG[8:1]	0D	Green PGA gain setting register. 0.66+PGAG[8:0]*7.34/511

Register	Bit No.	Name	POR.	Description
PGA gain (Blue)	7:0	PGAB[8:1]	0D	Blue PGA gain setting register. 0.66+PGAB[8:0]*7.34/511
PGA gain (RGB)	7:0	PGA[8:1]	0	A write to this register will cause R, G and B PGA gain registers to be overwritten by the new value.

Application Circuits



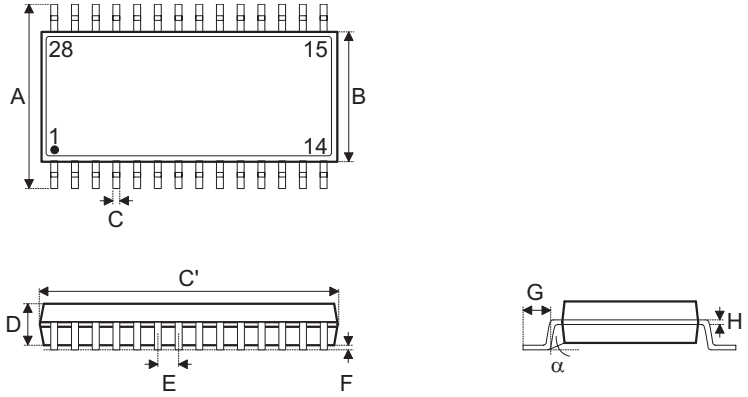
Note: 1. All de-coupling capacitors should be fitted as close to HT82V46 as possible.

2. AVSS and DVSS should be connected as close to HT82V46 as possible.

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (http://www.holtek.com.tw/english/literature/package.pdf) for the latest version of the package information.

28-pin SSOP (209mil) Outline Dimensions

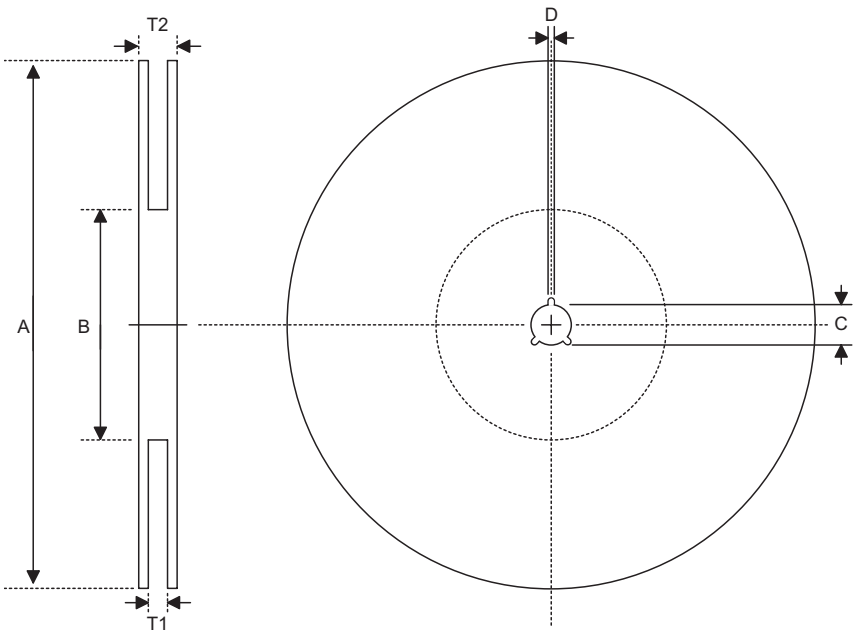


MS-150

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.291	—	0.323
B	0.197	—	0.220
C	0.009	—	0.013
C'	0.390	—	0.413
D	—	—	0.079
E	—	0.026	—
F	0.002	—	—
G	0.022	—	0.037
H	0.004	—	0.008
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	7.40	—	8.20
B	5.00	—	5.60
C	0.22	—	0.33
C'	9.90	—	10.50
D	—	—	2.00
E	—	0.65	—
F	0.05	—	—
G	0.55	—	0.95
H	0.09	—	0.21
α	0°	—	8°

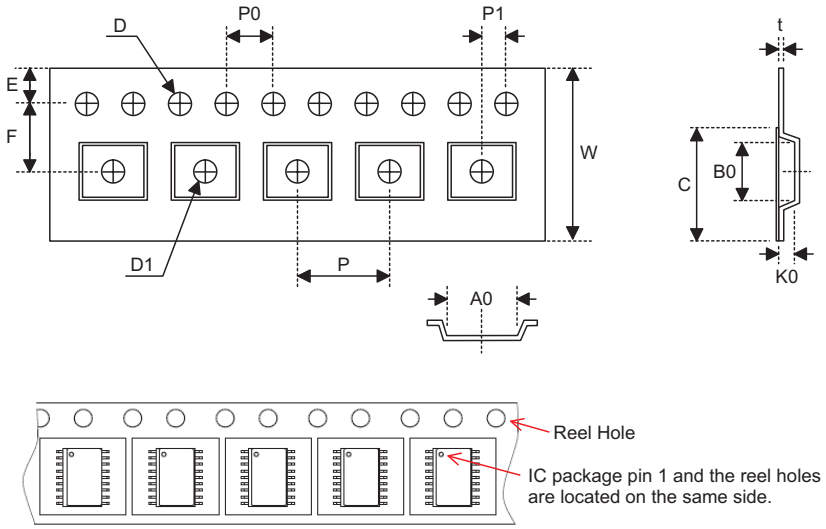
Reel Dimensions



SSOP 28S (209mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	28.4 $^{+0.3/-0.2}$
T2	Reel Thickness	31.1 (max.)

Carrier Tape Dimensions



SSOP 28S (209mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	$1.5^{+0.1/-0.00}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.2
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	8.4±0.1
B0	Cavity Width	10.65±0.10
K0	Cavity Depth	2.4±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	21.3±0.1

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