# MC74ACT564

# Octal D-Type Flip-Flop with 3-State Outputs1

The MC74ACT564 is a high–speed, low power octal flip–flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$).

The information presented to the D inputs is stored in the flip–flops on the LOW–to–HIGH Clock (CP) transition.

The MC74ACT564 device is functionally indentical to the MC74ACT574, but with inverted outputs.

- Inputs and Outputs on the Opposite Sides of the Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessor
- Functionally Indentical to the MC74ACT574 but with Inverted Outputs
- 3–State Outputs for Bus–Oriented Applications
- Outputs Source/Sink 24 mA
- TTL Compatible Inputs

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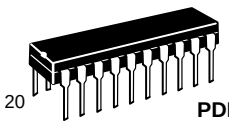
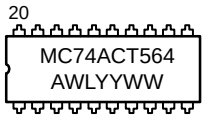
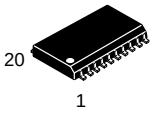
**MARKING DIAGRAMS**

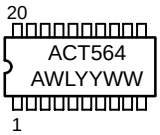


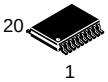

**PDIP–20**
**N SUFFIX**
**CASE 738**



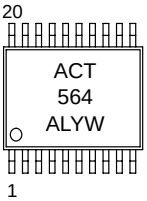




**SO–20**
**DW SUFFIX**
**CASE 751D**




**TSSOP–20**
**DT SUFFIX**
**CASE 948E**




A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MC74ACT564N | PDIP–20 | 18 Units/Rail |
| MC74ACT564DW | SOIC–20 | 38 Units/Rail |
| MC74ACT564DWR2 | SOIC–20 | 1000 Tape & Reel |
| MC74ACT564DT | TSSOP–20 | 75 Units/Rail |
| MC74ACT564DTR2 | TSSOP–20 | 2500 Tape & Reel |

**PIN ASSIGNMENT**

| PIN | FUNCTION |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| CP | Clock Pulse Input |
| $\overline{OE}$ | 3–State Output Enable Input |
| $\overline{O}_0$–$\overline{O}_7$ | 3–State Outputs |

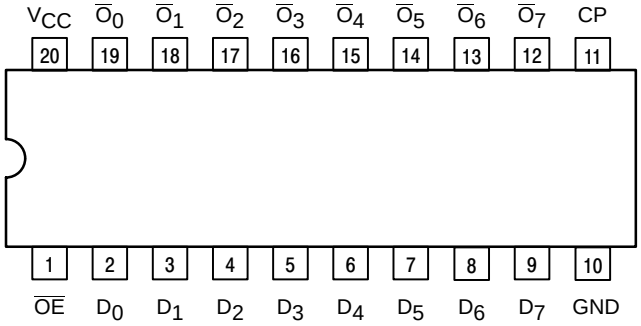



**Figure 1. Pinout: 20–Lead Packages Conductors**
(Top View)

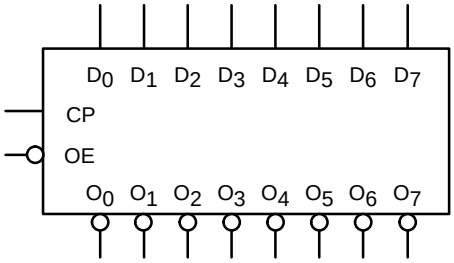
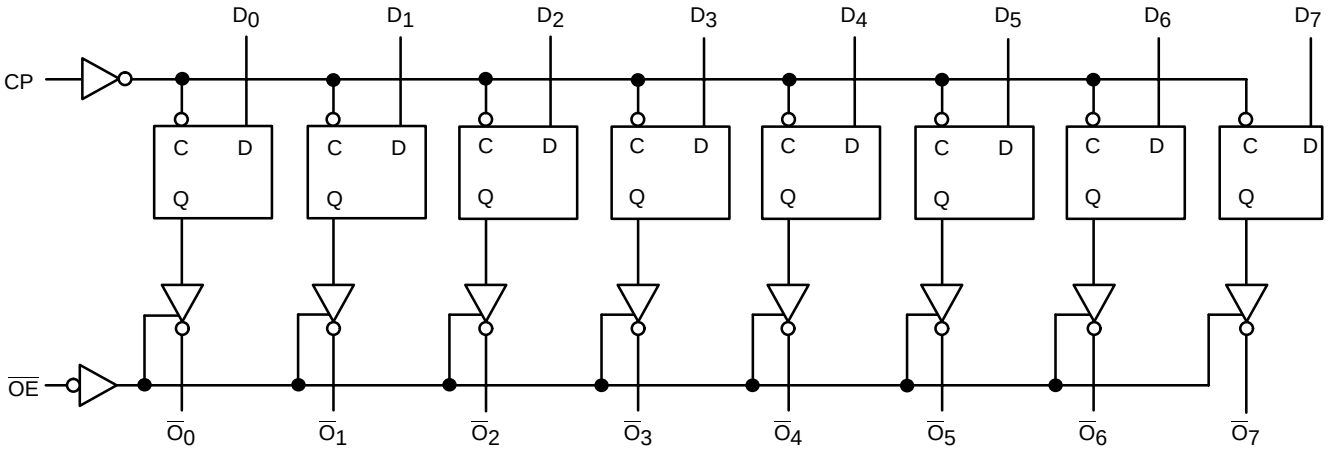



**Figure 2. Logic Symbol**




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 3. Logic Diagram**

**FUNCTION TABLE**

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | Q | O | |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | ⌐ | L | H | Z | Load |
| H | ⌐ | H | L | Z | Load |
| L | ⌐ | L | H | H | Data Available |
| L | ⌐ | H | L | L | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW–to–HIGH Transition
NC = No Change

## FUNCTIONAL DESCRIPTION

The MC74ACT564 consists of eight edge–triggered flip–flops with individual D–type inputs and 3–state complementary outputs. The buffered clock and buffered Output Enable are common to all flip–flops. The eight flip–flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW–to–HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip–flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip–flops.

**MAXIMUM RATINGS** (Note 1)

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | | $-0.5 \le V_I \le V_{CC} + 0.5$ | V |
| $V_O$ | DC Output Voltage | (Note 2) | $-0.5 \le V_O \le V_{CC} + 0.5$ | V |
| $I_{IK}$ | DC Input Diode Current | | ±20 | mA |
| $I_{OK}$ | DC Output Diode Current | | ±50 | mA |
| $I_O$ | DC Output Sink/Source Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current per Output Pin | | ±50 | mA |
| $I_{GND}$ | DC Ground Current per Output Pin | | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction temperature under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal resistance | PDIP<br>SOIC<br>TSSOP | 67<br>96<br>128 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 85°C | PDIP<br>SOIC<br>TSSOP | 750<br>500<br>450 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 30% – 35% | UL–94–VO (0.125 in) | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 3)<br>Machine Model (Note 4)<br>Charged Device Model (Note 5) | > 2000<br>> 200<br>> 1000 | V |
| $I_{Latch–Up}$ | Latch–Up Performance | Above $V_{CC}$ and Below GND at 85°C (Note 6) | ±100 | mA |

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied.
2. $I_O$ absolute maximum rating must be observed.
3. Tested to EIA/JESD22–A114–A.
4. Tested to EIA/JESD22–A115–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | DC Input Voltage (Referenced to GND) | | 4.5 | | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | –40 | 25 | +85 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 8) | $V_{CC}$ = 4.5 V<br>$V_{CC}$ = 5.5 V | 0<br>0 | 10<br>8.0 | 10<br>8.0 | ns/V |
| $T_J$ | Junction Temperature (PDIP) | | | | 140 | °C |
| $I_{OH}$ | Output Current – High | | | | –24 | mA |
| $I_{OL}$ | Output Current – Low | | | | 24 | mA |

7. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. $V_{in}$ from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

**DC CHARACTERISTICS**

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | $T_A$ = –40°C to +85°C | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V<br>V | $V_{OUT}$ = 0.1 V<br>or<br>$V_{CC}$ – 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V<br>V | $V_{OUT}$ = 0.1 V<br>or<br>$V_{CC}$ – 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V<br>V | $I_{OUT}$ = –50 μA |
| | | 4.5<br>5.5 | | 3.86<br>4.86 | 3.76<br>4.76 | V<br>V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ –24 mA<br>$I_{OH}$ –24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V<br>V | $I_{OUT}$ = 50 μA |
| | | 4.5<br>5.5 | | 0.36<br>0.36 | 0.44<br>0.44 | V<br>V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ 24 mA<br>$I_{OL}$ 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $\Delta I_{CCT}$ | Additional Max. $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I$ = $V_{CC}$ – 2.1 V |
| $I_{OZ}$ | Maximum 3–State Current | 5.5 | | ±0.5 | ±5.0 | μA | $V_I$ (OE) = $V_{IL}$, $V_{IH}$<br>$V_I$ = $V_{CC}$, GND<br>$V_O$ = $V_{CC}$, GND |
| $I_{OLD}$<br>$I_{OHD}$ | †Minimum Dynamic Output Current | 5.5<br>5.5 | | | 75<br>–75 | mA<br>mA | $V_{OLD}$ = 1.65 V Max<br>$V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

**AC CHARACTERISTICS** $t_r$ = $t_f$ = 3.0 ns (For Figures and Waveforms, See Figures 4, 5, and 6.)

| Symbol | Parameter | $V_{CC}$* (V) | $T_A$ = +25°C<br>$C_L$ = 50 pF | | | $T_A$ = –40°C to +85°C<br>$C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{max}$ | Maximum Clock Frequency | 5.0 | 85 | | | 75 | | MHz |
| $t_{PLH}$ | Propagation Delay CP to $\overline{Q}_n$ | 5.0 | 2.0 | | 10.5 | 1.5 | 11.5 | ns |
| $t_{PHL}$ | Propagation Delay CP to $\overline{Q}_n$ | 5.0 | 1.5 | | 9.5 | 1.5 | 10.5 | ns |
| $t_{PZH}$ | Output Enable Time | 5.0 | 1.5 | | 9.0 | 1.5 | 9.5 | ns |
| $t_{PZL}$ | Output Enable Time | 5.0 | 1.5 | | 8.5 | 1.0 | 9.5 | ns |
| $t_{PHZ}$ | Output Disable Time | 5.0 | 1.5 | | 10.5 | 1.5 | 11.5 | ns |
| $t_{PLZ}$ | Output Disable Time | 5.0 | 1.5 | | 8.0 | 1.0 | 8.5 | ns |

*Voltage Range 5.0 V is 5.0 V ±0.5 V

### AC OPERATING REQUIREMENTS

| Symbol | Parameter | | $V_{CC}$* (V) | $T_A$ = +25°C $C_L$ = 50 pF | $T_A$ = –40°C to +85°C $C_L$ = 50 pF | Unit |
|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Minimum | |
| $t_s$ | Setup Time, HIGH or LOW | $D_n$ to $C_P$ | 5.0 | | 2.5 | 3.0 | ns |
| $t_h$ | Hold Time, HIGH or LOW | $D_n$ to $C_P$ | 5.0 | | 1.0 | 1.0 | ns |
| $t_w$ | $C_P$ Pulse Width | HIGH or LOW | 5.0 | | 3.0 | 3.5 | ns |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

### CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 50 | pF | $V_{CC}$ = 5.0 V |

## SWITCHING WAVEFORMS

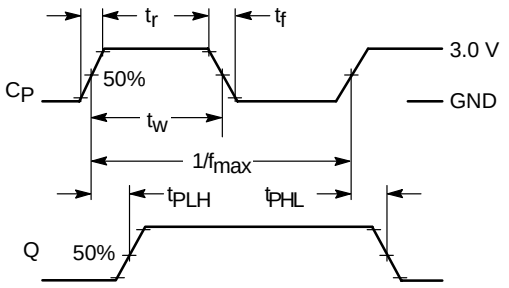



**Figure 4.**

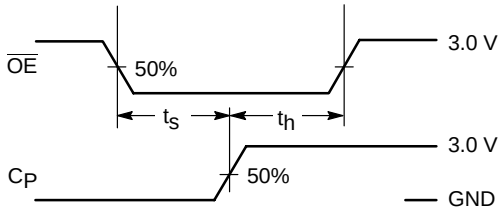



**Figure 5.**

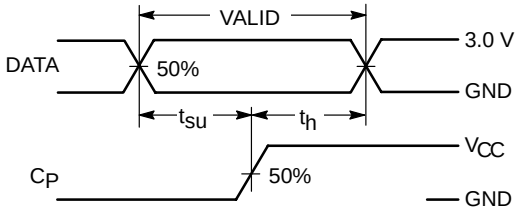
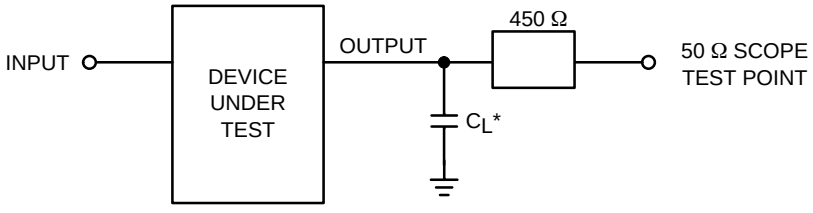



**Figure 6.**

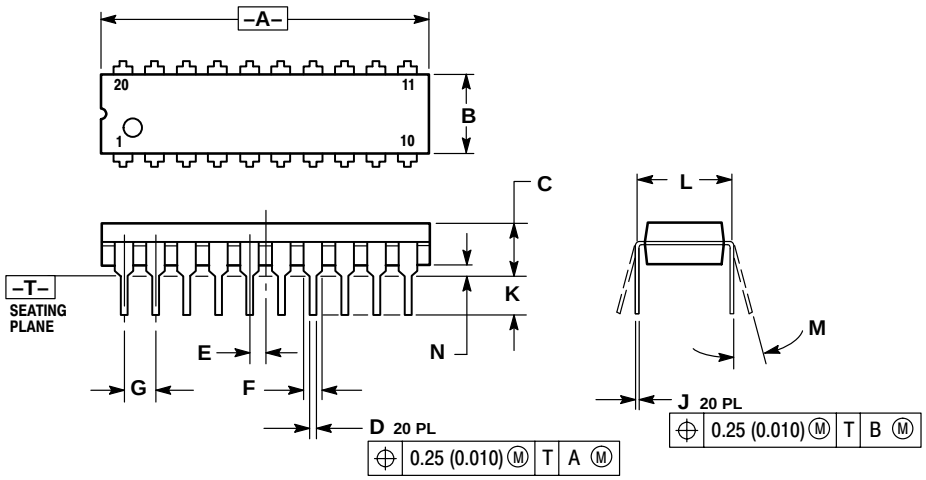



*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

## PACKAGE DIMENSIONS

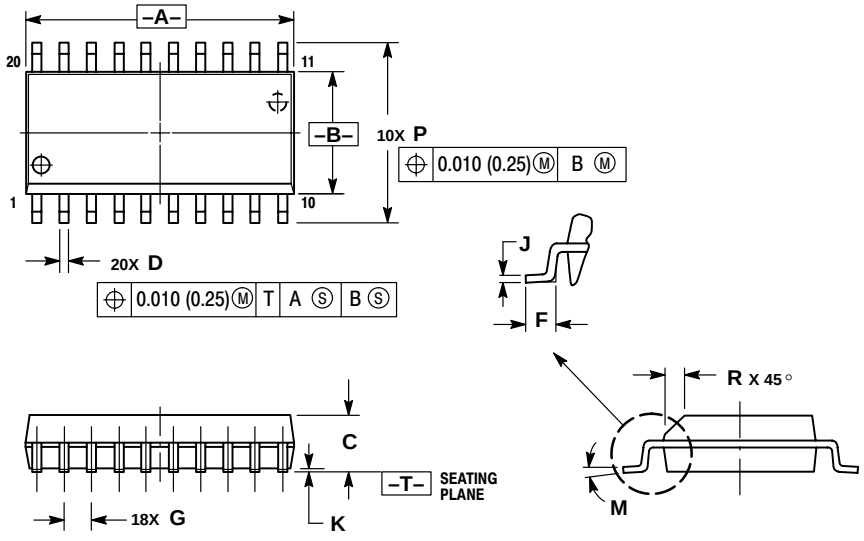
**N SUFFIX**
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**DW SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E

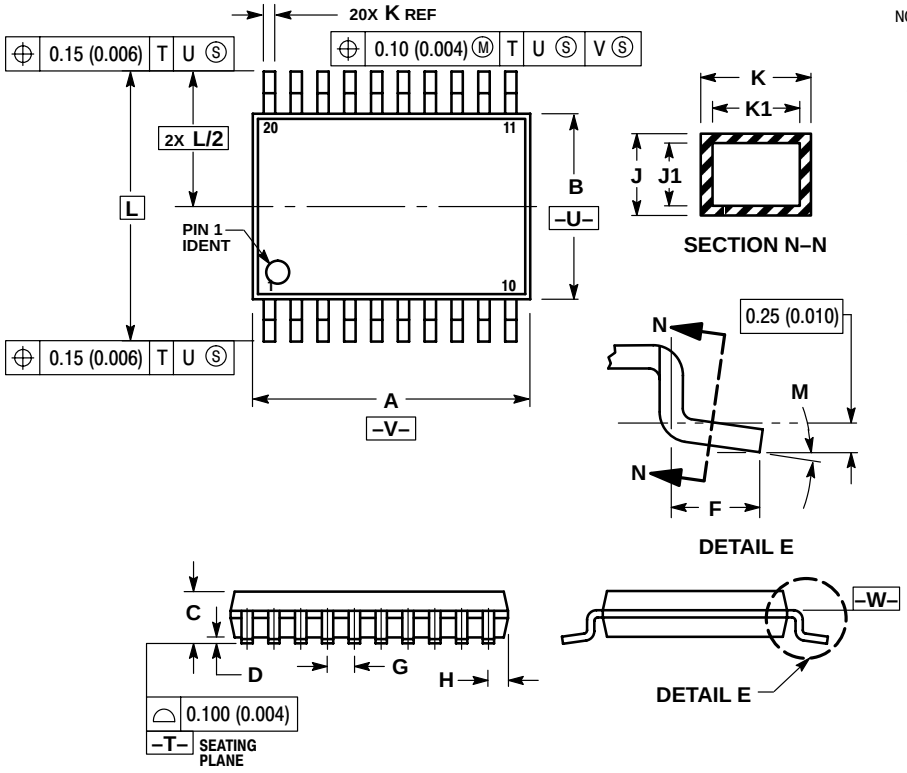



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

## PACKAGE DIMENSIONS

**TSSOP–20**
**DT SUFFIX**
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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