

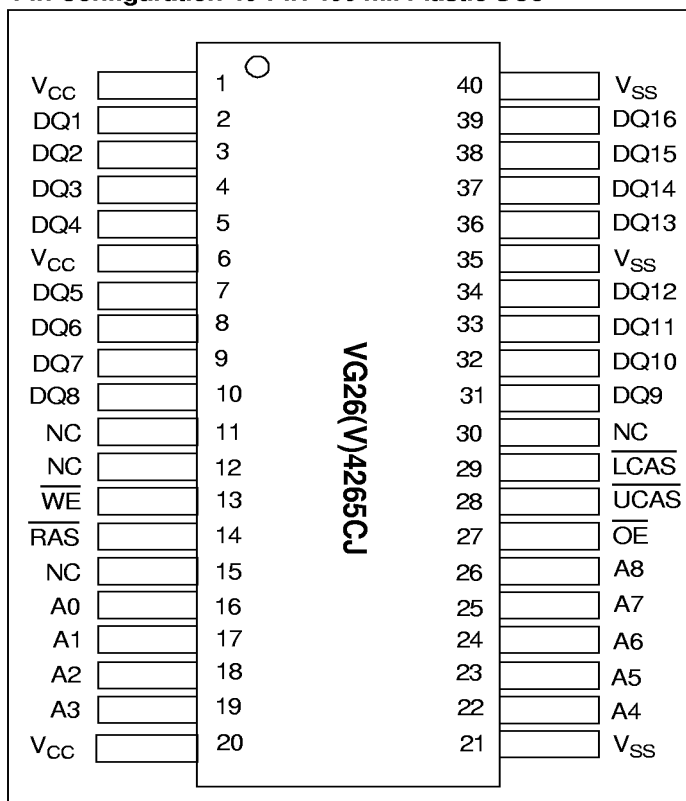
Description

The device is CMOS Dynamic RAM organized as 262,144 words x 16 bits with extended data out access mode. It is fabricated with an advanced submicron CMOS technology and advanced CMOS circuit design technologies. It is packaged in JEDEC standard 40-pin plastic SOJ package.

Features

- Single 5V ($\pm 10\%$) or 3.3V ($\pm 10\%$) power supply
- High speed t_{RAC} access time :
 - 5V: 25/28/30/35/40ns
 - 3.3V: 40/50/60ns
- Low power dissipation
- Extended-data-out (EDO) page mode access
- I/O level: TTL compatible
 - 5V: TTL compatible
 - 3.3V: LVTTL compatible
- 512 refresh cycles in 8 ms
- 2 $\overline{CAS}$ byte control
- 3 refresh modes :
 - $\overline{RAS}$ only refresh
 - $\overline{CAS}$ -before- $\overline{RAS}$ refresh
 - Hidden refresh

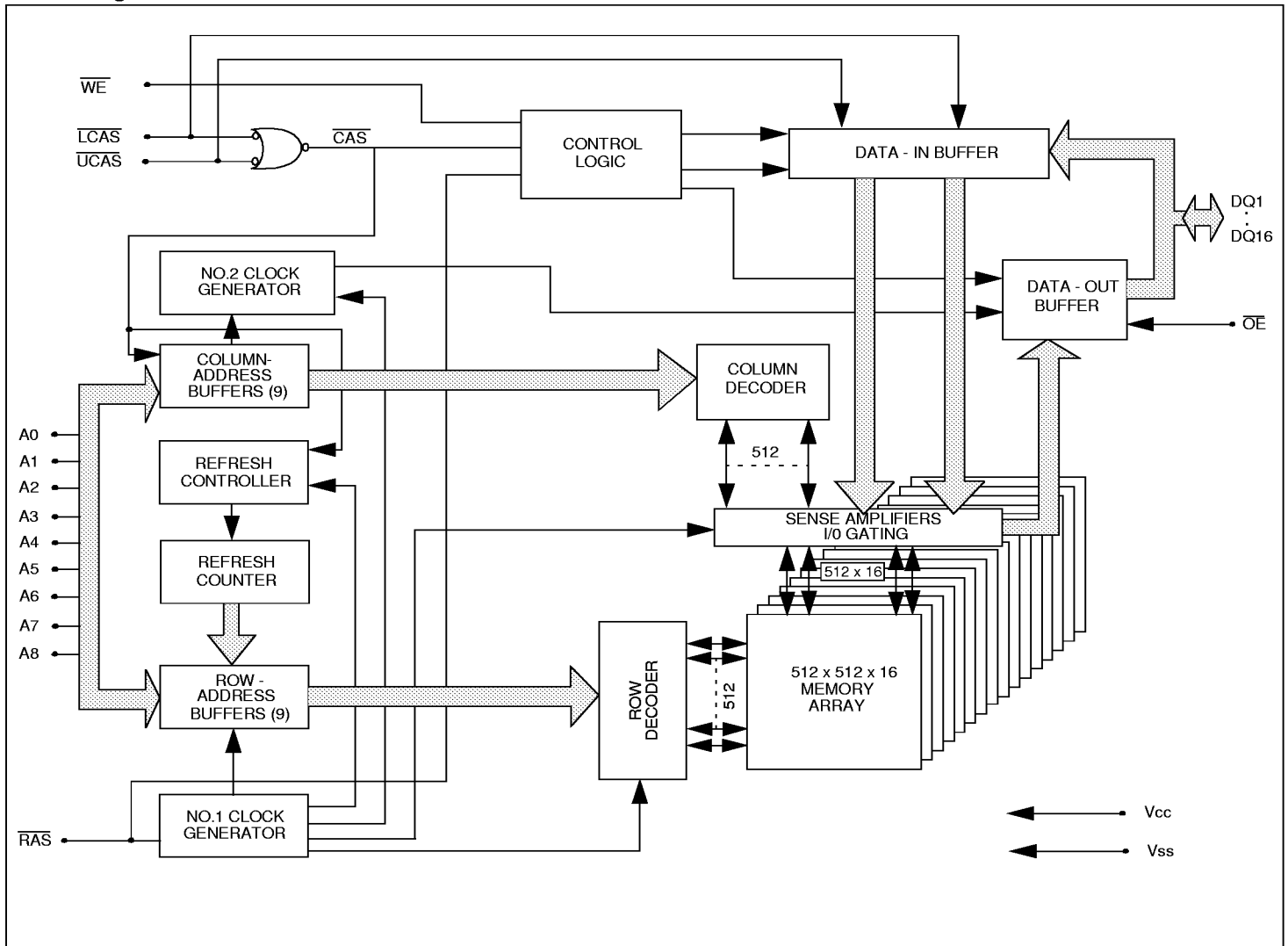
Pin Configuration 40-PIN 400 mil Plastic SOJ



Pin Description

Pin Name	Function
A0 - A8	Address inputs - Row address A0 - A8 - Column address A0 - A8 - Refresh address A0 - A8
DQ1 ~ DQ16	Data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+5V or +3.3V)
V_{SS}	Ground

Block Diagram



TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQ _S	Notes
							ROW	COL		
STANDBY		H	H → X	H → X	X	X	X	X	High-Z	
READ : WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ : LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte: Data-Out Upper Byte: High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte: High-Z Upper Byte: Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte: Data-In Upper Byte: High-Z	
WRITE : UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte: High-Z Upper Byte: Data-In	
READ WRITE		L	L	L	H → L	L → H	ROW	COL	Data-Out, Data-In	1,2
PAGE-MODE READ	1st Cycle	L	H → L	H → L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H → L	H → L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H → L	H → L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H → L	H → L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H → L	H → L	H → L	L → H	ROW	COL	Data-Out, Data-In	1,2
	2nd Cycle	L	H → L	H → L	H → L	L → H	n/a	COL	Data-Out, Data-In	1,2
HIDDEN REFRESH	READ	L → H → L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L → H → L	L	L	L	X	ROW	COL	Data-In	1,3
$\overline{\text{RAS}}$ -ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H → L	L	L	H	X	X	X	High-Z	4

Notes: 1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).

2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).

3. EARLY WRITE only.

4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vs.	V_T	5V - 0.5 to +7.0	V
3.3V		- 0.5 to +4.6	
Supply voltage relative to Vs.	V_{CC}	5V - 0.5 to +7.0	V
3.3V		- 0.5 to +4.6	
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to +70	°C
Storage temperature	T_{STG}	- 55 to +125	°C

Recommended DC Operating Conditions

Parameter/Condition	Symbol	5V Version			3.3V Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.4	-	$V_{CC}+0.3$	2.0	-	$V_{CC}+0.3$	V
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	-0.3	-	0.8	V

Capacitance

$T_a = 25^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$ or $3V \pm 10\%$, $f = 1\text{MHz}$

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{11}	-	5	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$)	C_{12}	-	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	-	7	pF	1,2

Note : 1. Capacitance measured with effective capacitance measuring method.

2. $\overline{\text{RAS}}$, $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}} = V_{IH}$ to disable Dout.

DC Characteristics: 5V Version

($T_a = 0$ to 70°C , $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	Test Conditions	VG264265CJ										Unit	Notes
			-25		-28		-3		-35		-4			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Operating current	I _{CC1}	$\overline{\text{RAS}}$ cycling $\overline{\text{LCAS}}, \overline{\text{UCAS}}$ cycling t _{RC} = min.	-	230	-	210	-	200	-	180	-	170	mA	1,2
Standby Current (TTL Interface)	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}} = V_{IH}$ Dout = High-Z	-	2	-	2	-	2	-	2	-	2	mA	
Standby current (CMOS Interface)		$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}}, \overline{\text{OE}} = V_{CC}-0.2V$ Dout = High-Z	-	1	-	1	-	1	-	1	-	1	mA	
$\overline{\text{RAS}}$ -only refresh current	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ t _{RC} = min.	-	230	-	210	-	200	-	180		170	mA	2
EDO page mode current	I _{CC4}	t _{RC} = min.	-	230	-	210	-	200	-	180		170	mA	1,3
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I _{CC5}	t _{RC} = min. $\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling	-	230	-	210	-	200	-	180		170	mA	2
Input leakage current	I _{LI}	0V < Vin < Vcc	-10	10	-10	10	-10	10	-10	10	-10	10	μA	
Output leakage current	I _{LO}	0V < Vout < Vcc Dout = Disable	-10	10	-10	10	-10	10	-10	10	-10	10	μA	
Output high voltage	V _{OH}	I _{OH} = -5mA	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	v	
Output low voltage	V _{OL}	I _{OL} = + 4.2mA	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	v	

Note :

1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. Address can be changed once or less while $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}} = V_{IH}$.

DC Characteristics: 3.3V Version

($T_a = 0$ to $+70^\circ\text{C}$, $V_{cc} = +3.3\text{V} \pm 10\%$, $V_{ss} = 0\text{V}$)

Parameter	Symbol	Test Conditions	VG26V265BJ						Unit	Notes
			-4		-5		-6			
			Min	Max	Min	Max	Min	Max		
Operating cur- rent	I _{cc1}	$\overline{\text{RAS}}$ cycling $\overline{\text{LCAS}}, \overline{\text{UCAS}}$ cycling t _{RC} = min	-	210	-	180	-	150	mA	1,2
Standby Current (TTL Interface)	I _{cc2}	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}} = V_{\text{IH}}$ Dout = High-Z	-	2	-	2	-	2	mA	
Standby current (CMOS Inter- face)		$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}}$ OE = V _{cc} -0.2V Dout = High-z	-	1	-	1	-	1	mA	
$\overline{\text{RAS}}$ -only refresh current	I _{cc3}	$\overline{\text{RA}}\text{c}l\text{ing}, \overline{\text{CAS}} = V_{\text{IH}}$ t _{RC} = min.	-	210	-	180	-	150	mA	2
Hyper page mode current	I _{cc4}	t _{PC} = min.	-	210	-	180	-	150	mA	1,3
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cur- rent	I _{cc5}	t _{RC} = min. $\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling	-	210	-	180	-	150	mA	2
Input leakage curent	I _{LI}	0V < V _{in} < V _{cc}	-10	10	-10	10	-10	10	μA	
Output leakage current	I _{LO}	0V < V _{OUT} < V _{CC} D _{OUT} = Disable	-10	10	-10	10	-10	10	μA	
Output high voltage	V _{OH}	I _{OH} = -5mA	2.4	-	2.4	-	2.4	-	V	
Output low Voltage	V _{OL}	I _{OL} = +4.2mA	-	0.4	-	0.4	-	0.4	V	

Note:

1. I_{CC} depends on output load condition when the device is selected. $I_{CC\text{max}}$ is specified at the output open condition.
2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. Address can be changed once or less while $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}} = V_{IH}$.
4. All the V_{CC} pins shall be shanged with the same voltage. And all the V_{SS} pins shall be supplied with the same vvoltage.

AC Characteristics: 5V Version

(Ta = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) * 1, * 2, * 3, * 4, * 5

- Input rise and fall times : 5ns
- Input pulse level : 0~3V
- Input timing reference levels : V_{IL} = 0.8, V_{IH} = 2.4V
- Oututload : one TTL load and 50pF
- Output reference levels : V_{OL} = 0.8V, V_{OH} = 2.0V

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	50	-	55	-	60	-	70	-	80	-	ns	
RAS precharge time	t _{RP}	15	-	18	-	20	-	25	-	30	-	ns	
LCAS/UCAS precharge time in normal mode	t _{CPN}	10	-	10	-	10	-	10	-	10	-	ns	22
RAS pulse width	t _{RAS}	25	10 ⁵	28	10 ⁵	30	10 ⁵	35	10 ⁵	40	10 ⁵	ns	6
LCAS/UCAS pulse width	t _{CAS}	5	10 ⁵	5	10 ⁵	5	10 ⁵	6	10 ⁵	6	10 ⁵	ns	7
Row address setup time	t _{ASR}	0	-	0	-	0	-	0	-	0	-	ns	
Row address hold time	t _{RAH}	5	-	5	-	5	-	6	-	6	-	ns	
Column address setup time	t _{ASC}	0	-	0	-	0	-	0	-	0	-	ns	8
Column address hold time	t _{CAH}	5	-	5	-	5	-	6	-	6	-	ns	
RAS to LCAS/UCAS delay time	t _{RCD}	11	17	11	19	11	21	12	25	12	29	ns	9
RAS to column address delay time	t _{RAD}	8	13	8	14	8	14	9	17	9	20	ns	10
Column address to RAS lead time	t _{RAL}	15	-	16	-	17	-	18	-	20	-	ns	
RAS hold time	t _{RSH}	6	-	6	-	6	-	6	-	6	-	ns	
LCAS/UCAS hold time	t _{CSH}	25	-	28	-	30	-	35	-	40	-	ns	
LCAS/UCAS to RAS precharge time	t _{CRP}	4	-	4	-	4	-	4	-	4	-	ns	11
OE to Din delay time	t _{OED}	6	-	6	-	7	-	7	-	8	-	ns	
Transition time (rise and fall)	t _T	1	50	1	50	1	50	1	50	1	50	ns	12
Refresh period	t _{REF}	-	8	-	8	-	8	-	8	-	8	ns	
CAS to output in Low-Z	t _{CLZ}	0	-	0	-	0	-	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from <u>RAS</u>	t _{RAC}	-	25	-	28	-	30	-	35	-	40	ns	13
Access time from <u>LCAS/UCAS</u>	t _{CAC}	-	8	-	9	-	9	-	10	-	11	ns	14,15
Access time from column address	t _{AA}	-	13	-	14	-	15	-	18	-	20	ns	15,16
Access time from <u>OE</u>	t _{OEA}	-	8	-	8	-	8	-	9	-	9	ns	
Read command setup time	t _{RCS}	0	-	0	-	0	-	0	-	0	-	ns	8
Read command hold time to <u>LCAS/UCAS</u>	t _{RCH}	0	-	0	-	0	-	0	-	0	-	ns	11,17
Read command hold time to <u>RAS</u>	t _{RRH}	0	-	0	-	0	-	0	-	0	-	ns	17
Output buffer turn-off time	t _{OFF}	0	6	0	6	0	7	0	7	-	8	ns	18
Output buffer turn-off time from <u>OE</u>	t _{OEZ}	0	6	0	6	0	7	0	7	-	8	ns	18

Write Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	-	0	-	0	-	0	-	0	-	ns	8,19
Write command hold time	t _{WCH}	5	-	5	-	5	-	6	-	6	-	ns	
Write command pulse width	t _{WP}	5	-	5	-	5	-	6	-	6	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	10	-	10	-	10	-	10	-	10	-	ns	
Write command to $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ lead time	t _{CWL}	6	-	6	-	6	-	7	-	7	-	ns	20
Data-in setup time	t _{DS}	0	-	0	-	0	-	0	-	0	-	ns	21
Data-in hold time	t _{DH}	4	-	4	-	5	-	6	-	7	-	ns	21
$\overline{\text{WE}}$ to Data-in delay	t _{WED}	6	-	6	-	6	-	6	-	7	-	ns	

Read-Modify-Write Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	85	-	90	-	94	-	100	-	110	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	43	-	46	-	48	-	53	-	58	-	ns	19
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ to $\overline{\text{WE}}$ dealy time	t _{CWD}	25	-	26	-	27	-	28	-	29	-	ns	19
Column address to $\overline{\text{WE}}$ dealy time	t _{AWD}	32	-	33	-	34	-	36	-	38	-	ns	19
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OEH}	6	-	6	-	6	-	6	-	7	-	ns	

Refresh Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ setup time (CBR refrsh)	t _{CSR}	5	-	5	-	5	-	5	-	5	-	ns	
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ hold time (CBR refrsh)	t _{CHR}	10	-	10	-	10	-	10	-	10	-	ns	11
$\overline{\text{RAS}}$ precharge to $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ hold time	t _{RPC}	5	-	5	-	5	-	5	-	5	-	ns	8

EDO Page Mode Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t _{PC}	10	-	11	-	12	-	15	-	16	-	ns	
EDO page mode $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge time	t _{CP}	4	-	4	-	4	-	5	-	6	-	ns	22
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	25	10 ⁵	28	10 ⁵	30	10 ⁵	35	10 ⁵	40	10 ⁵	ns	23
Access time from $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge	t _{CPA}	-	17	-	18	-	19	-	22	-	25	ns	11,15
$\overline{\text{RAS}}$ hold time from $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge	t _{CPRH}	25	-	25	-	25	-	25	-	28	-	ns	
$\overline{\text{OE}}$ high hold time from $\overline{\text{CAS}}$ high	t _{OEHC}	5	-	5	-	5	-	7	-	7	-	ns	
$\overline{\text{OE}}$ high pulse width	t _{OEP}	5	-	5	-	5	-	7	-	7	-	ns	
Data output hold after $\overline{\text{CAS}}$ low	t _{COH}	3	-	3	-	3	-	3	-	3	-	ns	
Output disable delay from $\overline{\text{WE}}$	t _{WHZ}	0	12	0	12	0	13	0	13	0	13	ns	
$\overline{\text{WE}}$ pulse width for output disable when $\overline{\text{CAS}}$ high	t _{WPZ}	7	-	7	-	7	-	7	-	7	-	ns	
$\overline{\text{OE}}$ low to $\overline{\text{CAS}}$ high setup time	t _{OES}	5	-	5	-	5	-	5	-	5	-	ns	

EDO Page Mode Read Modify Write Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle <u>LCAS/UCAS</u> precharge to <u>WE</u> delay time	t _{CPW}	44	-	44	-	44	-	46	-	46	-	ns	11
EDO page mode read-modify-write cycle time	t _{PRWC}	40	-	43	-	45	-	50	-	56	-	ns	

AC Characteristics: 3.3V Version

(Ta = 0 to +70°C, V_{CC} = 3.3V ± 10%, V_{SS} = 0V) *1, *2, *3, *4, *5

Test conditions

- Input rise and fall times : 5ns
- Input pulse level : 0~3V
- Input timing reference levels : V_{IL} = 0.8, V_{IH} = 2.0V
- Output load : one TTL load and 50pF
- Output reference levels : V_{OL} = 0.8V, V_{OH} = 2.0V

Read, Write, Read - Modify - Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	80	-	95	-	110	-	ns	
RAS precharge time	t _{RP}	30	-	40	-	50	-	ns	
LCAS/UCAS precharge time in normal mode	t _{CPN}	10	-	10	-	10	-	ns	22
RAS pulse width	t _{RAS}	40	10 ⁵	50	10 ⁵	60	10 ⁵	ns	6
LCAS/UCAS pulse width	t _{CAS}	6	10 ⁵	8	10 ⁵	10	10 ⁵	ns	7
Row adress setup time	t _{ASR}	0	-	0	-	0	-	ns	
Row adress hold time	t _{RAH}	6	-	8	-	10	-	ns	
Column address setup time	t _{ASC}	0	-	0	-	0	-	ns	8
Column address hold time	t _{CAH}	6	-	8	-	10	-	ns	
RAS to LCAS/UCAS delay time	t _{RCD}	12	29	13	36	14	45	ns	9
RAS to column address delay time	t _{RAD}	9	20	11	25	12	30	ns	10
Column address to RAS lead time	t _{RAL}	20	-	24	-	30	-	ns	
RAS hold time	t _{RSH}	6	-	8	-	10	-	ns	
LCAS/UCAS hold time	t _{CSH}	30	-	35	-	40	-	ns	
LCAS/UCAS to RAS precharge time	t _{CRP}	4	-	5	-	5	-	ns	11
OE to Din delay time	t _{OED}	8	-	8	-	10	-	ns	
Transition time (rise and fall)	t _T	1	50	1	50	1	50	ns	12
Refresh period	t _{REF}	-	8	-	8	-	8	ms	
CAS to output in Low - Z	t _{CLZ}	0	-	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	-	40	-	50	-	60	ns	13
Access time from $\overline{\text{LCAS/UCAS}}$	t_{CAC}	-	13	-	14	-	15	ns	14,15
Access time from column/address	t_{AA}	-	20	-	25	-	30	ns	15,16
Access time from $\overline{\text{OE}}$	t_{OEA}	-	10	-	12	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	0	-	ns	8
Read command hold time to $\overline{\text{LCAS/UCAS}}$	t_{RCH}	0	-	0	-	0	-	ns	11,17
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	-	0	-	0	-	ns	17
Output buffer turn-off time	t_{OFF}	-	8	0	8	0	10	ns	18
Output buffer turn-off time from $\overline{\text{OE}}$	t_{OEZ}	-	8	0	8	0	10	ns	18

Write Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	-	0	-	0	-	ns	8,19
Write command hold time	t _{WCH}	6	-	7	-	10	-	ns	
Write command pulse width	t _{WP}	6	-	7	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t _{RWL}	10	-	12	-	15	-	ns	
Write command to $\overline{LCAS}/\overline{UCAS}$ lead time	t _{CWL}	7	-	8	-	10	-	ns	20
Data-in setup time	t _{DS}	0	-	0	-	0	-	ns	21
Data-in hold time	t _{DH}	7	-	8	-	10	-	ns	21
$\overline{WE}$ to Data-in delay	t _{WED}	7	-	8	-	8	-	ns	

Read - Modify - Write Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	110	-	126	-	140	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	58	-	68	-	77	-	ns	19
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ to $\overline{\text{WE}}$ dealy time	t _{CWD}	29	-	30	-	32	-	ns	19
Column address to $\overline{\text{WE}}$ dealy time	t _{AWD}	38	-	43	-	47	-	ns	19
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OEH}	7	-	8	-	10	-	ns	

Refresh Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
$\overline{LCAS}/\overline{UCAS}$ setup time (CBR refresh)	t _{CSR}	5	-	5	-	5	-	ns	
$\overline{LCAS}/\overline{UCAS}$ hold time (CBR refresh)	t _{CHR}	10	-	10	-	10	-	ns	11
$\overline{RAS}$ precharge to $\overline{LCAS}/\overline{UCAS}$ hold time	t _{RPC}	5	-	5	-	5	-	ns	8

EDO Page Mode Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t _{PC}	16	-	20	-	25	-	ns	
EDO page mode $\overline{LCAS}/\overline{UCAS}$ precharge time	t _{CP}	6	-	8	-	10	-	ns	22
EDO page mode $\overline{RAS}$ pulse width	t _{RASP}	40	10 ⁵	50	10 ⁵	60	10 ⁵	ns	23
Access time from $\overline{LCAS}/\overline{UCAS}$ precharge	t _{CPA}	-	25	-	30	-	35	ns	11,15
$\overline{RAS}$ hold time from $\overline{LCAS}/\overline{UCAS}$ pre-charge	t _{CPRH}	28	-	30	-	35	-	ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ high	t _{OEHC}	7	-	8	-	10	-	ns	
$\overline{OE}$ high pulse width	t _{OEP}	7	-	7	-	10	-	ns	
Data output hold after $\overline{CAS}$ low	t _{COH}	3	-	3	-	3	-	ns	
Output disable delay from $\overline{WE}$	t _{WHZ}	0	13	0	13	0	13	ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ high	t _{WPZ}	7	-	7	-	7	-	ns	
$\overline{OE}$ low to $\overline{CAS}$ high setup time	t _{OES}	5	-	5	-	5	-	ns	

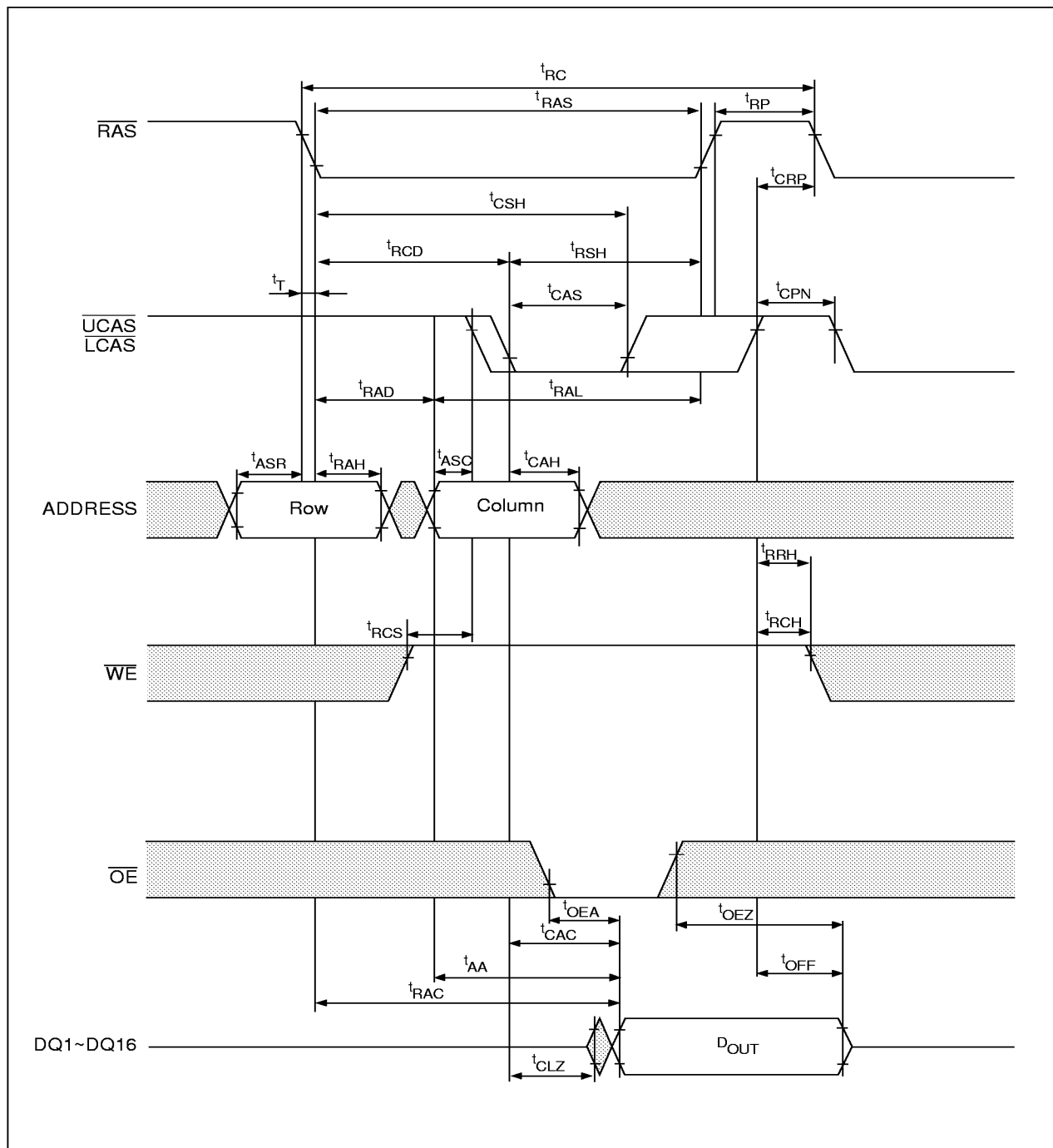
EDO Page Mode Read Modify Write Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle LCAS / UCAS precharge to WE delaycycle time	t _{CPW}	46	-	48	-	55	-	ns	11
EDO page mode read-modify-write cycle time	t _{PRWC}	56	-	64	-	66	-	ns	

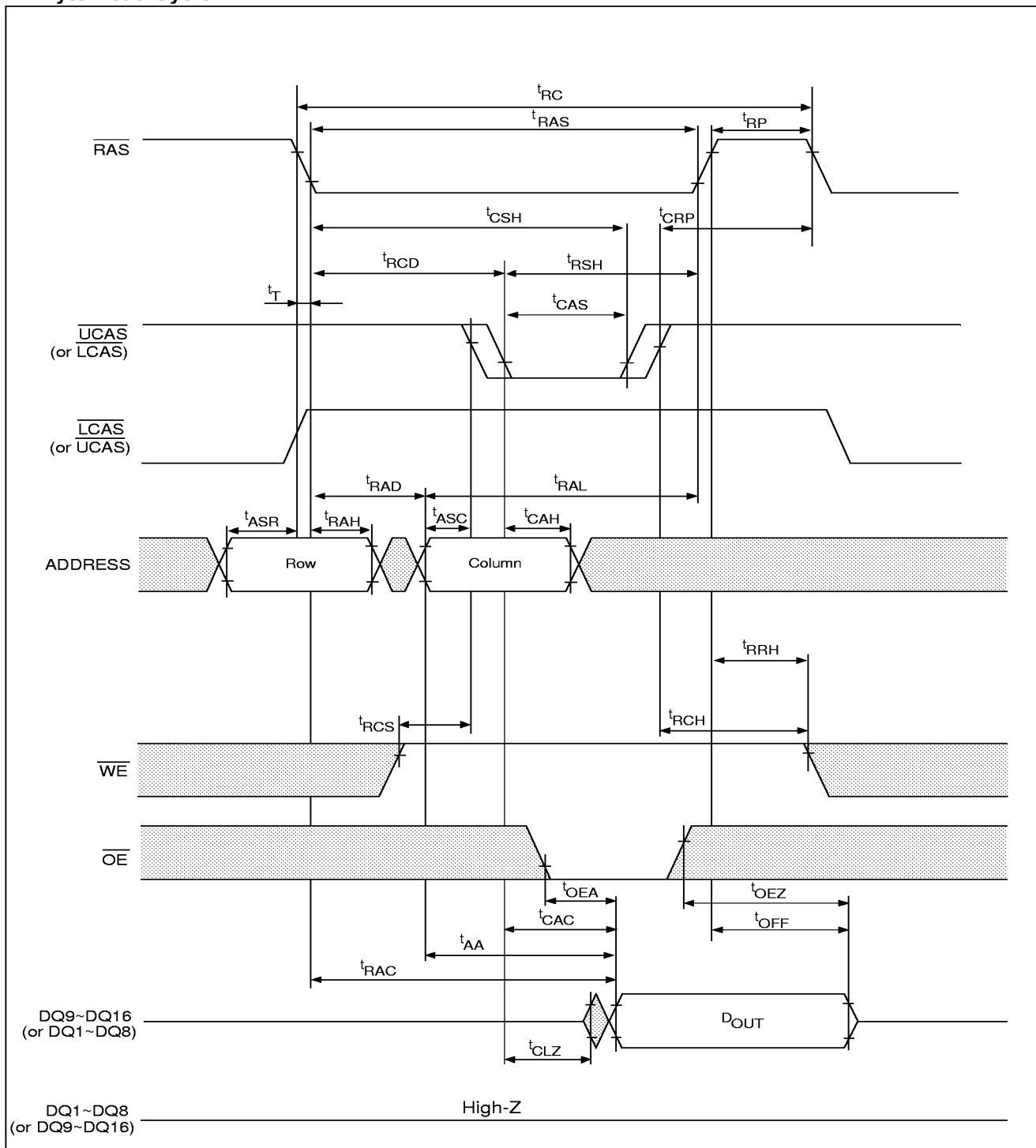
Notes :

1. AC measurements assume $t_T = 5\text{ns}$.
2. An initial pause of $100\ \mu\text{S}$ is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycles or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
3. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
4. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be staggered within the same write/read cycles.
5. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
6. $t_{\text{RAS}}(\text{min}) = t_{\text{RWD}}(\text{min}) + t_{\text{RWL}}(\text{min}) + t_T$ in read-modify-write cycle.
7. $t_{\text{CAS}}(\text{min}) = t_{\text{CWD}}(\text{min}) + t_{\text{CWL}}(\text{min}) + t_T$ in read-modify-write cycle.
8. $t_{\text{ASC}}(\text{min})$, $t_{\text{RCS}}(\text{min})$, $t_{\text{WCS}}(\text{min})$ and t_{RPC} are determined by the falling edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
9. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
10. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
11. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
12. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing or input signals. Also, transition times are measured between V_{IH} and V_{IL} .
13. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
14. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
15. Access time is determined by the longer of t_{AA} , t_{CAC} and t_{CPA} . t_{CAC} is guaranteed for one TTL and 50pF load.
16. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
17. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
18. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. t_{OFF} is determined by the later rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$.
19. t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
20. t_{CWL} shall be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$.
21. These parameters are referenced to $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ separately in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
22. t_{CPN} and t_{CP} are determined by the time that both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high.
23. t_{RASp} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.

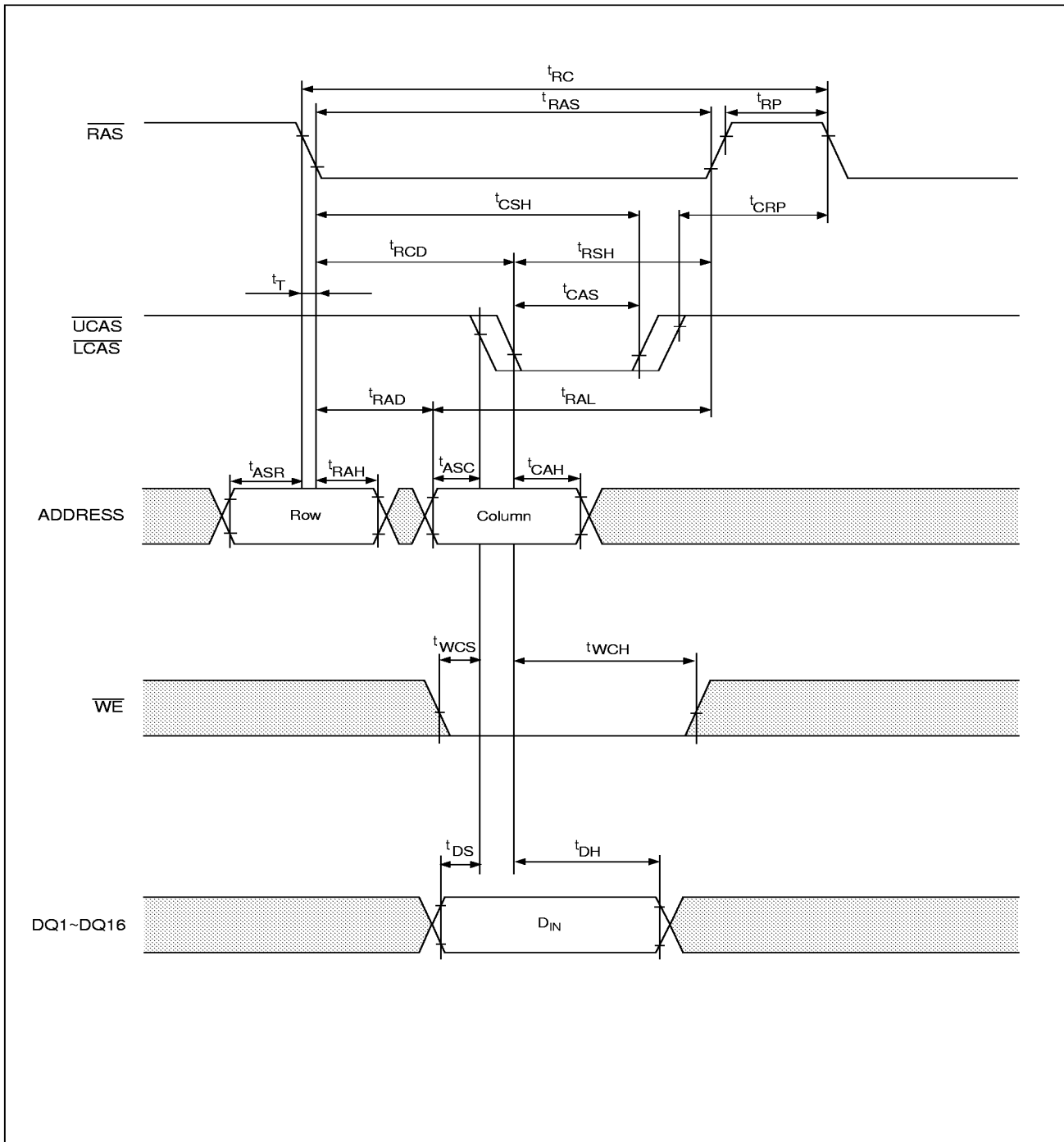
Timing Waveforms • Word Read Cycle



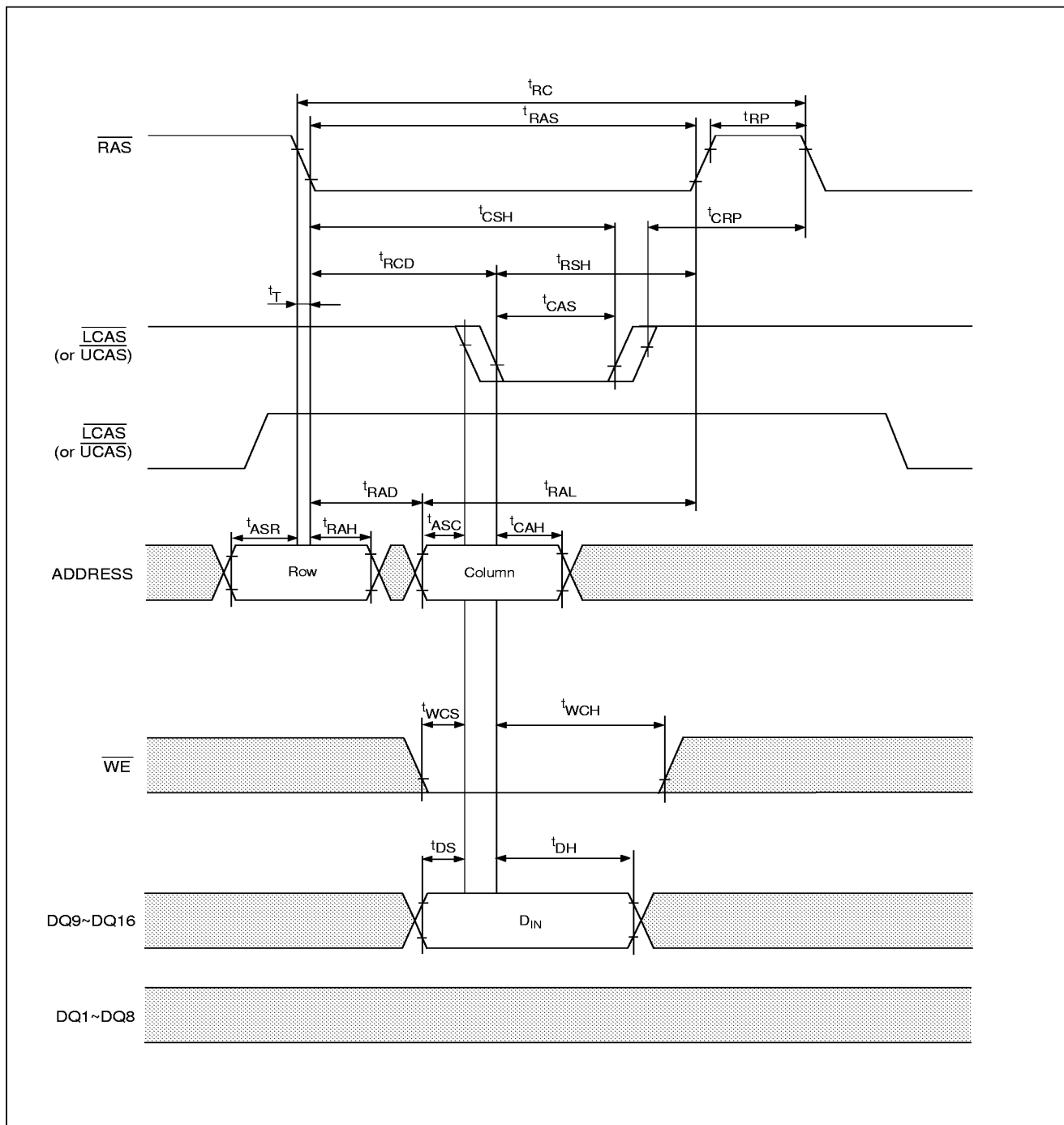
• Byte Read Cycle



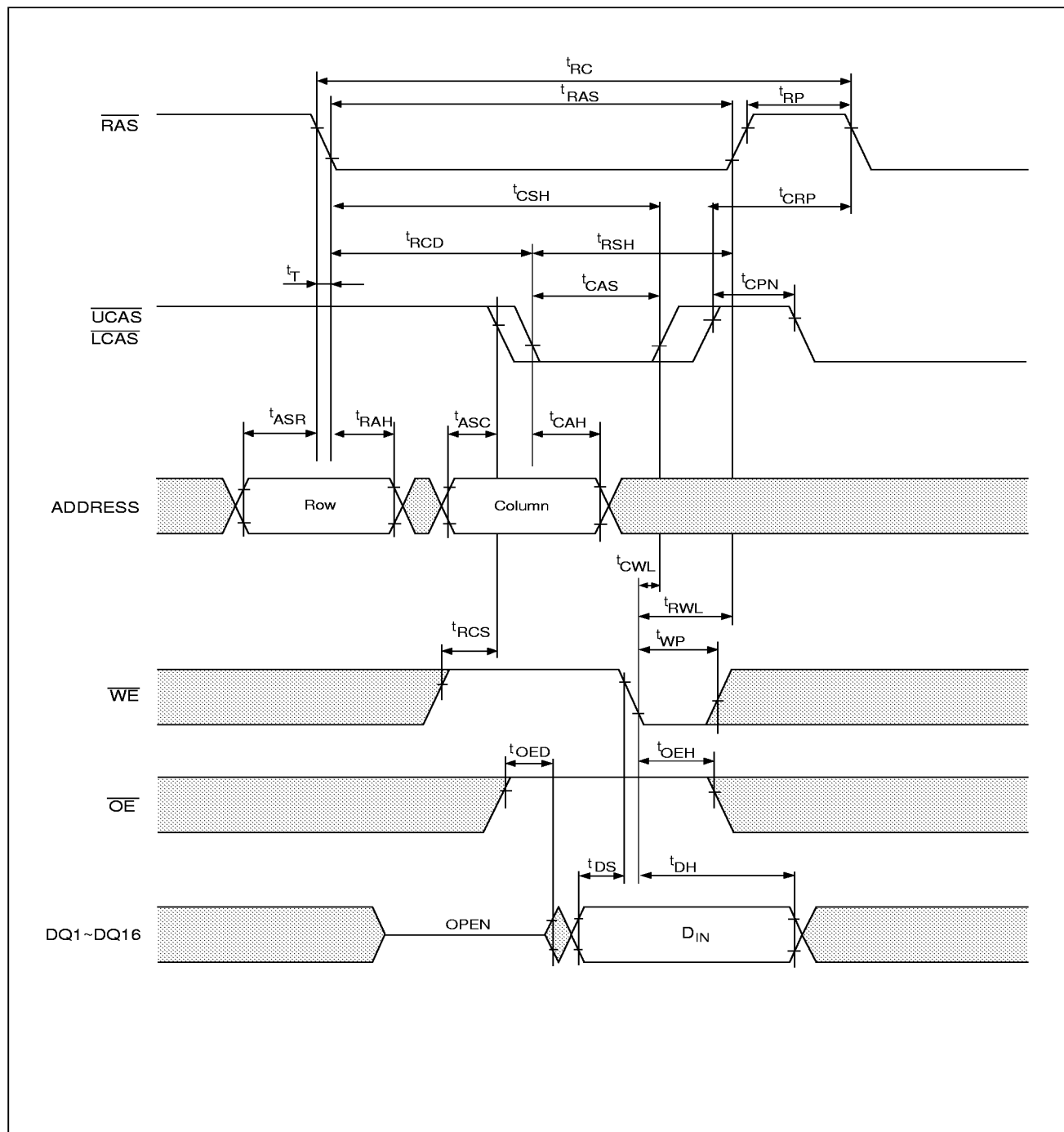
• Word Early Write Cycle



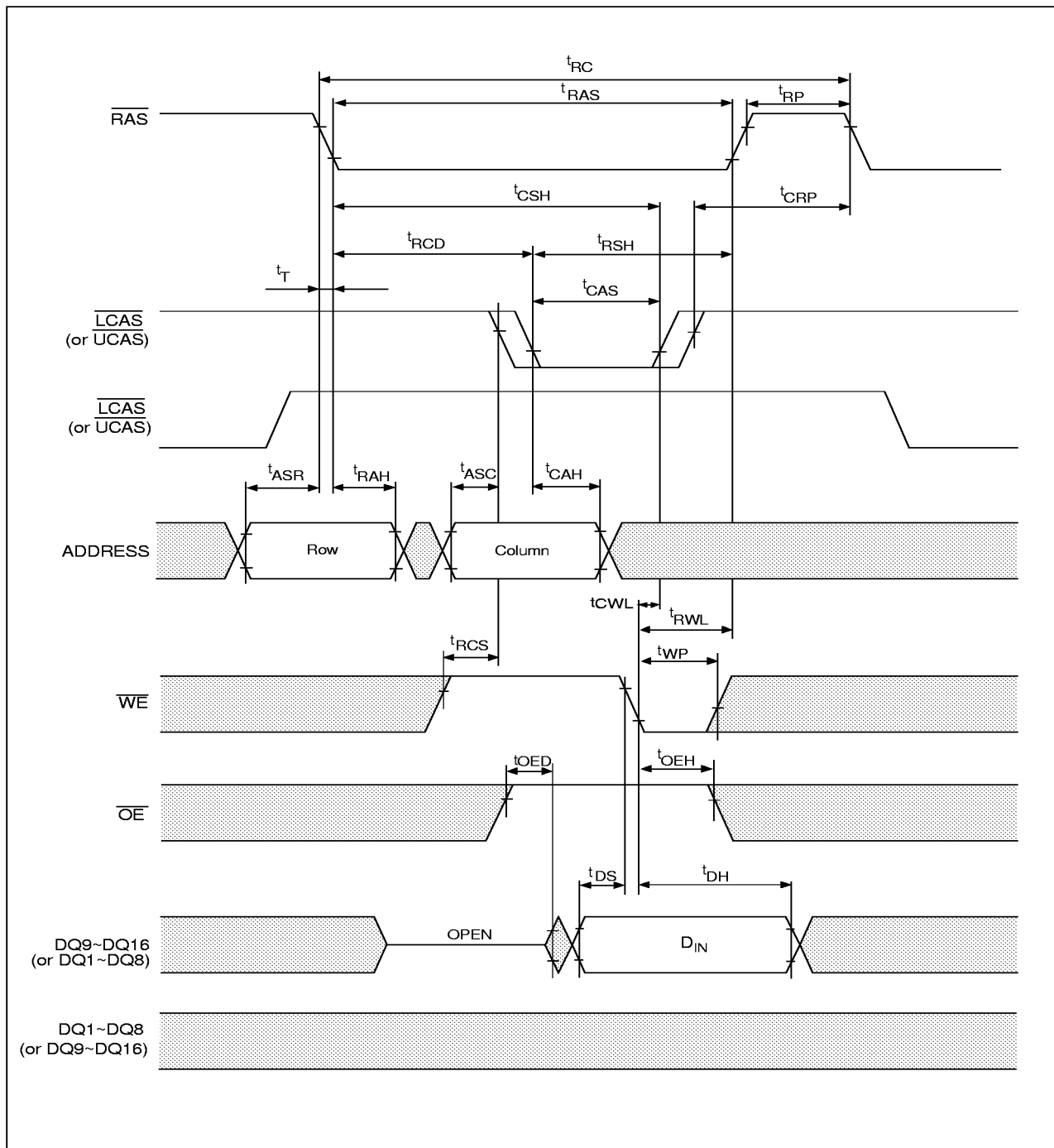
• Byte Early Write Cycle



• Word Delayed Write Cycle

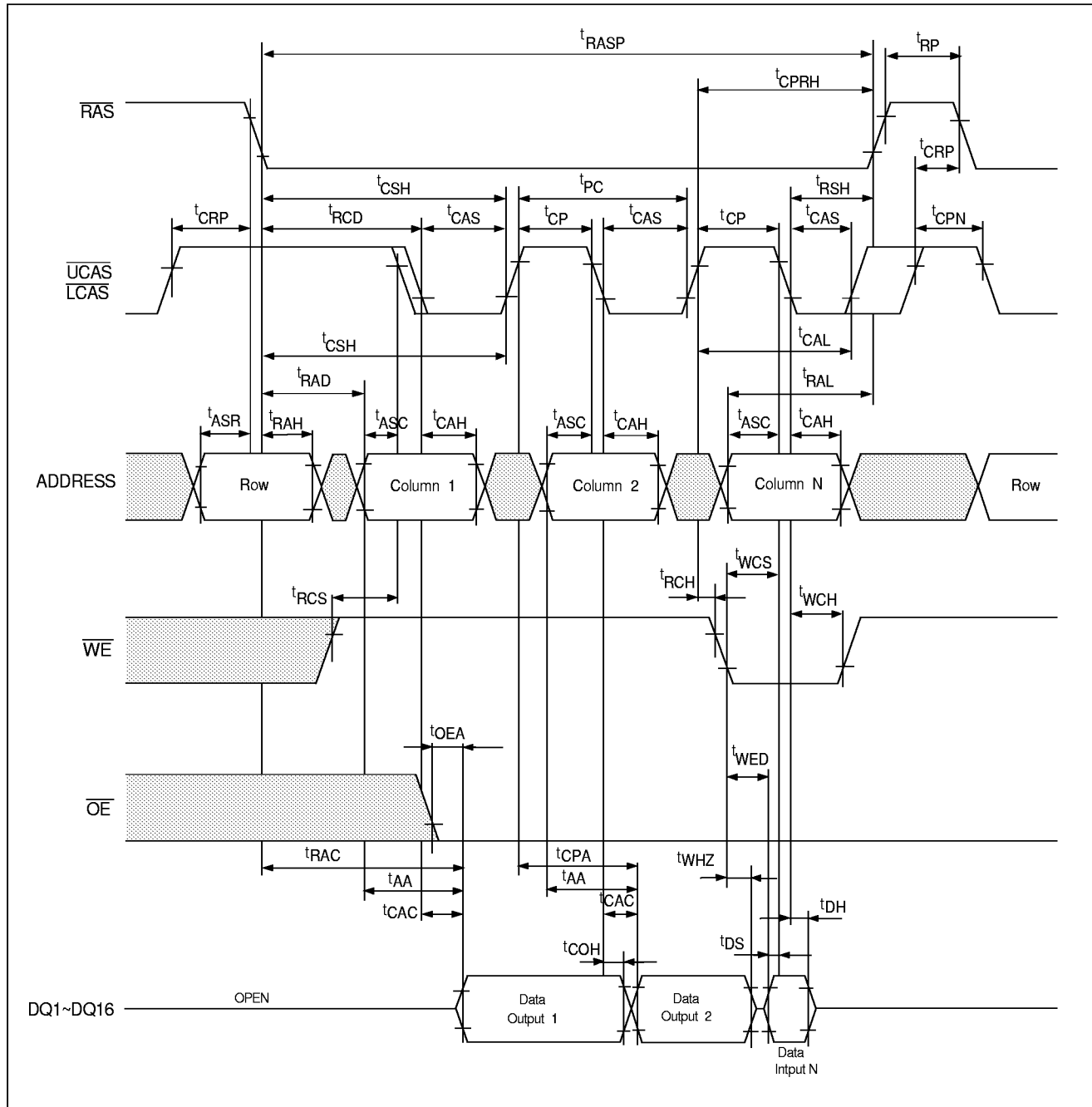


• Byte Delayed Write Cycle

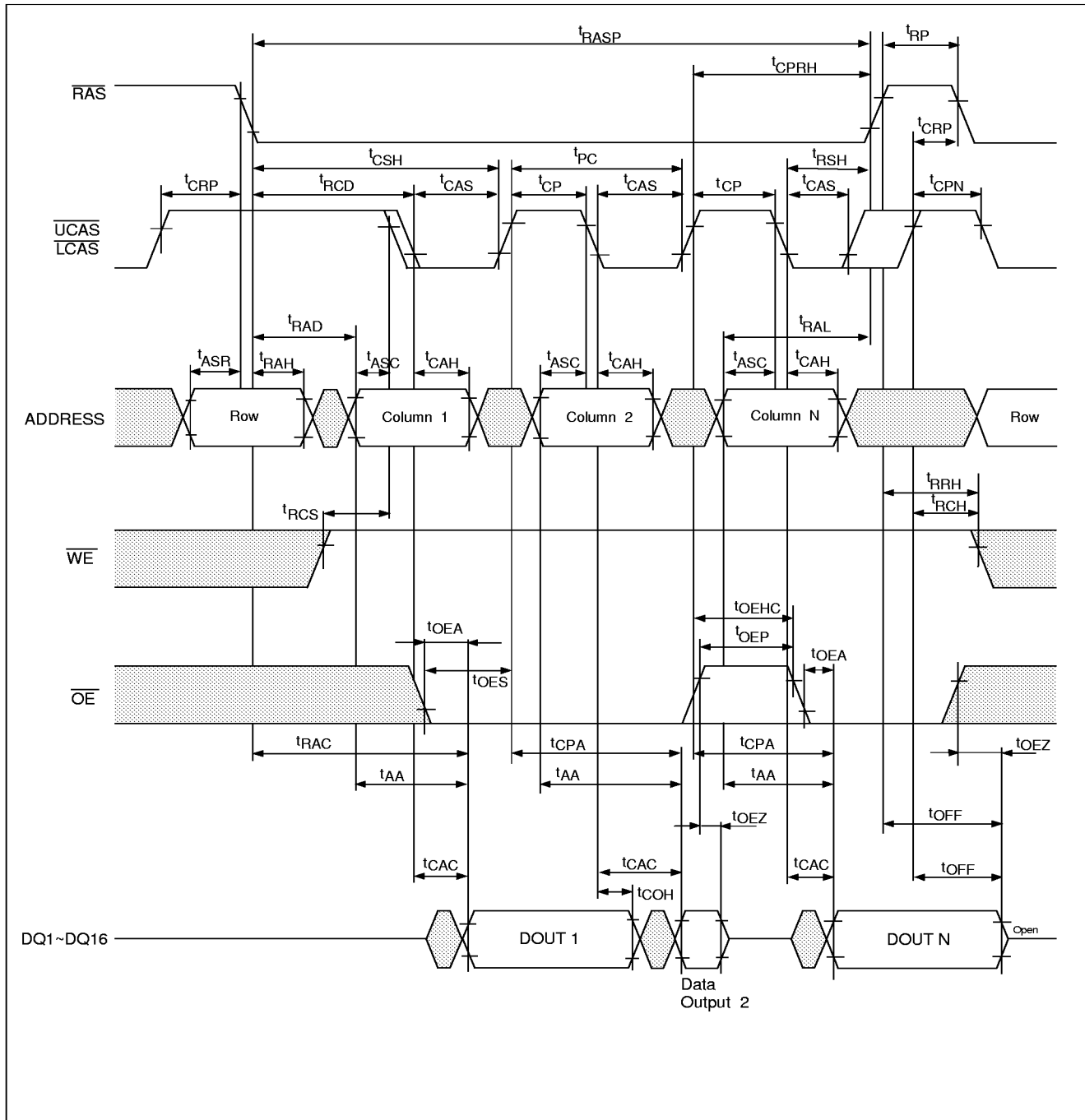


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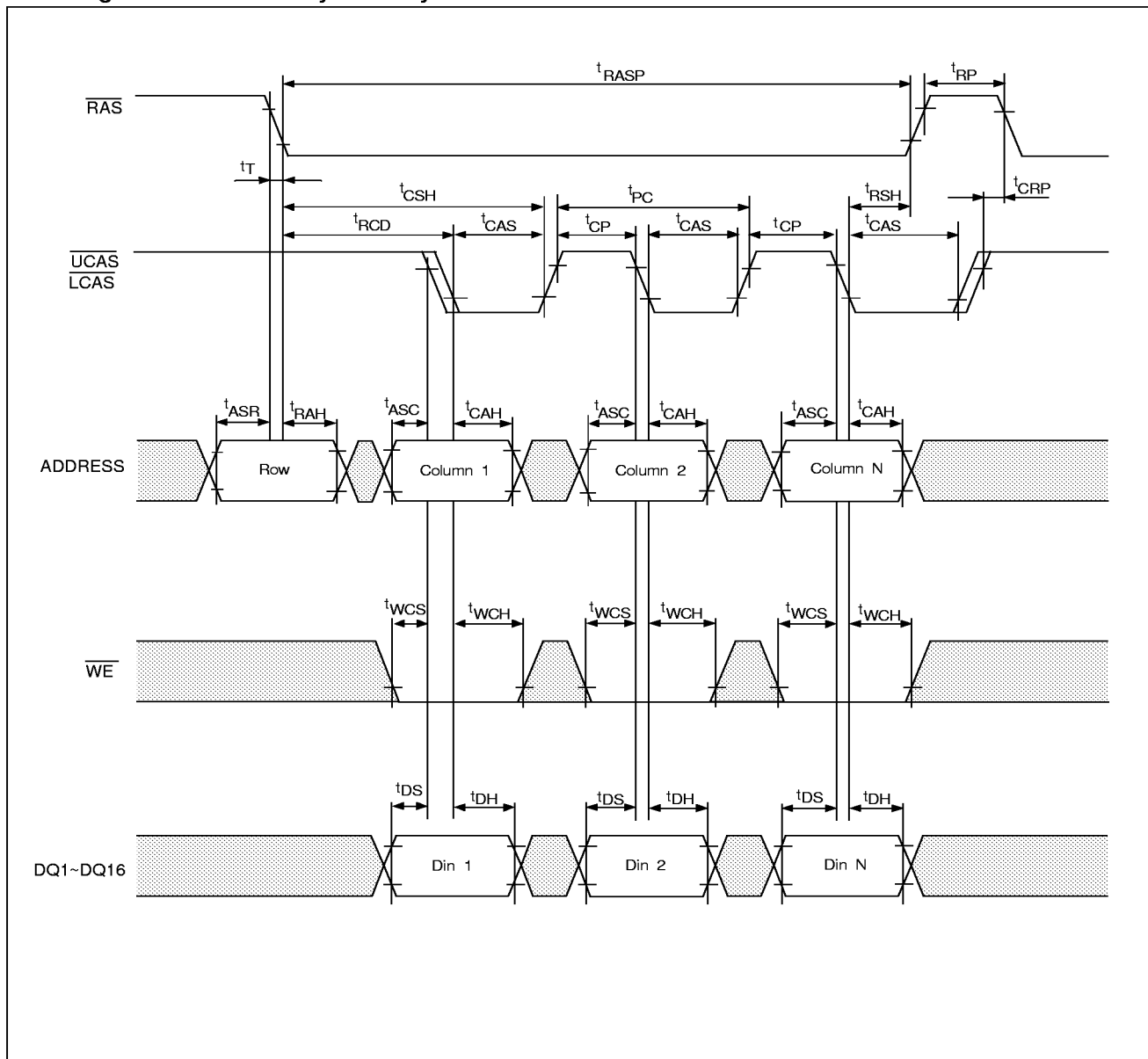
• EDO Page Mode Word Read-Early-Write Cycle



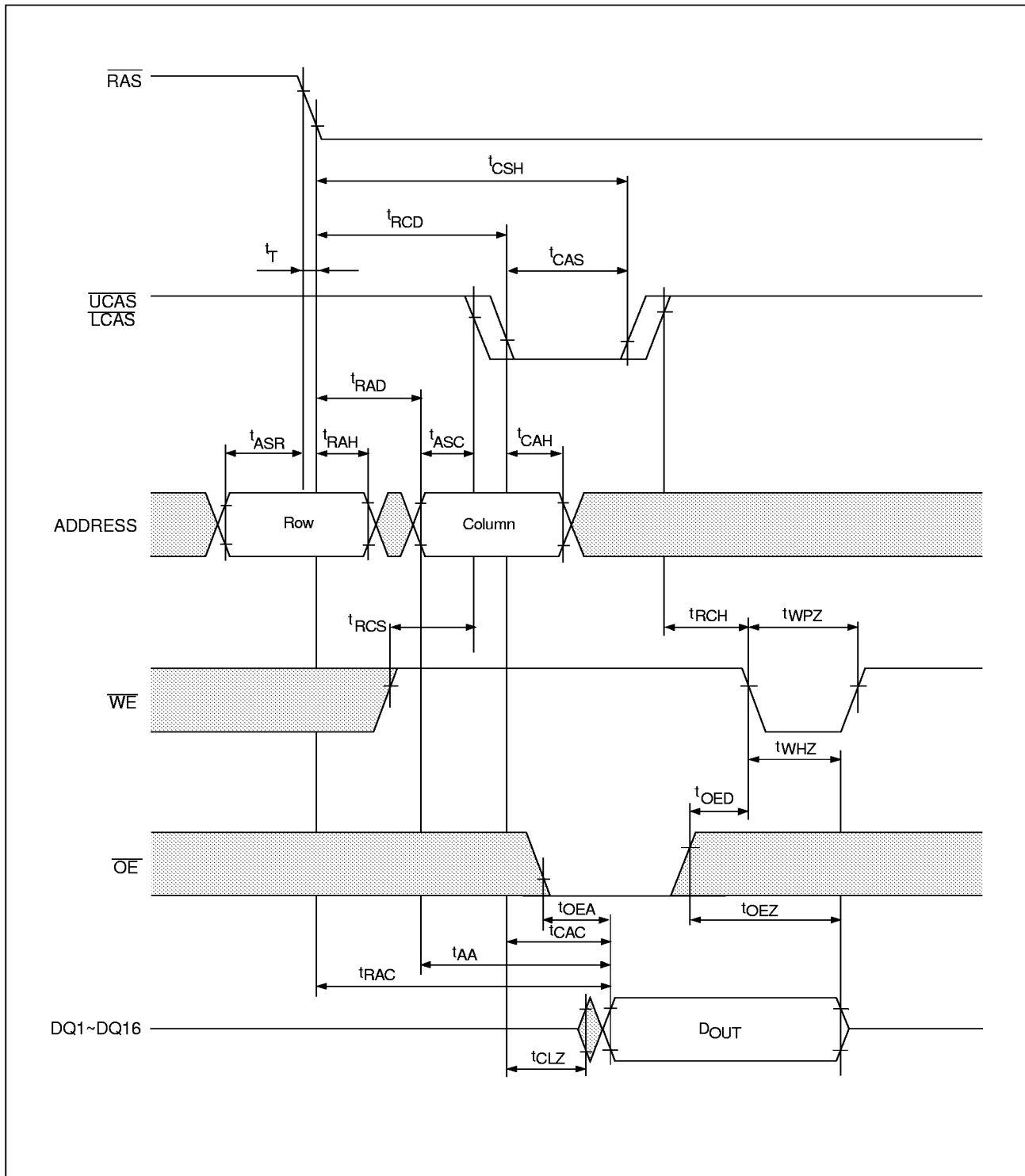
- EDO Page Mode Word Read Cycle



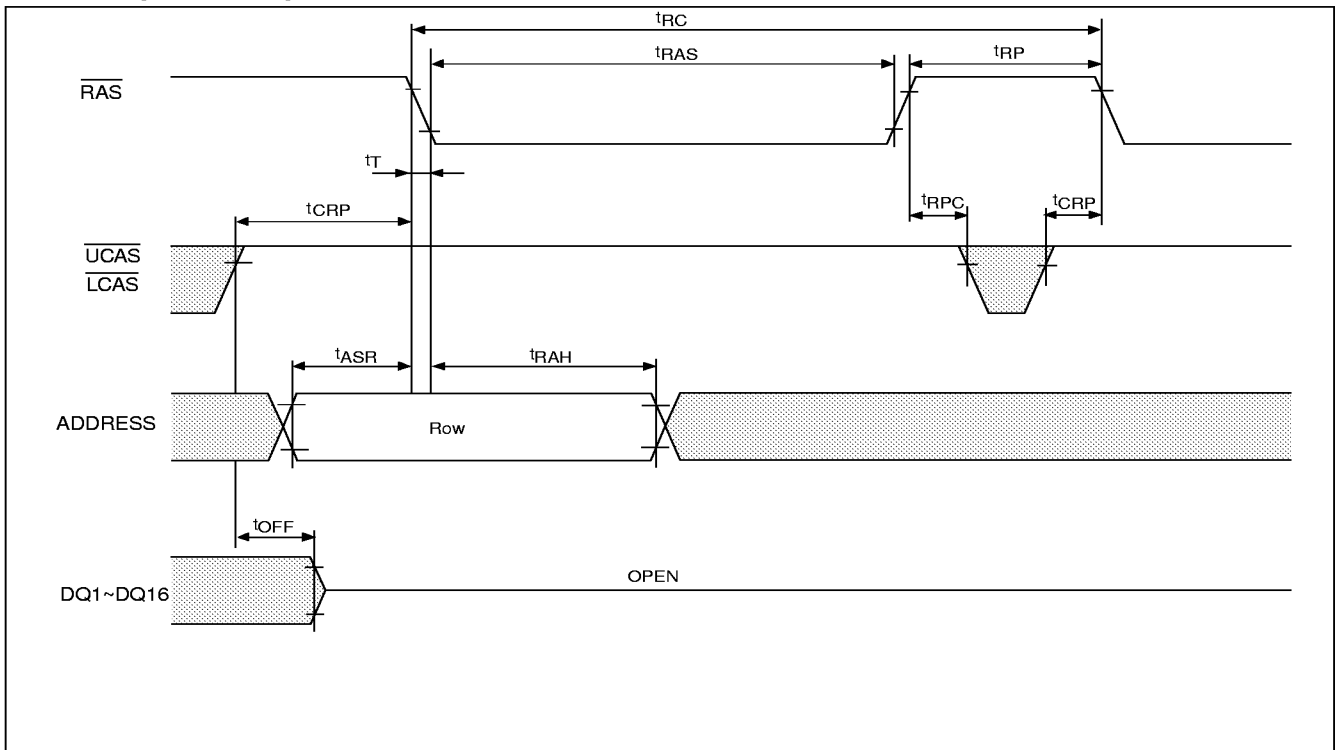
• EDO Page Mode WORD Early Write Cycle



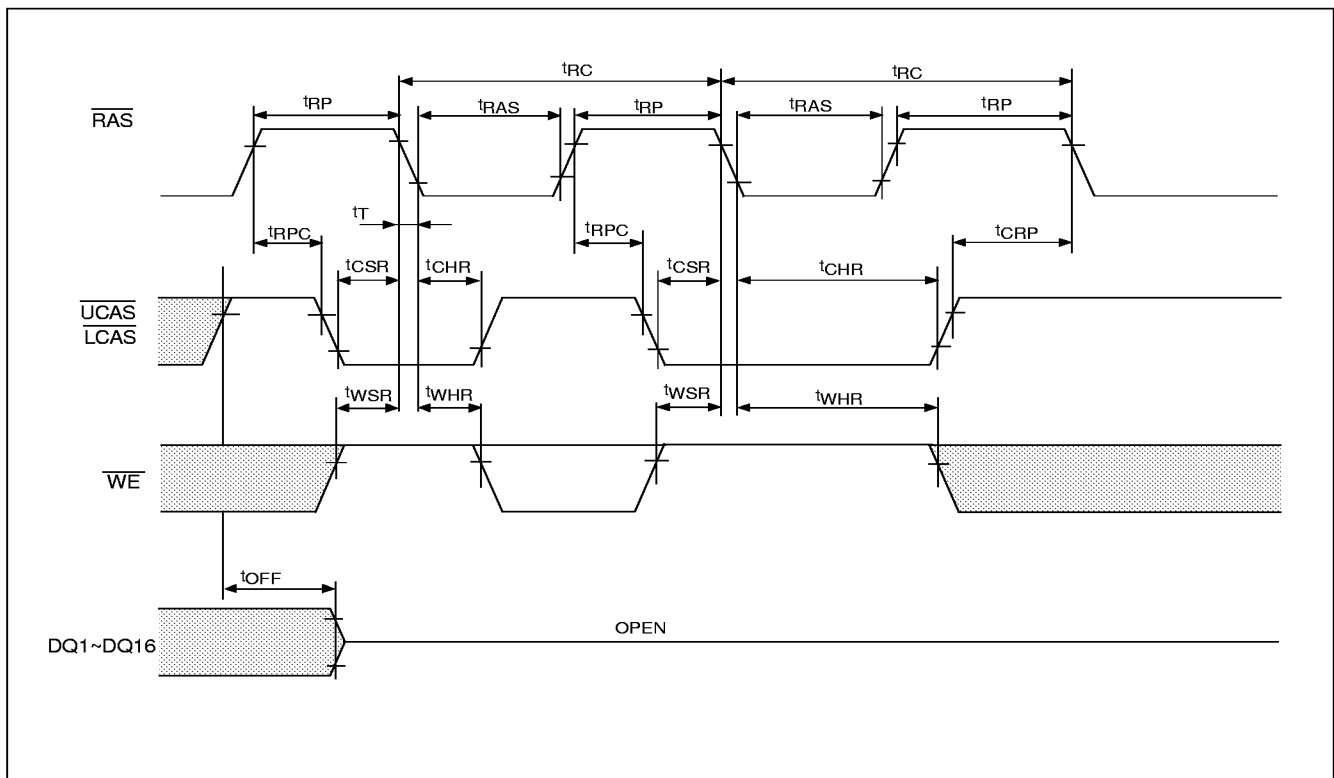
• Read Cycle with $\overline{\text{WE}}$ Controlled Disable



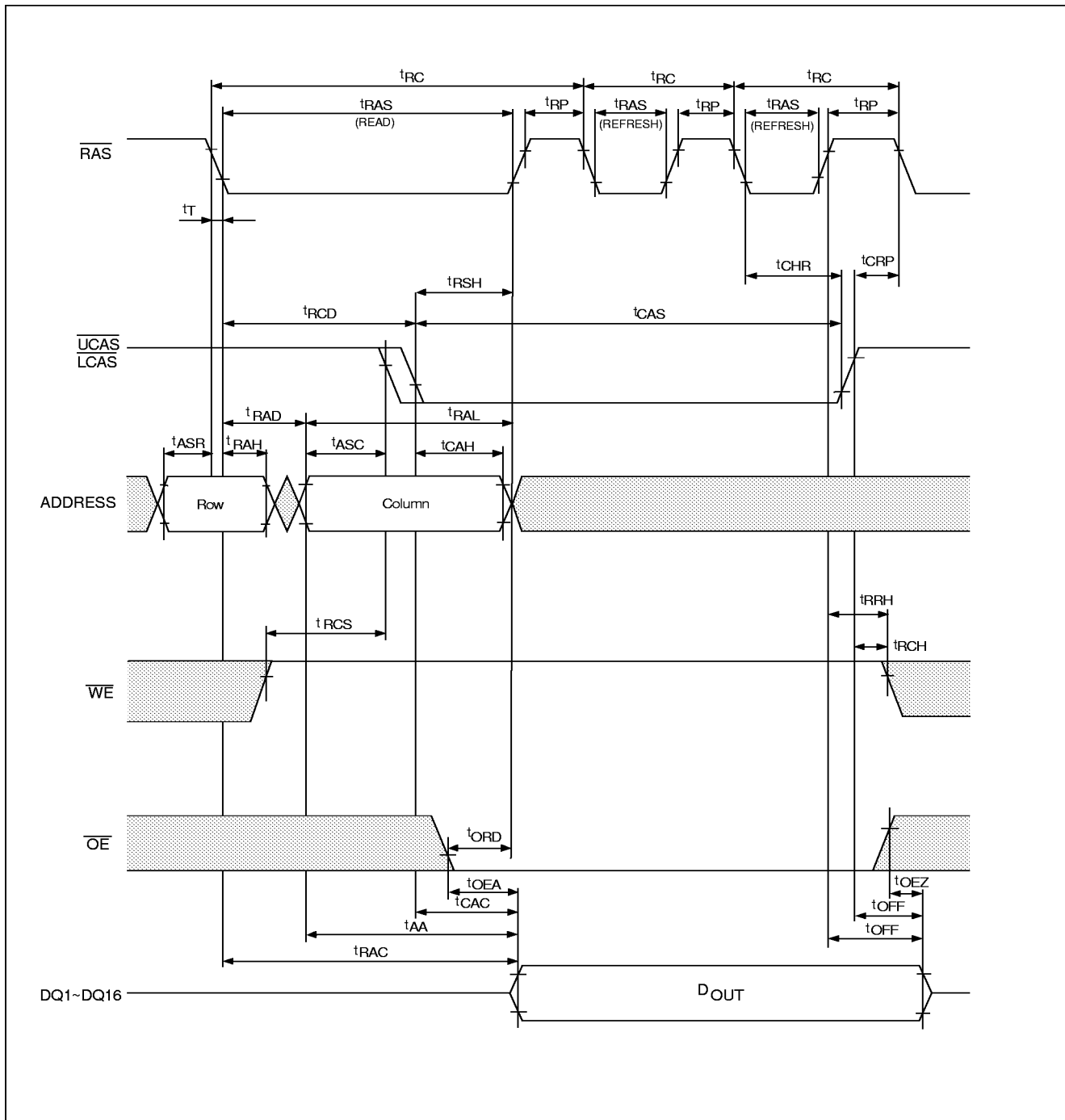
$\overline{\text{RAS}}$ - Only Refresh Cycle



$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle



• Hidden Refresh Cycle



Ordering information

Part Number	Access Time	Package
VG264265CJ - 25	25 ns	400mil 40 - Pin Plastic SOJ
VG264265CJ - 28	28 ns	
VG264265CJ - 3	30 ns	
VG264265CJ - 35	35 ns	
VG26(V)4265CJ - 4	40 ns	
VG26V4265CJ - 5	50 ns	
VG26V4265CJ - 6	60 ns	

VG26(V)4265CJ - 3

- VG → • VIS Memory Product
- 26 → • Technology/Design Rule
- V → • 3.3V Version
- 4265 → • Device Type/Configuration
- C → • Mask/Design Version
- J → • Package Type, J : SOJ
- 3 → • Speed -5V: 25, 28, 30, 35, 40ns
-3.3V: 40, 50, 60ns

Packaging Information

- 400mil, 40-pin Plastic SOJ

