National Semiconductor

DM77/87SR183
(1k x 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR183 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 1024 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR183 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

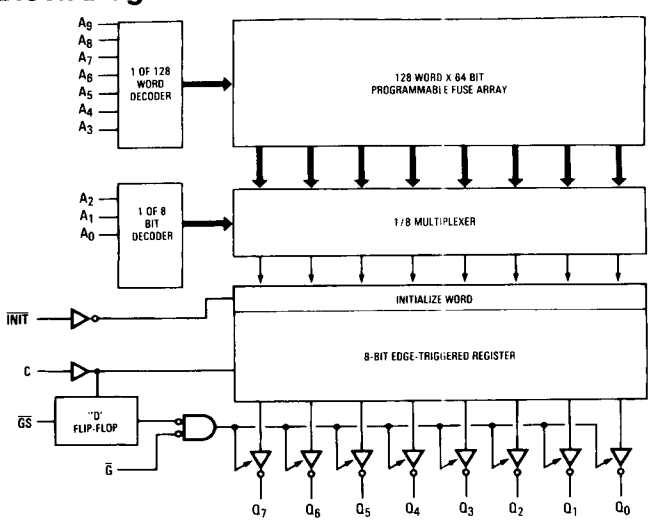
The DM77/87SR183 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S35
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



TL/D/8351–1

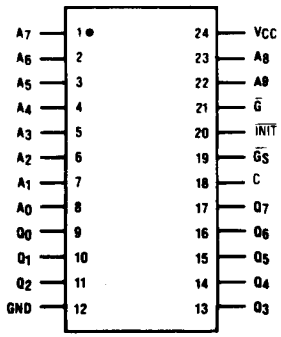
Pin Names

A0–A9	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
$\overline{INIT}$	Initialize
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

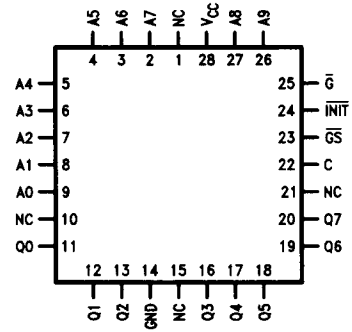


TL/D/8351–2

Top View

Order Number DM77/87SR183J, 183BJ, DM87SR183N or 183BN
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/8351–8

Top View

Order Number DM87SR183V or 183BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM87SR183BJ	35
DM87SR183J	40
DM87SR183BN	35
DM87SR183N	40
DM87SR183BV	35
DM87SR183V	40

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM77SR183BJ	40
DM77SR183J	45

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating to be determined	

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR183, 183B			DM87SR183, 183B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_1	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR183, 183B			DM87SR183, 183B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR183	45	20		40	20		ns
		SR183B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR183		15	30		15	25	ns
		SR183B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		20	10		15	10		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		15	0		15	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	35		20	30	ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		30	10		25	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to C (High)		20	10		20	10		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			20	35		20	30	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.