National Semiconductor Corporation

DM77/87SR476, DM77/87SR25, DM77/87SR476B, DM77/87SR25B (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR476 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR476 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

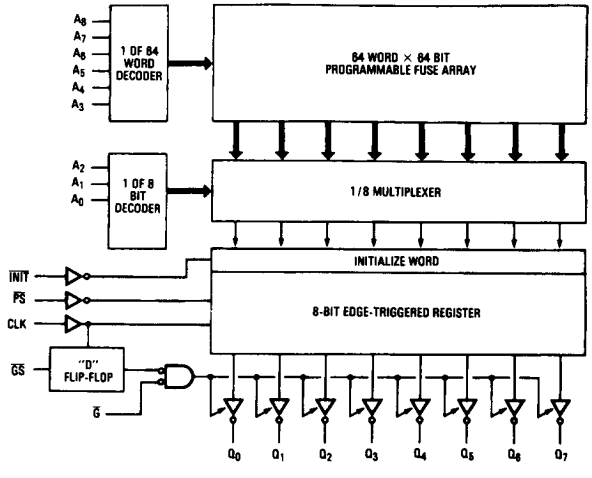
The DM77SR476 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows, which makes it compatible with the CLEAR function on the AM27S25. $\overline{PS}$ loads ones into the output registers when brought low.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S25
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable asynchronous INITIALIZE (SR476 only)
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameter's guaranteed over temperature
- Preset input

Block and Connection Diagrams



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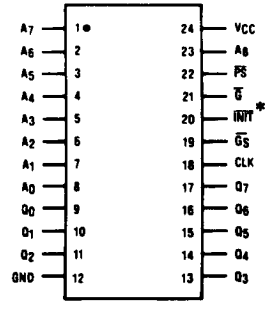

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Top View

*$\overline{CLR}$ only on DM77/87SR25

Order Number DM77/87SR476J, SR25J, SR476BJ, SR25B, DM87SR476N, SR25N, SR476BN, SR25BN, DM87SR476V, SR25V, SR476BV or SR25BV

See NS Package Number J24F, N24C or V28A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR476, 476B DM77SR25, 25B			DM87SR476, 476B DM87SR25, 25B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		135	185		135	185	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurements, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR476, 476B DM77SR25, 25B			DM87SR476, 476B DM87SR25, 25B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR476, SR25	55	20		50	20		ns
		SR476B, SR25B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR476, SR25		15	30		15	27	ns
		SR476B, SR25B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{PS})}$	Delay from $\overline{PS}$ (Low) to Output (High)			20	40		20	30	ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	40		20	30	ns
$t_{WL(\overline{PS})}$	$\overline{PS}$ Pulse Width (Low)		15	10		15	10		ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		15	10		15	10		
$t_{S(\overline{PS})}$	$\overline{PS}$ Recovery (High) to CLK (High)		25	10		20	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to CLK (High)		25	10		20	10		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (High or Low)			15	30		15	25	ns
$t_{PZL(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns