FAIRCHILD SEMICONDUCTOR®

December 2005

FDMC3300NZA

Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® MOSFET

8A,20V,26mΩ

General Description

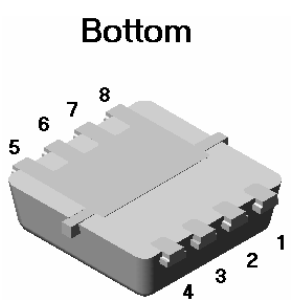
This Dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS}(on)$@V_{GS}=2.5v on special MicroFET leadframe with all the drains on one side of the package.

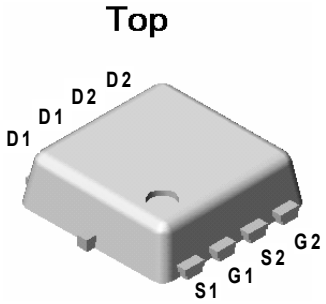
Applications

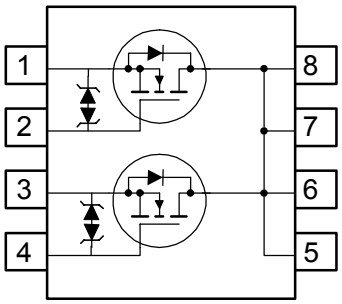
- Li-Ion Battery Pack

Features

- $R_{DS(ON)}$ = 26mΩ @ V_{GS} = 4.5 V, I_D = 8A
- $R_{DS(ON)}$ = 34mΩ @ V_{GS} = 2.5 V, I_D = 7A
- >2000V ESD protection
- Low Profile-1mm maxium-in the new package MicroFET 3.3x3.3 mm
- Pb-free and RoHS Compliant







Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current -Continuous	(Note 1a)	8	A
	-Pulsed		40	
P_D	Power dissipation (Steady State)	(Note 1a)	2.4	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	108	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	5	

Package Marking and Ordering Information

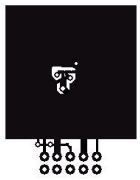
Device Marking	Device	Reel Size	Tape Width	Quantity
3300A	FDMC3300NZA	7"	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

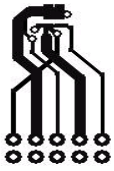
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V , I_D = 250μA	20	-	-	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	12.0	-	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{GS} = 0V,	-	-	1	μA
I_{GSS}	Gate-Body Leakage,	V_{GS} = ±12V, V_{DS} = 0V	-	-	±10	μA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	0.6	-	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	-3.1	-	mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 8A	-	20	26	mΩ
		V_{GS} = 2.5V, I_D = 7A		25	34	
		V_{GS} = 4.5V, I_D = 8A, T_J =150°C	-	29	38	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D =8 A	-	29	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} =0V, f = 1.0MHz	-	610	-	pF
C_{oss}	Output Capacitance		-	165	-	pF
C_{rss}	Reverse Transfer Capacitance		-	115	-	pF
R_G	Gate Resistance	f = 1.0MHz	-	1.7	-	Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10V, I_D = 1A V_{GS} = 4.5V, R_{GEN} = 6Ω	-	8	16	ns
t_r	Turn-On Rise Time		-	8	16	ns
$t_{d(off)}$	Turn-Off Delay Time		-	19	34	ns
t_f	Turn-Off Fall Time		-	9	18	ns
Q_g	Total Gate Charge	V_{DS} = 10V, I_D = 8A, V_{GS} = 4.5V	-	8	-	nC
Q_{gs}	Gate-Source Charge		-	1	-	nC
Q_{gd}	Gate-Drain Charge		-	2	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 2A (Note 2)	-	0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F= 8A, dI_F/dt=100A/μs	-	-	21	ns
Q_{rr}	Diode Reverse Recovery Charge		-	-	6	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 oz.copper pad on a 1.5x1.5 in board of FR-4 material .$R_{\theta JC}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. **52**°C/W when mounted on a 1 in^2 pad of 2 oz



b. **108**°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

Typical Characteristics T_J = 25°C unless otherwise noted

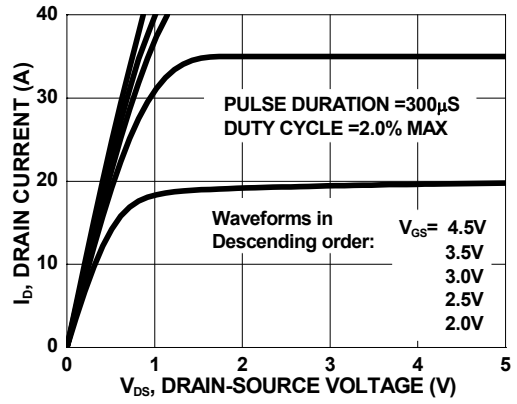


Figure 1. On Region Characteristics

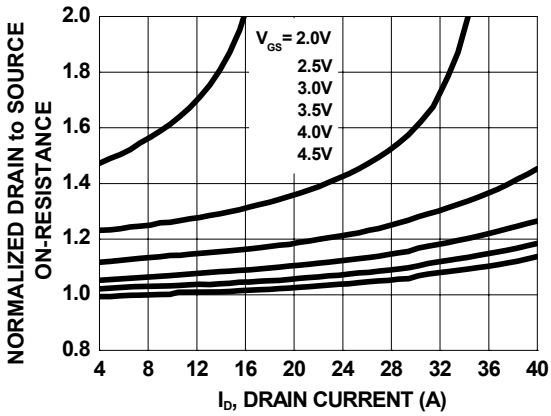


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

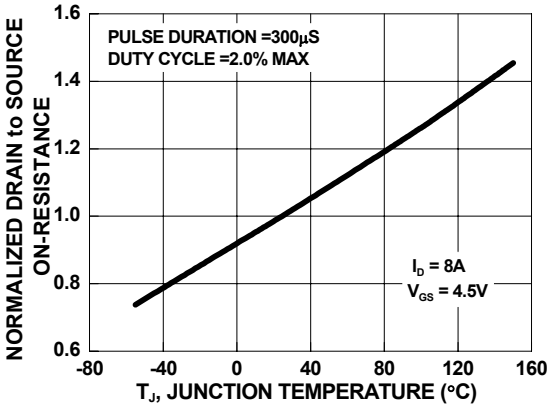


Figure 3. On Resistance Variation with Temperature

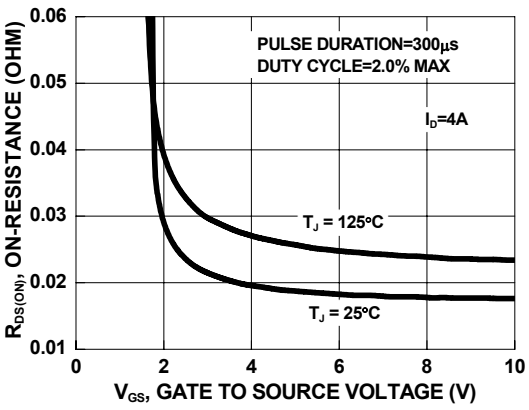


Figure 4. On-Resistance Variation with Gate-to-Source Votlage

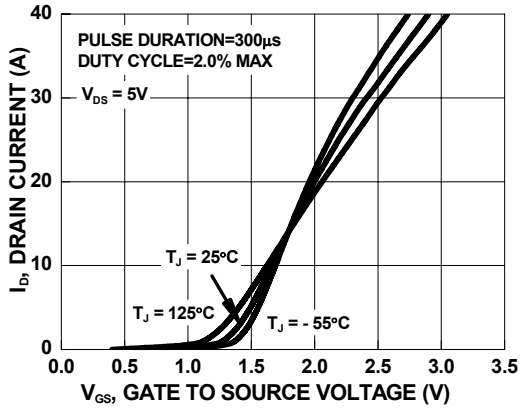


Figure 5. Transfer Characteristics

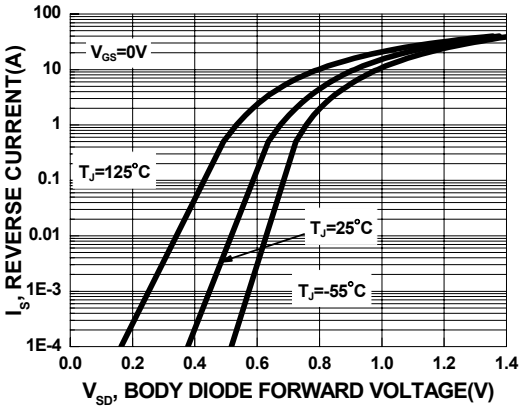


Figure 6. Body Diode Forward Voltage Variation With Source Current and Temperature

Typical Characteristics T_J = 25°C unless otherwise noted

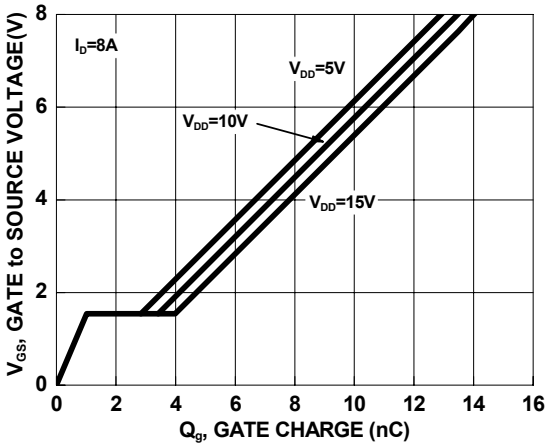


Figure 7. Gate Charge Characteristics

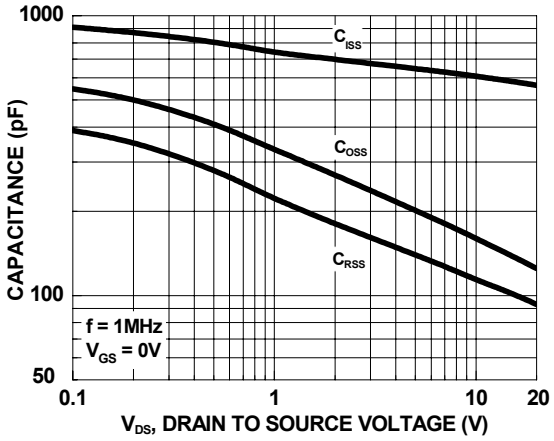


Figure 8. Capacitance Characteristics

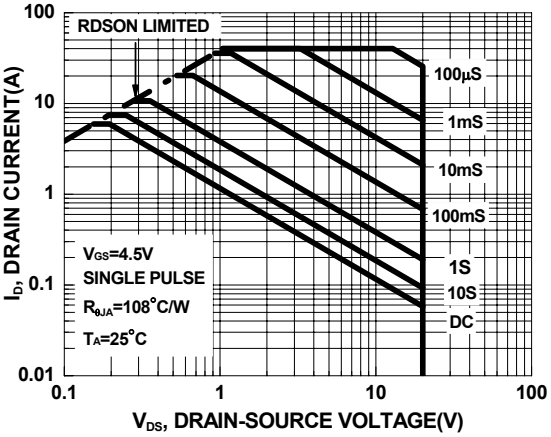


Figure 9. Safe Operating Area

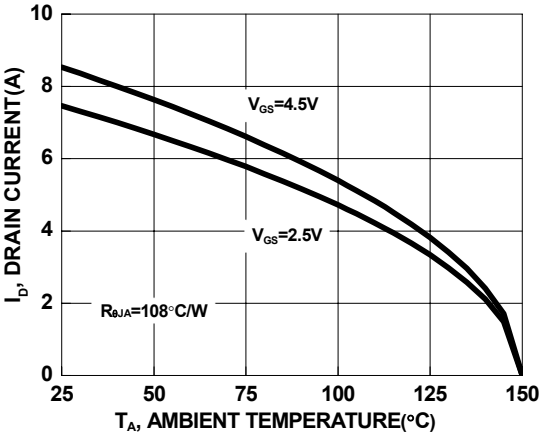


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

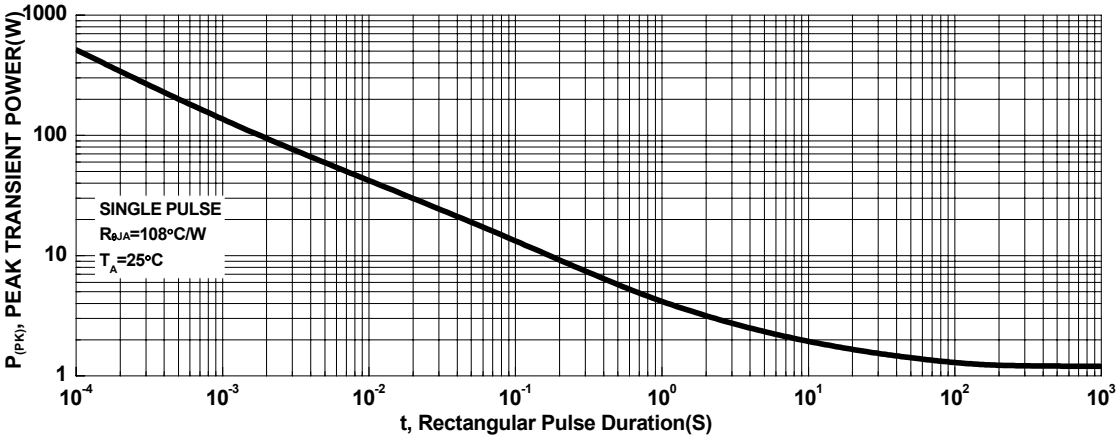


Figure 11. Single Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

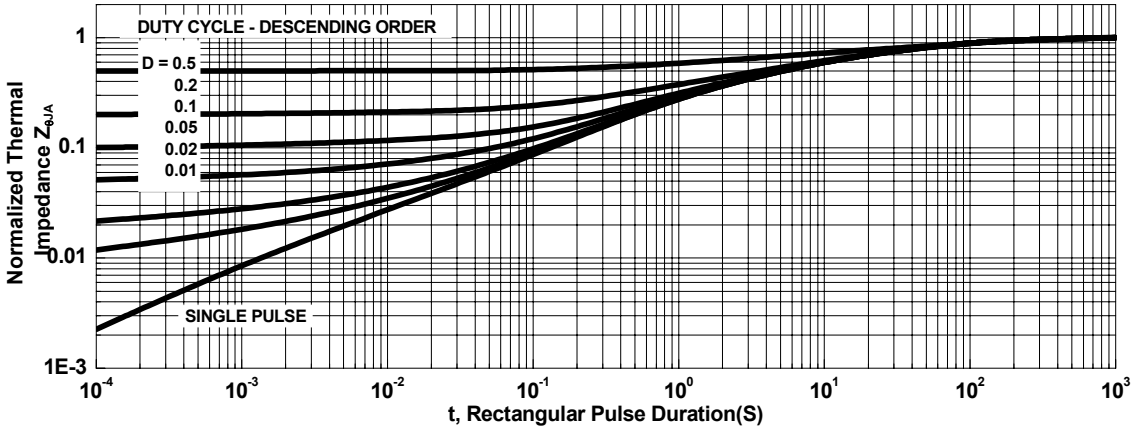
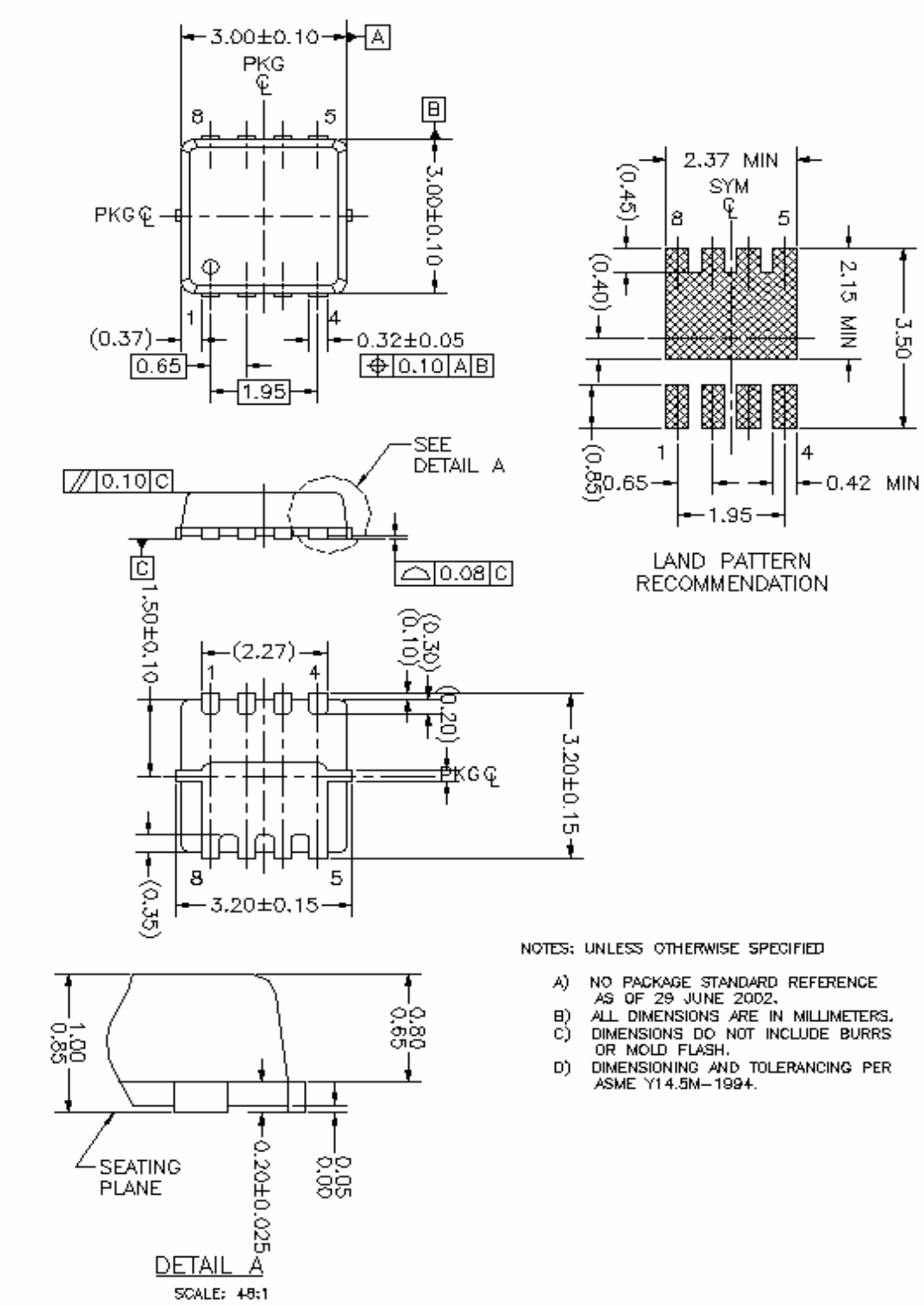


Figure 12. Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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