INA326
INA327

SBOS222 – DECEMBER 2001

Precision, Rail-to-Rail I/O INSTRUMENTATION AMPLIFIER

FEATURES

- **PRECISION**
  - **LOW OFFSET: 125μV (max)**
  - **LOW OFFSET DRIFT: 1μV/°C (max)**
  - **EXCELLENT LONG-TERM STABILITY**
  - **VERY-LOW 1/f NOISE**
- **TRUE RAIL-TO-RAIL I/O**
  - **INPUT COMMON-MODE RANGE: 20mV Beyond Rails**
  - **WIDE OUTPUT SWING: Within 10mV of Rails**
  - **SUPPLY RANGE: Single +2.7V to +5.5V**
- **SMALL SIZE**
  - ***micro*PACKAGE: MSOP-8**
- **LOW COST**

APPLICATIONS

- **LOW-LEVEL TRANSDUCER AMPLIFIER FOR BRIDGES, LOAD CELLS, THERMOCOUPLES**
- **WIDE DYNAMIC RANGE SENSOR MEASUREMENTS**
- **HIGH-RESOLUTION TEST SYSTEMS**
- **WEIGH SCALES**
- **MULTI-CHANNEL DATA ACQUISITION SYSTEMS**
- **MEDICAL INSTRUMENTATION**
- **GENERAL-PURPOSE**

DESCRIPTION

The INA326 is a high-performance, low-cost, precision instrumentation amplifier with rail-to-rail input and output. It is a true single-supply instrumentation amplifier with very-low DC errors and input common-mode range that extends beyond the positive and negative rails. These features make them suitable for applications ranging from general-purpose to high-accuracy.

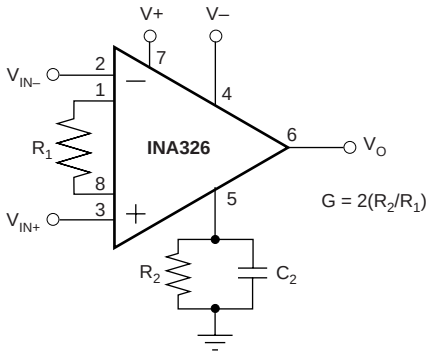
Excellent long-term stability and very low 1/f noise assure low offset voltage and drift throughout the life of the product.

The INA326 is specified over the extended industrial temperature range, –40°C to +85°C, with operation from –40°C to +125°C.

The INA327, with shutdown and synchronization, will be available Q1 2002.

INA326 AND INA327 RELATED PRODUCTS

PRODUCT	FEATURES
INA114	50μV V_{OS}, 0.5nA I_B, 115dB CMR, 3mA I_Q, 0.25μV/°C drift
INA118	50μV V_{OS}, 1nA I_B, 120dB CMR, 385μA I_Q, 0.5μV/°C drift
INA122	250μV V_{OS}, –10nA I_B, 85μA I_Q, Rail-to-Rail Output, 3μV/°C drift
INA128	50μV V_{OS}, 2nA I_B, 125dB CMR, 750μA I_Q, 0.5μV/°C drift
INA321	500μV V_{OS}, 0.5pA I_B, 94dB CMRR, 60μA I_Q, Rail-to-Rail Output



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
INA326	MSOP-8	DGK	–40°C to +85°C	B26	INA326EA/250	Tape and Reel, 250
"	"	"	"	"	INA326EA/2K5	Tape and Reel, 2500
"(2)	MSOP-8	DGK	–40°C to +125°C	B26	INA326IDGKT	Tape and Reel, 250
"	"	"	"	"	INA326IDGKR	Tape and Reel, 2500
INA327(2)	MSOP-10	DGS	–40°C to +85°C	B27	INA327EA/250	Tape and Reel, 250
"	"	"	"	"	INA327EA/2K5	Tape and Reel, 2500
"(2)	MSOP-10	DGS	–40°C to +125°C	B27	INA327IDGST	Tape and Reel, 250
"	"	"	"	"	INA327IDGSR	Tape and Reel, 2500

NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com. (2) INA326I with 125°C range and INA327 available Q1 2002—specifications of 125°C parts may differ.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals: Voltage(2)	–0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short-Circuit	Continuous
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

ELECTROSTATIC DISCHARGE SENSITIVITY

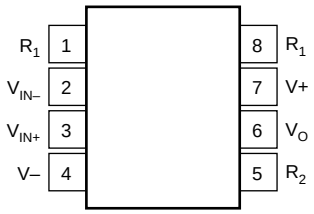
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

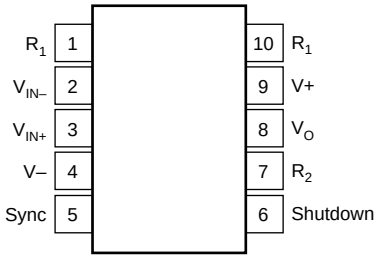
Top View

INA326



MSOP-8

INA327(1)



MSOP-10

NOTE: (1) INA327 expected Q1 2002.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V TO +5.5V

BOLDFACE limits apply over the specified temperature range, T_A = –40°C TO 85°C

At T_A = +25°C, R_L = 10kΩ, G = 100 (R_1 = 2kΩ, R_2 = 100kΩ), external gain set resistors, and $IA_{COMMON} = V_S/2$, with external 1kHz filters, unless otherwise noted.

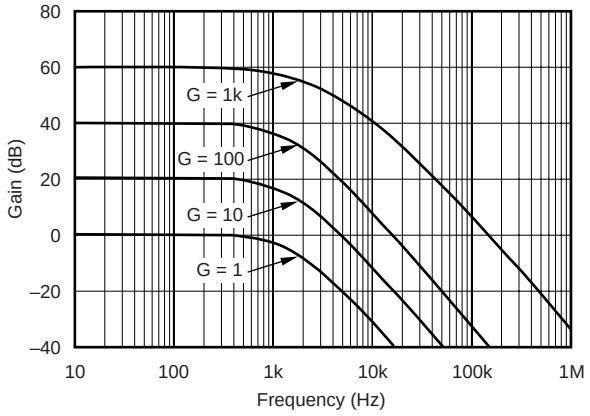
PARAMETER		CONDITION	INA326EA MIN	INA326EA TYP	INA326EA MAX	UNITS
INPUT						
Offset Voltage, RTI	V_{OS}	V_S = +5V, $V_{CM} = V_S/2$		±30	±125	µV
Over Temperature					**±185**	µV
vs Temperature	**dV_{OS}/dT**			**±0.15**	**±1**	µV/°C
vs Power Supply	PSR	V_S = +2.7V to +5.5V, $V_{CM} = V_S/2$	±20	±4		µV/V
Long-Term Stability				See Note (1)		
Input Impedance, Differential				10^{10} || 2		Ω || pF
Common-Mode				10^{10} || 14		Ω || pF
Input Voltage Range			**–0.02**		**(V+) + 0.02**	**V**
Safe Input Voltage			–0.5		(V+) + 0.5	V
Common-Mode Rejection	CMR	V_S = 5V, V_{CM} = –0.02V to (V+) + 0.02V	100	110		dB
Over Temperature			**94**			dB
INPUT BIAS CURRENT		$V_{CM} = V_S/2$				
Bias Current	I_B	V_S = 5V		±0.2	±2	nA
vs Temperature				**See Typical Characteristics**		
Offset Current	I_{OS}	V_S = 5V		±0.2	±2	nA
NOISE						
Voltage Noise, RTI		R_S = 0Ω, G = 100, R_1 = 2kΩ, R_2 = 100kΩ				
f = 10Hz				44		nV/√Hz
f = 100Hz				44		nV/√Hz
f = 1kHz				44		nV/√Hz
f = 0.01Hz to 10Hz				1		µVp-p
Voltage Noise, RTI		R_S = 0Ω, G = 10, R_1 = 20kΩ, R_2 = 100kΩ				
f = 10Hz				120		nV/√Hz
f = 100Hz				97		nV/√Hz
f = 1kHz				97		nV/√Hz
f = 0.01Hz to 10Hz				4		µVp-p
Current Noise, RTI						
f = 1kHz				0.15		pA/√Hz
f = 0.1Hz to 10Hz				4.2		pAp-p
Output Ripple, V_O Filtered[2]				See Applications Information		
GAIN						
Gain Equation				$G = 2(R_2/R_1)$		
Range of Gain			< 0.1		> 10000	V/V
Gain Error[3]		G = 10, 100, V_S = 5V, V_O = 0.075V to 4.925V		±0.25	±0.5	%
vs Temperature		G = 10, 100, V_S = 5V, V_O = 0.075V to 4.925V		**±10**	**±60**	ppm/°C
Nonlinearity		G = 10, 100, V_S = 5V, V_O = 0.075V to 4.925V		±0.01	±0.024	% of FS
OUTPUT						
Voltage Output Swing from Rail		R_L = 100kΩ		5		mV
		R_L = 10kΩ, V_S = 5V	75	10		mV
Over Temperature			**75**			**mV**
Capacitive Load Drive				500		pF
Short-Circuit Current	I_{SC}			±25		mA
INTERNAL OSCILLATOR						
Frequency of Auto-Correction				90		kHz
Accuracy				±20		%
FREQUENCY RESPONSE						
Bandwidth[4], –3dB	BW	G = 1 to 1k		1		kHz
Slew Rate[4]	SR	V_S = 5V, All Gains, C_L = 100pF		Filter Limited		
Settling Time[4], 0.1%	t_S	1kHz Filter, G = 1 to 1k, V_O = 2V step, C_L = 100pF		0.95		ms
0.01%				1.3		ms
0.1%		10kHz Filter, G = 1 to 1k, V_O = 2V step, C_L = 100pF		130		µs
0.01%				160		µs
Overload Recovery[4]		1kHz Filter, 50% Output Overload, G = 1 to 1k		30		µs
		10kHz Filter, 50% Output Overload, G = 1 to 1k		5		µs
POWER SUPPLY						
Specified Voltage Range			+2.7		+5.5	V
Quiescent Current	I_Q	I_O = 0, Diff V_{IN} = 0V, V_S = 5V		2.4	3.4	mA
Over Temperature					**3.7**	**mA**
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range			–40		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}	MSOP-8 Surface Mount		150		°C/W

NOTES: (1) 1000-hour life test at 150°C demonstrated randomly distributed variation in the range of measurement limits—approximately 10µV. (2) See Applications Information section, Figures 1 and 2. (3) Does not include error and TCR of external gain-setting resistors. (4) Dynamic response is limited by filtering. Higher bandwidths can be achieved by adjusting the filter.

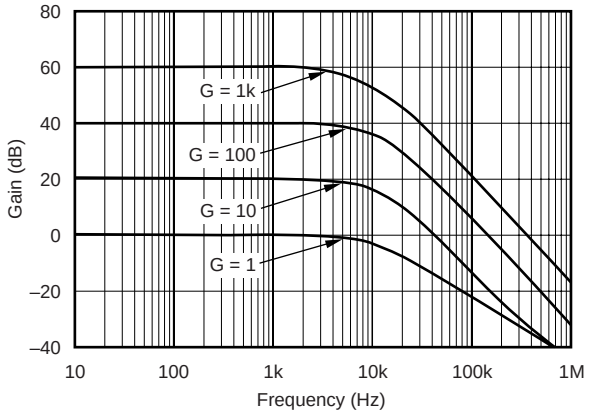
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = +5V, Gain = 100, R_L = 10kΩ with external 1kHz filters, unless otherwise noted.

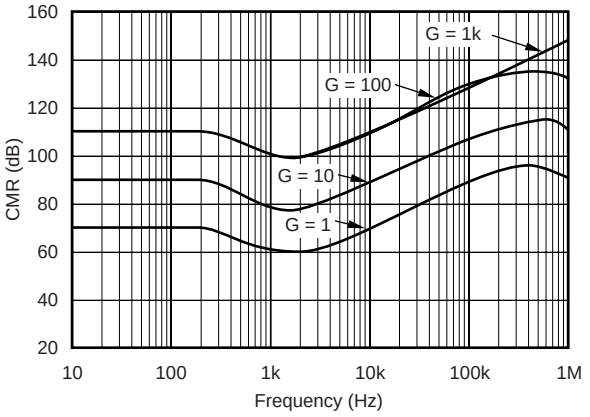
GAIN vs FREQUENCY
1kHz FILTER



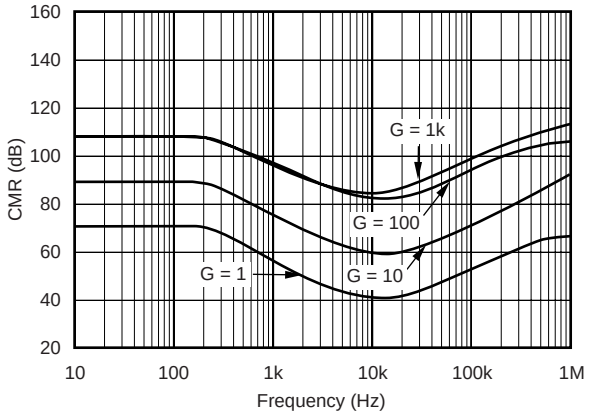
GAIN vs FREQUENCY
10kHz FILTER



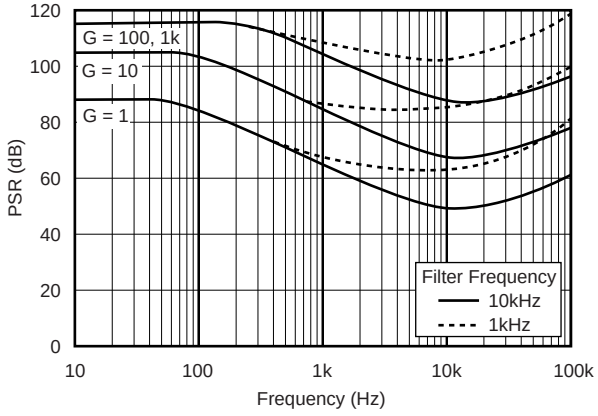
CMR vs FREQUENCY
1kHz FILTER



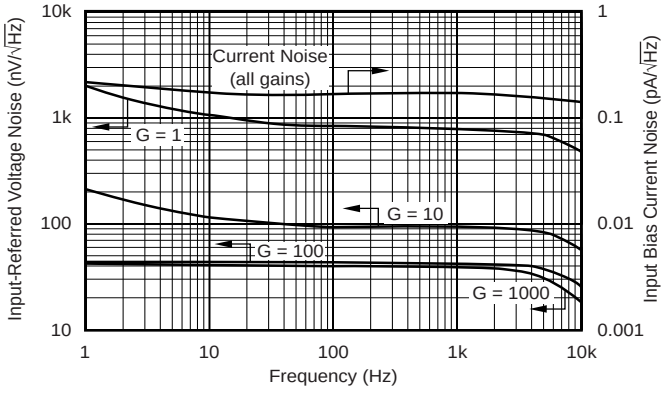
CMR vs FREQUENCY
10kHz FILTER



POWER-SUPPLY REJECTION vs FREQUENCY



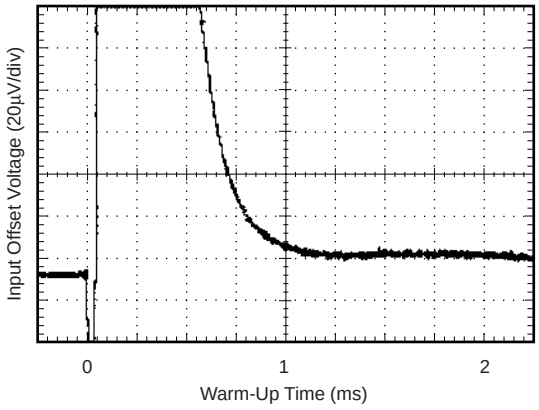
INPUT-REFERRED VOLTAGE NOISE AND
INPUT BIAS CURRENT NOISE vs FREQUENCY
10kHz Filter



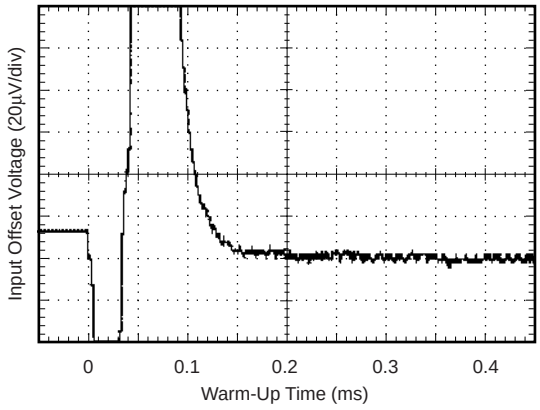
TYPICAL CHARACTERISTICS (Cont.)

At T_A = 25°C, V_S = +5V, Gain = 100, R_L = 10kΩ with external 1kHz filters, unless otherwise noted.

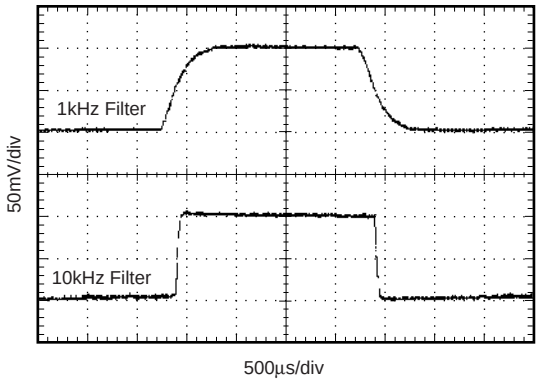
INPUT OFFSET VOLTAGE vs WARM-UP TIME
1kHz FILTER, G = 100



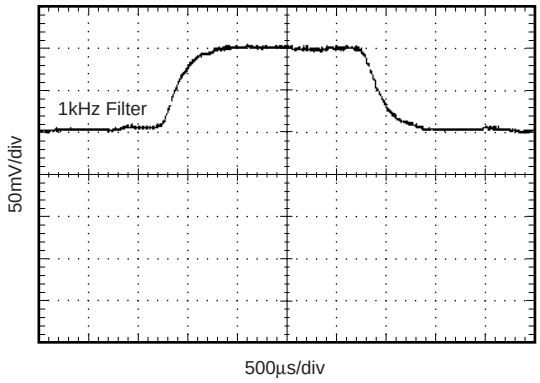
INPUT OFFSET VOLTAGE vs WARM-UP TIME
10kHz FILTER, G = 100



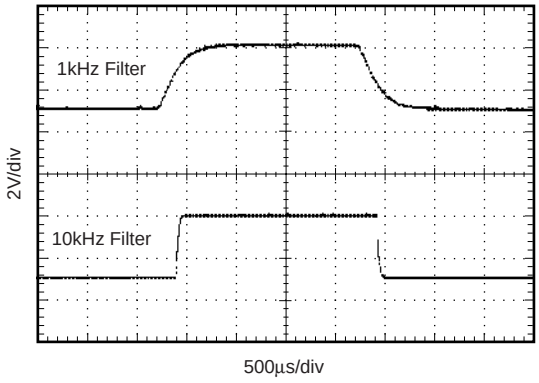
SMALL-SIGNAL RESPONSE
G = 1, 10, AND 100



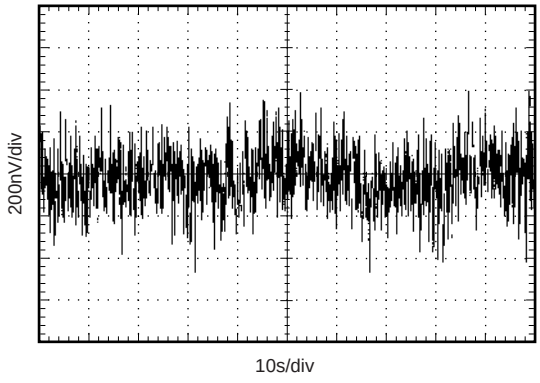
SMALL-SIGNAL STEP RESPONSE
G = 1000



LARGE-SIGNAL RESPONSE
G = 1 TO 1000



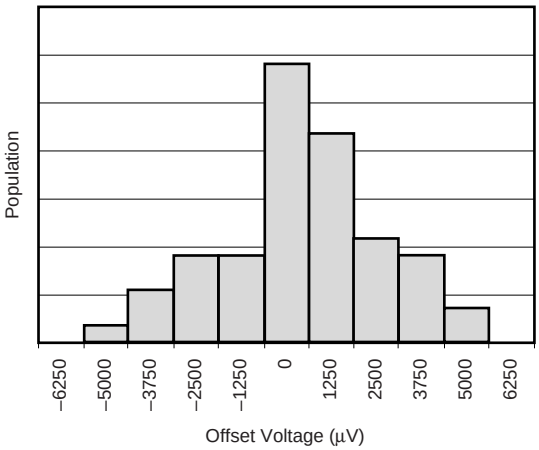
0.01Hz TO 10Hz VOLTAGE NOISE



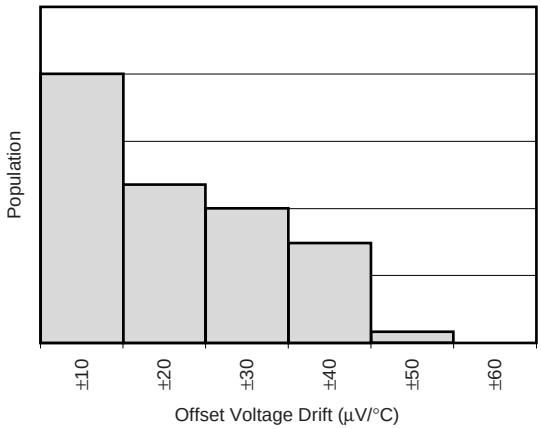
TYPICAL CHARACTERISTICS (Cont.)

At T_A = 25°C, V_S = +5V, Gain = 100, R_L = 10kΩ with external 1kHz filters, unless otherwise noted.

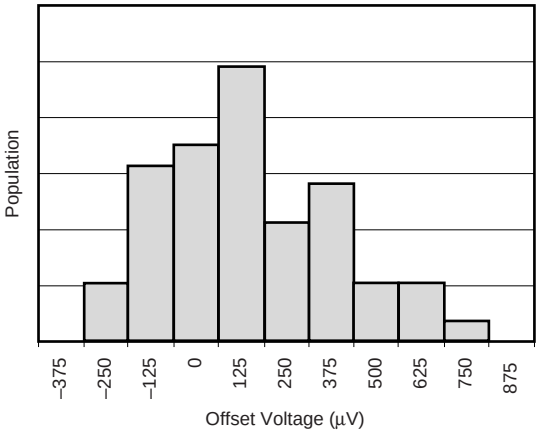
OFFSET VOLTAGE PRODUCTION DISTRIBUTION
G = 1



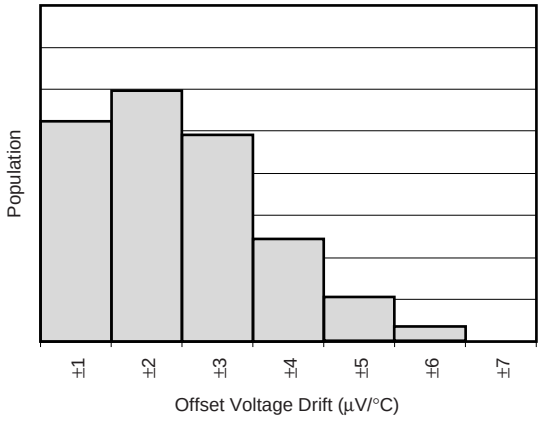
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION
G = 1



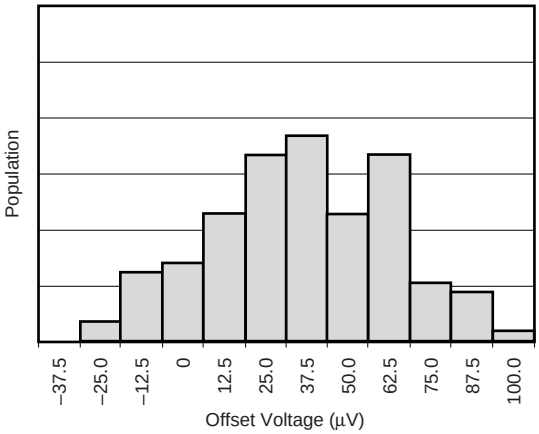
OFFSET VOLTAGE PRODUCTION DISTRIBUTION
G = 10



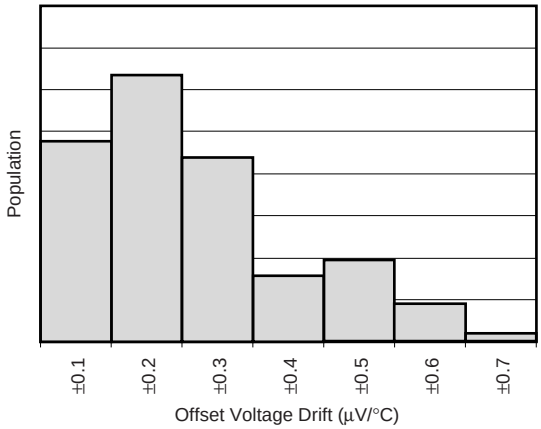
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION
G = 10



OFFSET VOLTAGE PRODUCTION DISTRIBUTION
G = 100, 1000



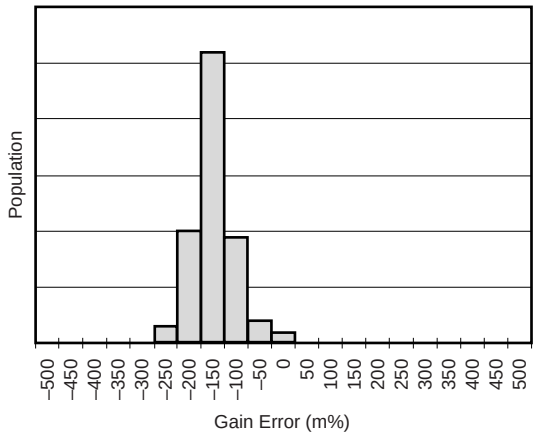
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION
G = 100, 1000



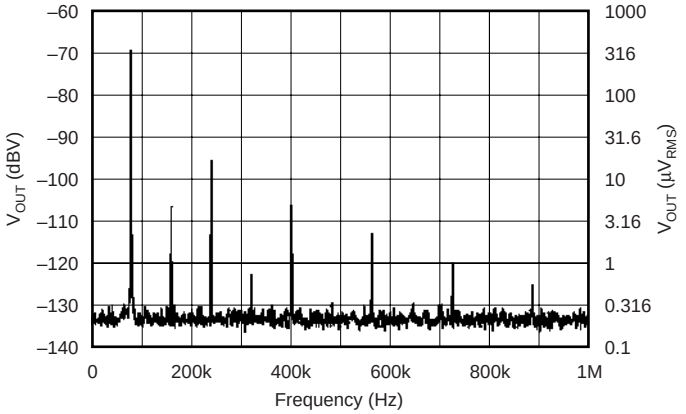
TYPICAL CHARACTERISTICS (Cont.)

At T_A = 25°C, V_S = +5V, Gain = 100, R_L = 10kΩ with external 1kHz filters, unless otherwise noted.

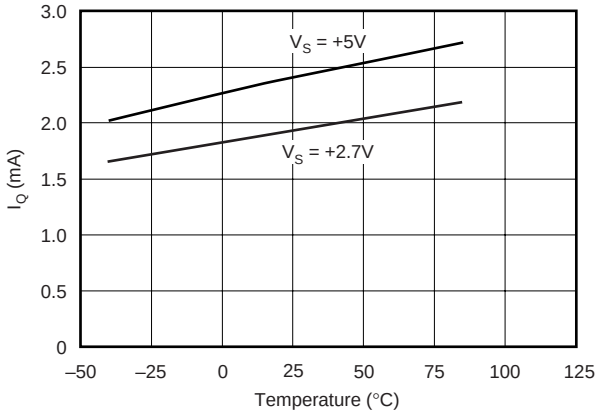
GAIN ERROR PRODUCTION DISTRIBUTION



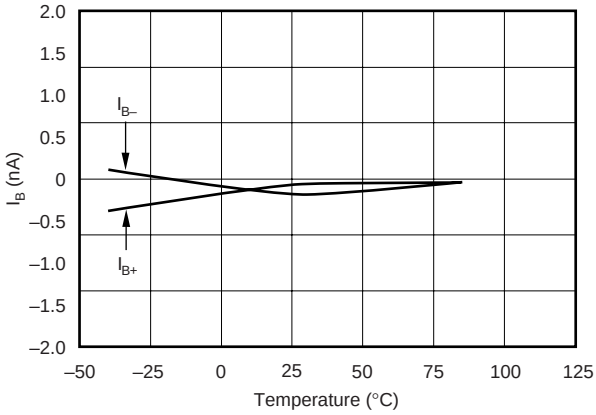
OUTPUT RIPPLE SPECTRUM
G = 100



QUIESCENT CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA326. A 0.1µF capacitor, placed close to and across the power supply pins is strongly recommended for highest accuracy. R_oC_o is an output filter that minimizes auto-correction circuitry noise. This output filter may also serve as an anti-aliasing filter ahead of an Analog-to-Digital (A/D) converter. It is also optional based on desired precision.

The output reference terminal is taken at the low side of R_2 (IA_{COMMON}).

The INA326 uses a unique internal topology to achieve excellent common-mode rejection (CMR). Unlike conventional instrumentation amplifiers, CMR is not affected by resistance in the reference connections or sockets. See "Inside the INA326" for further detail. To achieve best high-frequency CMR, minimize capacitance on pins 1 and 8.

SETTING THE GAIN

The INA326 is a two-stage amplifier with each stage gain set by R_1 and R_2, respectively (see Figure 4, "inside the INA326", for details.) Overall gain is described by the equation:

$$G = \frac{2R_2}{R_1} \quad (1)$$

The stability and temperature drift of the external gain-setting resistors will affect gain by an amount that can be directly inferred from the gain equation (1).

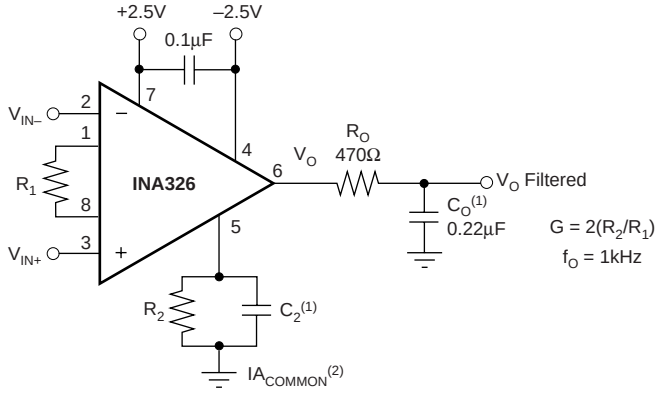
Resistor values for commonly used gains are shown in Figure 1. Gain-set resistor values for best performance are different for +5V single-supply and for ±2.5V dual-supply operation. Optimum value for R_1 can be calculated by:

$$R_1 = V_{IN,\ MAX}/12.5\mu A \quad (2)$$

where R_1 must be no less than 2kΩ.

Dual-Supply Operation

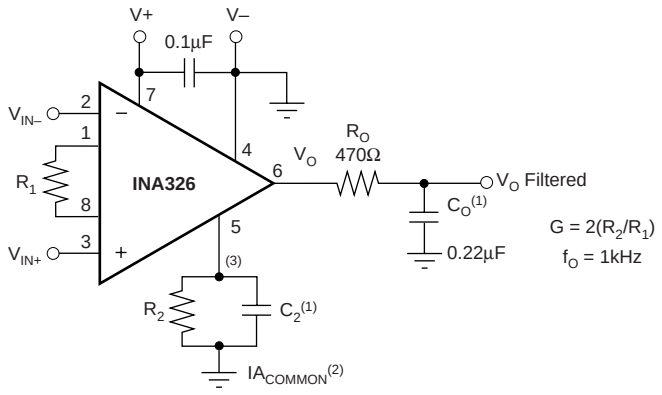
DESIRED GAIN	R_1 (Ω)	R_2 || C_2 (Ω || nF)
0.1	400k	20k || 5
0.2	400k	40k || 2.5
0.5	400k	100k || 1
1	200k	100k || 1
2	100k	100k || 1
5	40k	100k || 1
10	20k	100k || 1
20	10k	100k || 1
50	4k	100k || 1
100	2k	100k || 1
200	2k	200k || 0.5
500	2k	500k || 0.2
1000	2k	1M || 0.1
2000	2k	2M || 0.05
5000	2k	5M || 0.02
10000	2k	10M || 0.01



NOTE: (1) C_2 and C_O combine to form a 2-pole response that is –3dB at 1kHz. Each individual pole is at 1.5kHz. (2) Output voltage is referenced to IA_{COMMON} (see text).

Single-Supply Operation

DESIRED GAIN	R_1 (Ω)	R_2 || C_2 (Ω || nF)
0.1	400k	20k || 5
0.2	400k	40k || 2.5
0.5	400k	100k || 1
1	400k	200k || 0.5
2	200k	200k || 0.5
5	80k	200k || 0.5
10	40k	200k || 0.5
20	20k	200k || 0.5
50	8k	200k || 0.5
100	4k	200k || 0.5
200	2k	200k || 0.5
500	2k	500k || 0.2
1000	2k	1M || 0.1
2000	2k	2M || 0.05
5000	2k	5M || 0.02
10000	2k	10M || 0.01



NOTE: (1) C_2 and C_O combine to form a 2-pole response that is –3dB at 1kHz. Each individual pole is at 1.5kHz. (2) Output voltage is referenced to IA_{COMMON} (see text). (3) Output pedestal required for measurement near zero (see Figure 5).

FIGURE 1. Basic Connections.

Following this design procedure for R_1 produces the maximum possible input stage gain for best accuracy and lowest noise.

Circuit layout and supply bypassing can affect performance. Minimize the stray capacitance on pins 1 and 8. Use recommended supply bypassing, including a capacitor directly from pin 7 to pin 4 (V+ to V–), even with dual (split) power supplies (see Figure 1).

DYNAMIC PERFORMANCE

The typical characteristic “Gain vs Frequency” shows that the INA326 has nearly constant bandwidth regardless of gain. This results from the bandwidth limiting from the recommended filters.

NOISE PERFORMANCE

Internal auto-correction circuitry eliminates virtually all 1/f noise (noise that increases at low frequency) in gains of 100 or greater. Noise performance is affected by gain-setting resistor values. Follow recommendations in the “Setting Gain” section for best performance.

Total noise is a combination of input stage noise and output stage noise. When referred to the input, the total mid-band noise is:

$$V_N = 44nV/\sqrt{Hz} + \frac{800nV/\sqrt{Hz}}{G} \qquad (3)$$

The output noise has some 1/f components that affect performance in gains less than 10. See typical characteristic “Input-Referred Voltage Noise vs Frequency.”

High-frequency noise is created by internal auto-correction circuitry and is highly dependent on the filter characteristics chosen. This may be the dominant source of noise visible when viewing the output on an oscilloscope. Low cutoff frequency filters will provide lowest noise. Figure 2 shows the typical noise performance as a function of cutoff frequency.

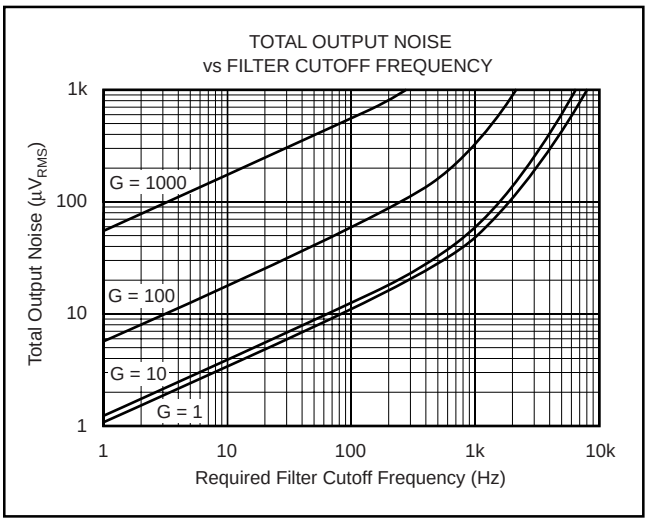


FIGURE 2. Total Output Noise vs Filter Cutoff Frequency.

Applications sensitive to the spectral characteristics of high-frequency noise may require consideration of the spurious frequencies generated by internal clocking circuitry. “Spurs” occur at approximately 90kHz and its harmonics (see typical characteristic “Output Spectrum”) which may be reduced by additional filtering below 1kHz.

Insufficient filtering at pin 5 can cause nonlinearity with large output voltage swings (very near the supply rails). Noise must be sufficiently filtered at pin 5 so that noise peaks do not “hit the rail” and change the average value of the signal. Figure 2 shows guidelines for filter cutoff frequency.

HIGH-FREQUENCY NOISE

C_2 and C_O form filters to reduce internally generated auto-correction circuitry noise. Filter frequencies can be chosen to optimize the tradeoff between noise and frequency response of the application, as shown in Figure 2. The cutoff frequencies of the filters are generally set to the same frequency. Figure 2 shows the typical output noise for four gains as a function of the –3dB cutoff frequency of the combined two-pole response. This is equal to the –1.5dB response frequency of each of the 1-pole filters. Small signals may exhibit the addition of internally generated auto-correction circuitry noise at the output. This noise, combined with broadband noise, becomes most evident in higher gains with filters of wider bandwidth.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA326 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±0.2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows provision for an input bias current path in a thermocouple application. Without a bias current path, the inputs will float to an undefined potential and the output voltage may not be valid.

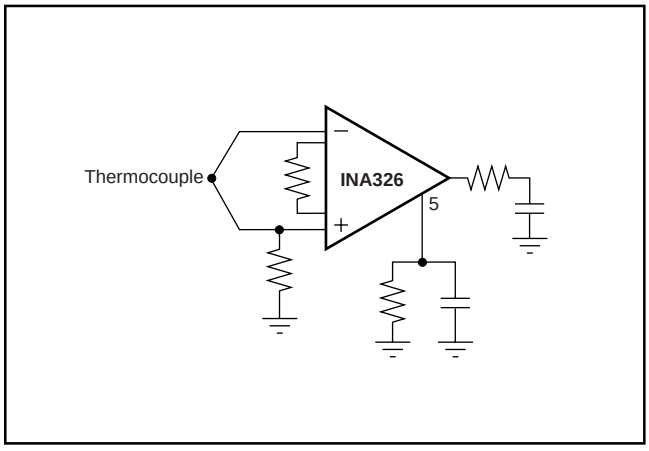


FIGURE 3. Providing Input Bias Current Return Path.

INPUT COMMON-MODE RANGE

Common instrumentation amplifiers do not respond linearly with common-mode signals near the power-supply rails, even if “rail-to-rail” op amps are used. The INA326 uses a unique topology to achieve true rail-to-rail input behavior (see “Inside the INA326”). The linear input voltage range of each input terminal extends to 20mV beyond the rails.

INPUT PROTECTION

The inputs of the INA326 are protected with internal diodes connected to the power-supply rails. These diodes will clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.5V, the input signal current should be limited to less than 10mA to protect the internal clamp diodes. This can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

INSIDE THE INA326

The INA326 uses a new, unique internal circuit topology that provides true rail-to-rail input. Unlike other instrumentation amplifiers, it can linearly process inputs up to 20mV beyond the power-supply rails. Conventional instrumentation amplifier circuits cannot deliver such performance, even if rail-to-rail op amps are used.

The ability to reject common-mode signals is derived in most instrumentation amplifiers through a combination of amplifier CMR and accurately matched resistor ratios. The INA326 converts the input voltage to a current. Current-mode signal processing provides rejection of common-mode input voltage and power supply variation without accurately matched resistors.

A simplified diagram shows the basic circuit function. The differential input voltage, $V_{IN}+ - V_{IN}-$ is applied across R_1.

The signal-generated current through R_1 comes from A1 and A2’s output stages. A2 combines the current in R_1 with a mirrored replica of the current from A1. The resulting current in A2’s output and associated current mirror is two times the current in R_1. This current flows in (or out) of pin 5 into R_2. The resulting gain equation is:

$$G = \frac{2R_2}{R_1}$$

Amplifiers A1, A2 and their associated mirrors are powered from internal charge-pumps that provide voltage supplies that are beyond the positive and negative supply rails. As a result, the voltage developed on R_2 can actually swing 20mV *beyond* the external power supply rails. A3 provides a buffered output of the voltage on R_2. A3’s input stage is also operated from the charge-pumped power supplies for true rail-to-rail operation.

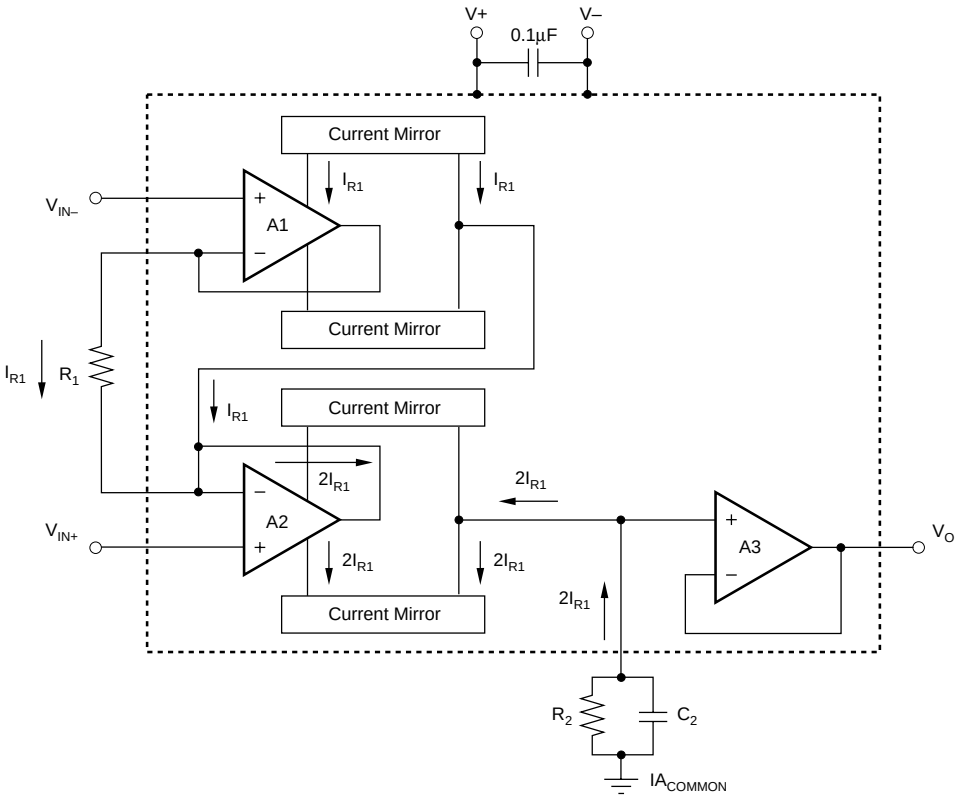


FIGURE 4. Simplified Circuit Diagram.

FILTERING

Filtering can be adjusted through selection of R_2C_2 and R_OC_O for the desired tradeoff of noise and bandwidth. Adjustment of these components will result in more or less ripple due to auto-correction circuitry noise and will also affect broadband noise. Filtering limits slew rate, settling time, and output overload recovery time.

It is generally desirable to keep the resistance of R_O relatively low to avoid DC gain error created by the subsequent stage. This may result in relatively high values for C_O to produce the desired filter response. The impedance of R_OC_O can be scaled higher to produce smaller capacitor values if the load impedance is very high.

Certain capacitor types greater than 0.1µF may have dielectric absorption effects that can significantly increase settling time in high-accuracy applications (settling to 0.01%). Polypropylene, polystyrene, and polycarbonate types are generally good. Certain "high-K" ceramic types may produce slow settling "tails." Settling time to 0.1% is not generally affected by high-K ceramic capacitors. Electrolytic types are not recommended for C_2 and C_O.

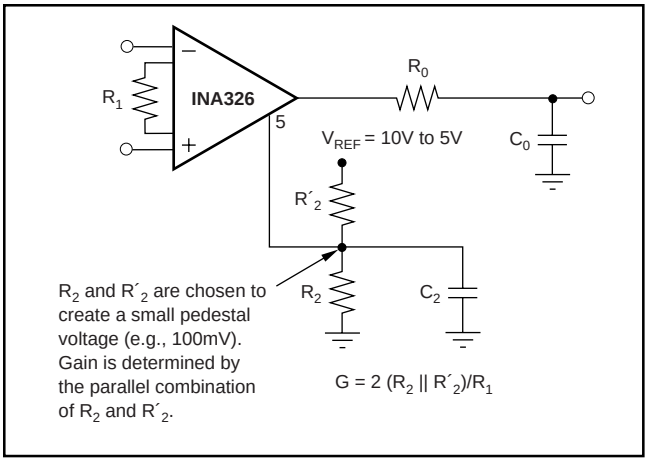


FIGURE 5. Output Range Pedestal.

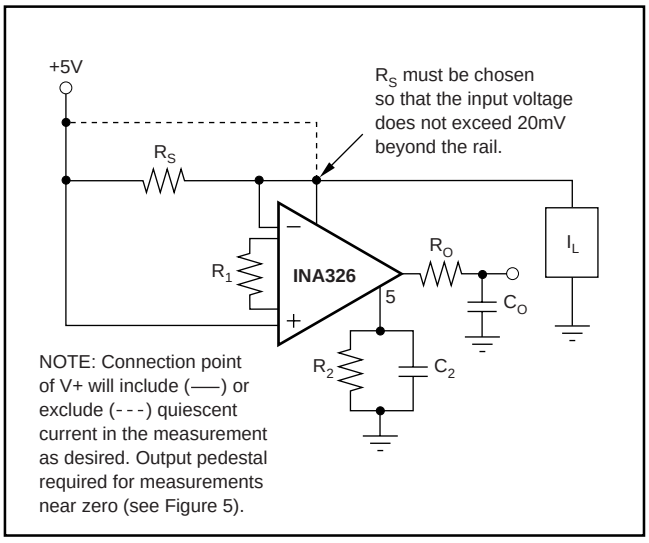


FIGURE 6. High-Side Shunt Measurement of Current Load.

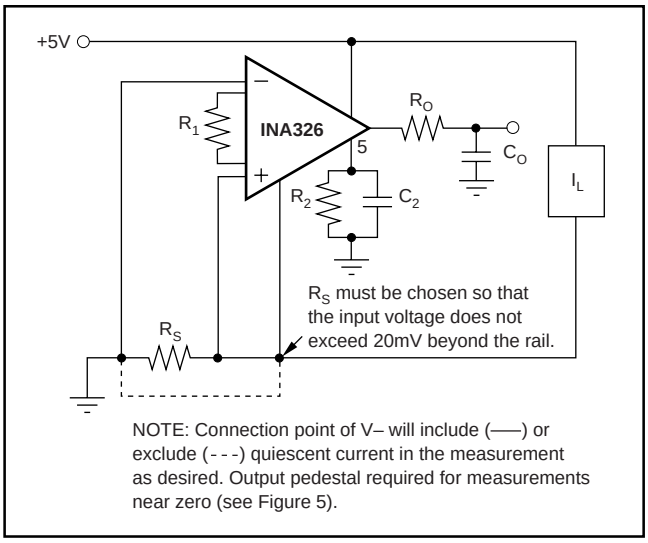


FIGURE 7. Low-Side Shunt Measurement of Current Load.

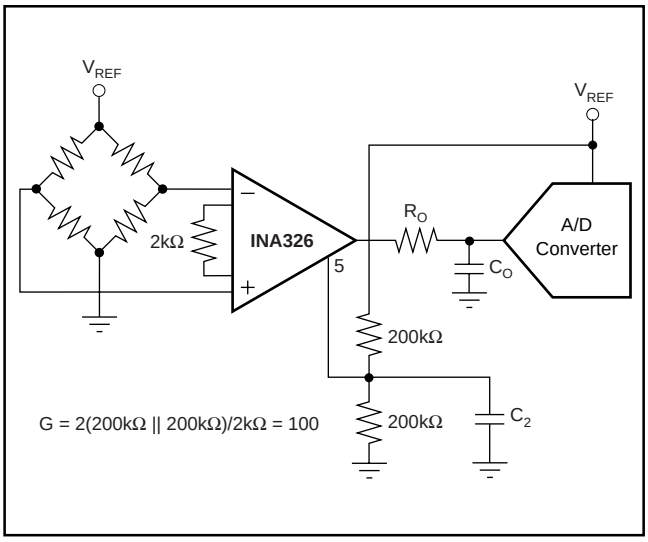


FIGURE 8. Output Referenced to $V_{REF}/2$.

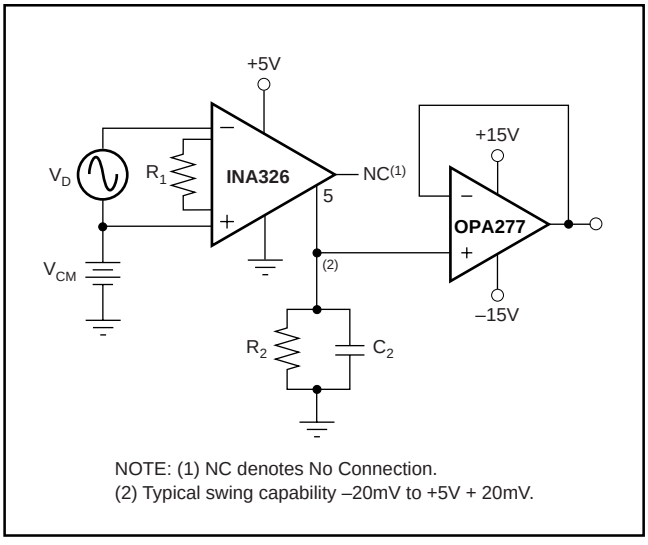


FIGURE 9. Output from Pin 5 to Allow Swing Beyond the Rail.

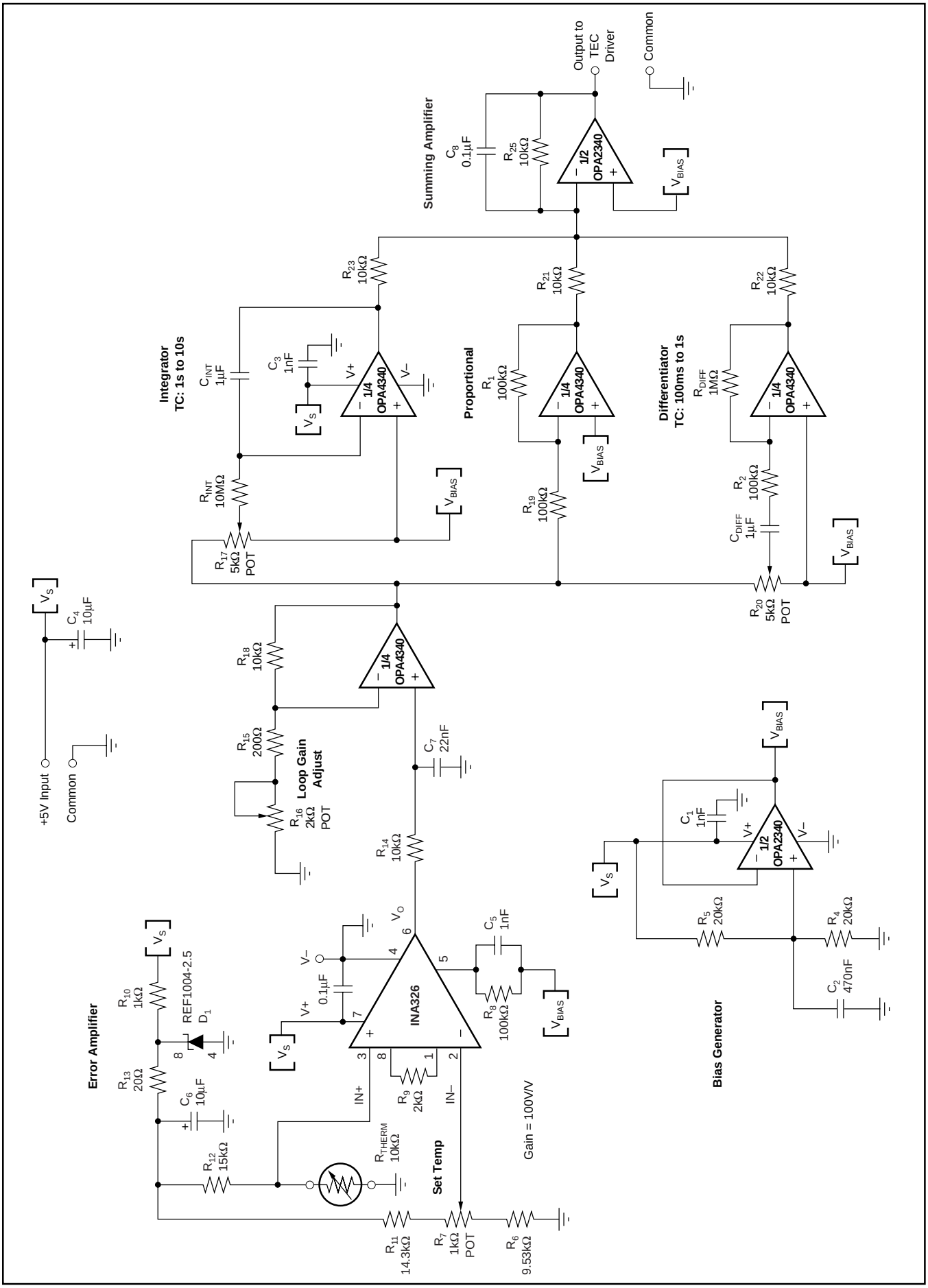
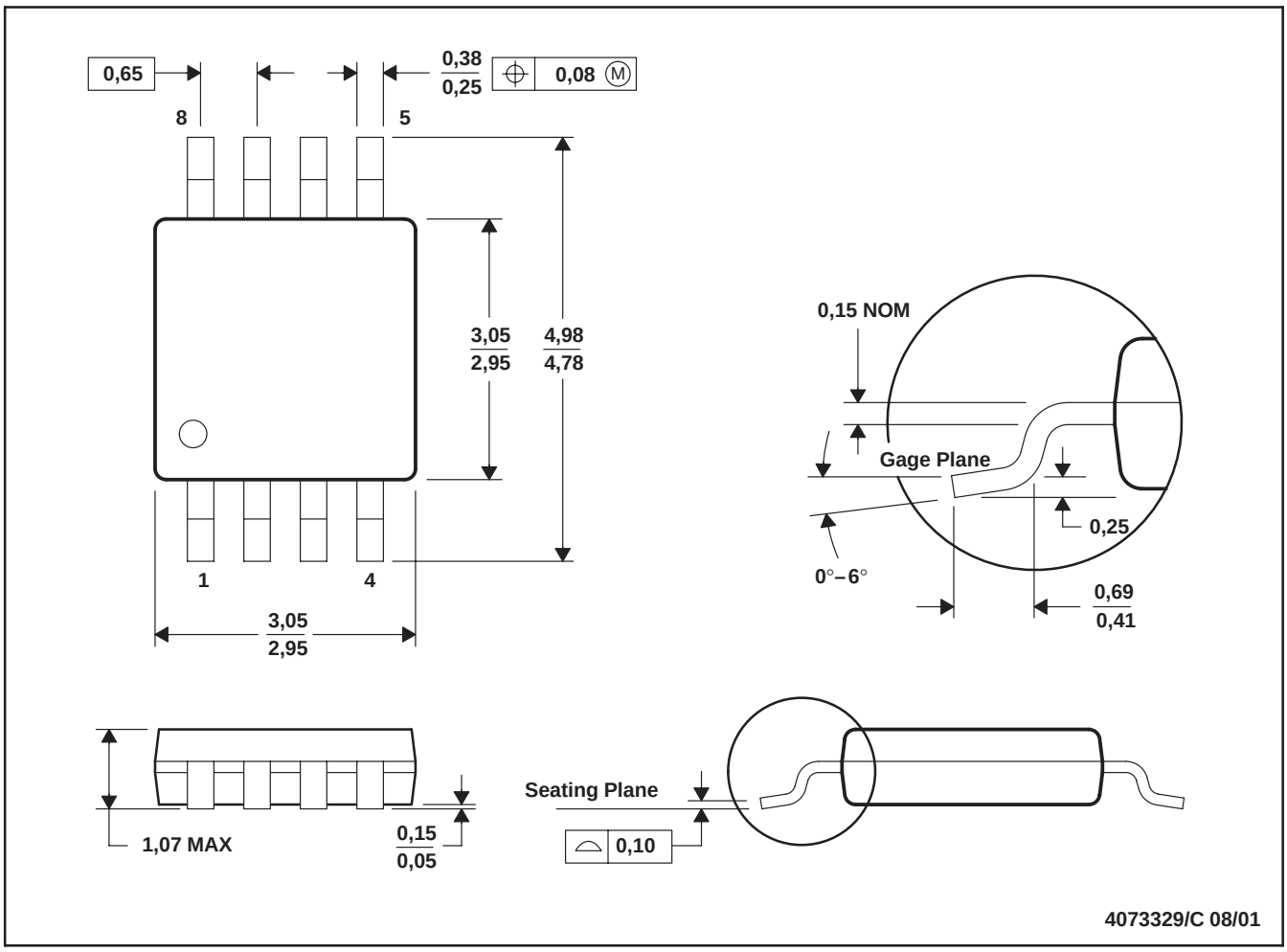


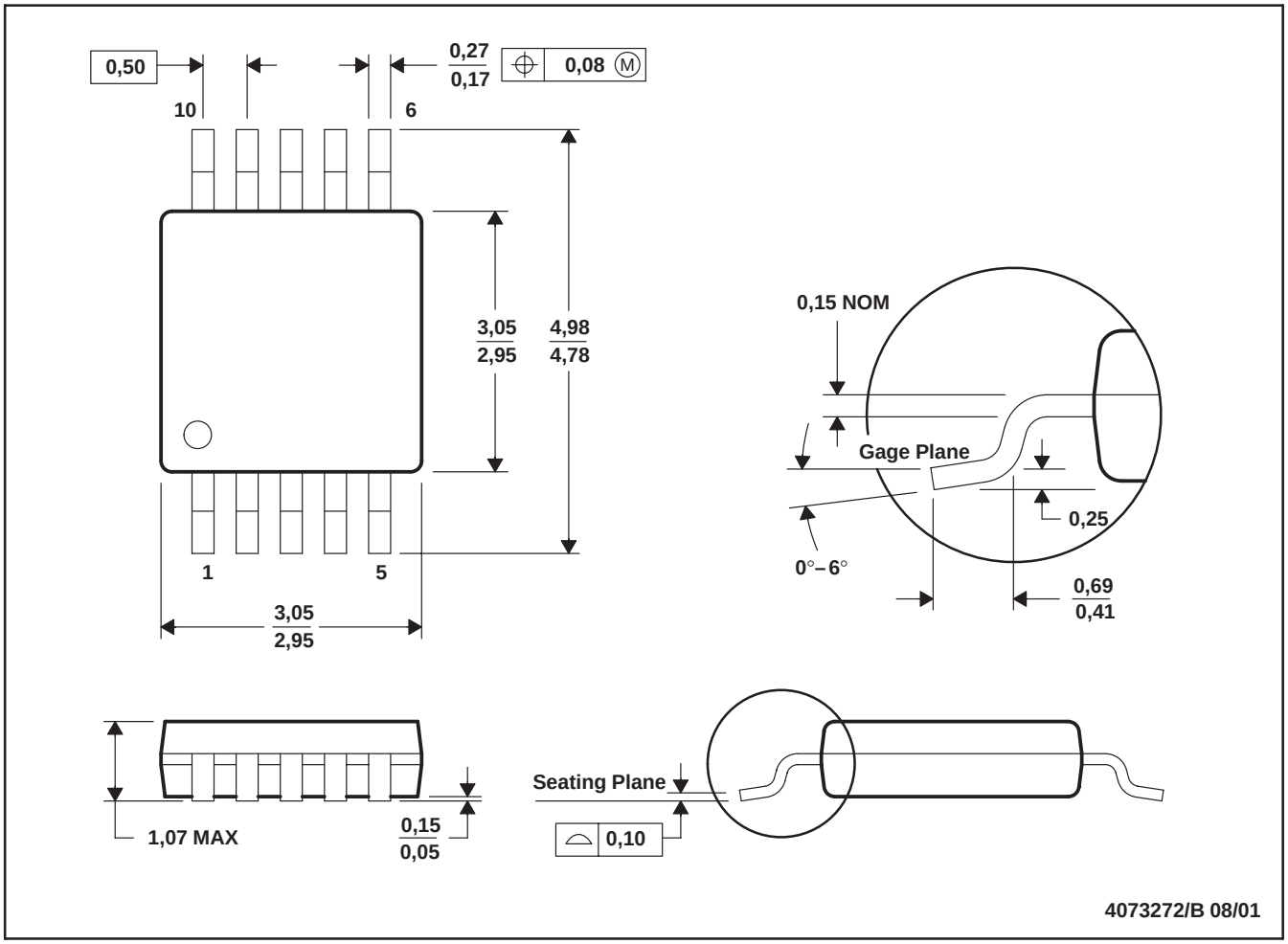
FIGURE 4. Single-Supply PID Temperature Control Loop.

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
A. Falls within JEDEC MO-187

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